Advanced
Micro
Devices

PAL Device Data Book

901 Thompson Place, P.O. Box 3453, Sunnyvale, California 94088
(408) 732-2400 TWX: 910-339-9280 TELEX: 34-6306

AMD thanks you for your interest in our programmable logic products. As world leaders and patent-holders on the PAL® device and ever-popular 22V10 architecture, we continue expanding our line in order to serve you better.

In this Data Book, we especially call your attention to our comprehensive offering of EE CMOS universal PAL devices. The distinctive *blue* pages will lead you straight to these low-power, reprogrammable choices. And please stay in touch with AMD as we have many excellent additions coming for you.

May all your projects be completed and go to market on time!

Andy Robin

Director of Marketing
Programmable Logic

Description

This 1990 PAL® Device Data Book is your complete guide to all data sheets and supporting information on programmable logic devices (PLDs) from Advanced Micro Devices, including those originally from Monolithic Memories, Inc. The blue pages highlight information relating to CMOS products.

The PAL Device Data Book is organized into eight easy-to-use sections:

1. Introduction
Includes an overview of the AMD PLD family. Highlights the advantages of each product; excellent for the new user.

2. PAL Device Data Sheets
Includes complete data sheets for all PAL devices offered by AMD, including both bipolar and CMOS devices. Order is alphanumeric.

3. Sequencer Data Sheets
Complete data sheets for the Programable Logic Sequencers (PLS) and Field-Programmable Controllers (FPC), and information on the Programmable Event Generator (PEG™ device).

4. ECL/PGA Data Sheets
Complete data sheets for the high-speed ECL PAL devices, and information on the high-density Programmable Gate Arrays (PGAs). The Programmable Gate Arrays are described in more detail in a separate PGA Data Book.

5. General Information
Includes military processing information, definitions of data sheet parameters, and package information.

6. Design and Programming
Includes information on AMD and third-party PLD software programs. Note that AMD's PALASM® software is now documented in a separate User's Manual. For design examples, see the PAL Handbook. This section also contains helpful programming information and a complete listing of approved programmers. Testing considerations for programmable logic are discussed. Includes new material on design considerations for high-speed bipolar and CMOS logic.

7. Quality and Reliability
Includes information on AMD PLD process technologies and quality procedures.

8. Appendices
Quick reference information, including replacements for PLDs no longer in this data book.

Call your local AMD sales office, listed at the back, for updated information on these products and the latest new products. If you have any questions or comments on PLDs or any other products, please contact your local AMD sales office or call the AMD Applications Hotline at (800) 222-9323.

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Table of Contents

Introduction

PAL Device Data Sheets

Sequencer Data Sheets

Programmable Logic Sequencers

Field-Programmable Controllers

Programmable Event Generator

ECL/PGA Data Sheets

ECL PAL Devices

Programmable Gate Array (PGA)

General Information

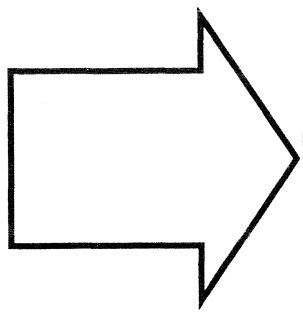
Design and Programming

Quality and Reliability

Appendices

CMOS Table of Contents

Alphanumeric Product Index



Introduction

Introduction

The Programmable Array Logic device, commonly known as the PAL® device, was invented at Monolithic Memories, now a part of Advanced Micro Devices, over 14 years ago. The concept for this revolutionary type of device sprang forth as a simple solution to the shortcomings of discrete TTL logic.

The successfully proven PROM technology which allowed the end user to "write on silicon" provided the technological basis which made this kind of device not only possible, but very popular as well.

The availability of design software made it much easier to design with programmable logic. As designers were freed from the drudgery of low-level implementation issues, new complex designs were easier to implement, and could be completed more quickly.

This chapter outlines some basic information essential to those who are unfamiliar with Programmable Logic devices (PLDs). The information may also be useful to those who are current users of programmable logic. The specific issues which need to be addressed are:

- What is a PLD?
- What other implementations are possible?
- What advantages do PLDs have over other implementations?

WHAT IS A PLD?

In general, a programmable logic device is a circuit which can be configured by the user to perform a logic function. Most "standard" PLDs consist of an AND array followed by an OR array, either (or both) of which is programmable. Inputs are fed into the AND array, which performs the desired AND functions and generates product terms. The product terms are then fed into the OR array. In the OR array, the outputs of the various product terms are combined to produce the desired outputs. There are three fundamental types of standard PLD: the PROM, the PAL device, and the PLS device.

PROMs

PROMs are usually thought of as memory elements. However, the PROM has a fixed AND array (which decodes the memory address) followed by a programmable OR array (Figure 1). For each of a given set of input combinations (addresses), it generates a value which has been programmed into the device.

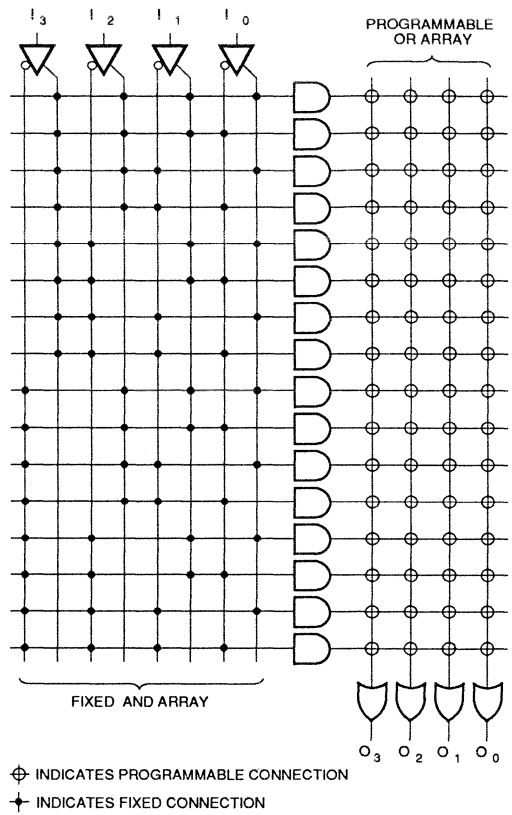


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Figure 1. PROM Array Structure

PAL Devices

The PAL device has a programmable AND array followed by a fixed OR array (Figure 2). The fact that the AND array is programmable makes it possible for the devices to have many inputs. The fact that the OR array is fixed makes the devices small (which means less expensive) and fast.

PLS Devices

The PLS (Programmable Logic-based Sequencer) devices are based on the standard PLA architecture (Figure 3), where both the AND and the OR arrays are programmable. This arrangement allows for greater overall flexibility. The architecture is a bit more costly in terms of die size and speed, so for simple logic functions, a PAL device is usually more cost effective. However, this architecture is very effective for sequencers, where the flexibility allows larger state machines than might fit in a PAL device.

Other PLDs

In addition to the basic sum-of-products PLDs, some more complex PLDs dedicated to sequencing are available, most notably the Am29CPL151 and the Am29CPL154. Their architectures are described elsewhere in the data book, but their fundamental benefits are the same as those of the more traditional PLDs.

In practice, the distinctions between architectures are not as significant as the differences between the types of functions to be performed.

WHAT OTHER IMPLEMENTATIONS ARE POSSIBLE?

There are essentially four alternatives to programmable logic:

- Discrete Logic
- Gate Arrays
- Standard Cell Circuits
- Full Custom Circuits

Discrete Logic

Discrete logic, or conventional TTL logic, has the advantage of familiarity; hence its popularity. It is also quite inexpensive when only unit cost is considered. The drawback is that the implementation of even a simple portion of a system may require many units of discrete logic. There are "hidden" costs associated with each unit that goes into a system, which can render the overall system more expensive.

Designing with discrete chips can also be very tedious. Each design decision directly affects the layout of the board. Changes are difficult to make. The design is also more difficult to document,

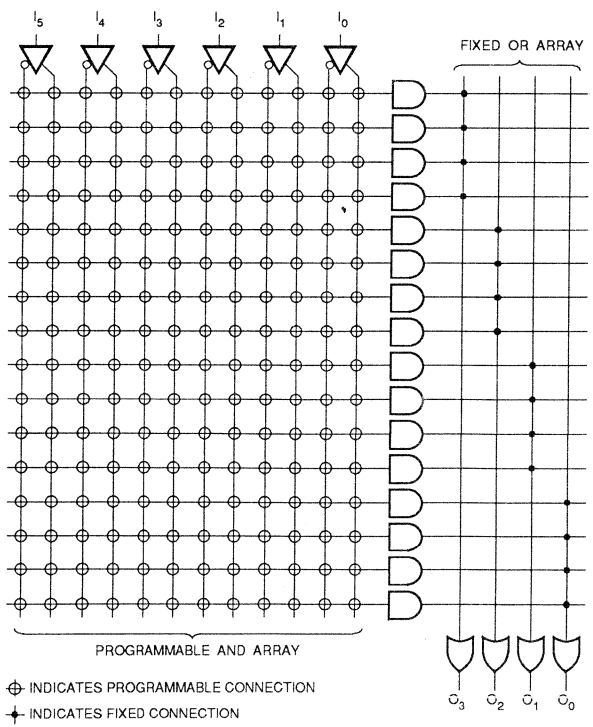

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Figure 2. PAL Device Array Structure

making it harder to debug and maintain later. These items all contribute to a long design cycle when discrete chips are used extensively.

Gate Arrays

Gate arrays have been increasing in popularity. The attractiveness of this solution lies in the device's flexibility. By packing the functions into the device, a great majority of the available silicon is actually used. Since such a device is customized for an application, it would seem to be the optimum device for that application.

However, one also pays substantial development costs, especially in the case of a design which needs changes after silicon has already been processed. Even though the unit costs are generally quite low for gate arrays, the volumes required to make their use worthwhile excludes them as a solution for many designers. This fact, added to the long design cycle and high risk involved, make this solution practical for only a limited number of designers.

Standard Cell Circuits

Standard cell circuits are quite similar to gate arrays, their main advantage being that they consist of a collection of different parts of circuits which have already been debugged. These circuits are then assembled and collected to perform the desired functions. This can ideally lead to reduced turnaround from conception to implementation, and a much more efficient circuit.

The drawback is that even though the individual components of the circuit have been laid out, a complete layout must still be performed to arrange the cells. Instead of just customizing the metal interconnections, as is done in a gate array, the circuit must be developed from the bottom up. Development costs can be even higher than for gate arrays, and despite the standard cell concept, turnaround time often tends to be longer than planned. Again, the volume must be sufficiently high to warrant the development costs.

Full Custom Circuits

Full custom designs require that a specific chip be designed from scratch to perform the needed functions. The intent is to provide a solution which gives the designer exactly what is needed for the application in question; no more and no less. Ideally, not a square micron of silicon is wasted. This normally results in the smallest piece of silicon possible to fit the needs of the design, which in turn reduces the system cost. Understandably, though, development costs and risks for such a design are extremely high, and volumes must be commensurately high in order for such a solution to be of value.

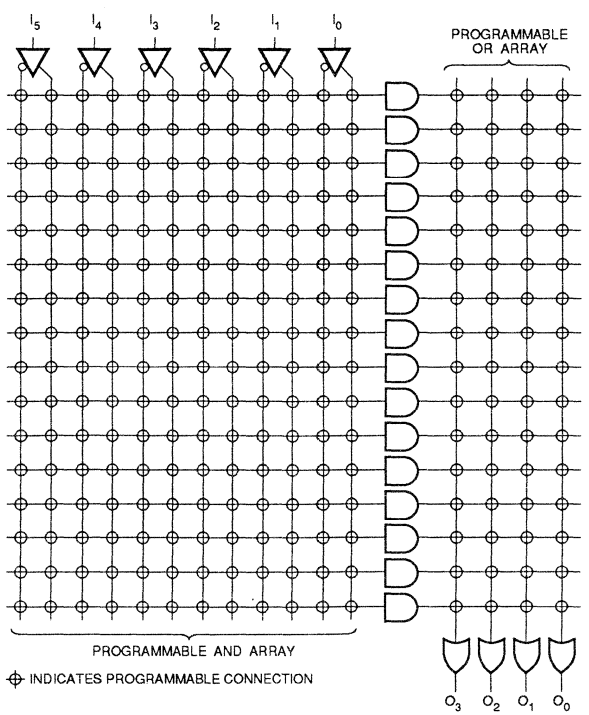

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Figure 3. PLA Array Architecture

WHAT ADVANTAGES DO PLDS HAVE OVER OTHER IMPLEMENTATIONS?

As user-programmable semicustom circuits, PLDs provide a valuable compromise which combines many of the benefits of discrete logic with many of the benefits of other semicustom circuits. The overall advantages can be found in several areas:

- Ease of design
- Performance
- Reliability
- Cost savings

Ease of Design

The support tools available for use in designing with PLDs greatly simplify the design process by making the lower-level implementation details transparent. In a matter of one or two hours, a first time PLD user can learn to design with a PAL device, program it, and implement the design in a system.

The design support tools consist of design software and a programmer. The design software is used in generating the design; the programmer is used to configure the device. The software provides the link between the higher-level design and the low-level programming details.

All of the available design software packages (of which Advanced Micro Devices' PALASM® software is the most widely used) perform essentially the same tasks. The design is specified with relatively high-level constructs; the software takes the design and converts it into a form which the programmer uses to configure the PLD. Most software packages provide logic simulation, which allows one to debug the design before actually programming a device. The high-level design file also serves as documentation of the design. This documentation can be even easier to understand than traditional schematics.

Depending on the capabilities desired, a device programmer can cost anywhere from under $1,000.00 to around $15,000.00 for a high-volume production programmer. Many PLD users do not find it necessary to purchase a programmer; it is often quite cost effective and convenient to have either the manufacturer or an outside distributor do the programming for them. For design and prototyping, though, it is very helpful to have a programmer; this allows one to implement designs immediately.

The convenience of programmable logic lies in the ability to customize a standard, off-the-shelf product. PLDs can be found in stock to suit a wide range of speed and power requirements. The variety of architectures available also allows a choice of the proper functionality for the application at hand. Thus a design can be implemented using a standard device, with the end result essentially being a custom device. If a design change is needed, it is a simple matter to edit the original design and then program a new device, or, in the case of reprogrammable CMOS devices, erase and reprogram the old device.

Board layout is vastly simplified with the use of programmable logic. PLDs offer great flexibility in the location of inputs and outputs on the device. Since larger functions are implemented inside the PLD, board layout can begin once the inputs and outputs are known. The details of what will actually be inside the PLD can be worked out independently of the layout. In many cases, any needed design changes can be taken care of entirely within the PLD, and will not affect the PC board.

Performance

Speed is one of the main reasons that designers use PAL devices. The TTL PAL devices presently on the market can provide better performance than the fastest discrete logic available. ECL PAL devices extend the benefits of programmable logic to the even higher-speed realm of ECL logic. Today's fastest PAL devices are being developed on the newest technologies to gain every extra nanosecond of performance.

Performance cannot come strictly at the expense of power consumption. Since PLDs can be used to replace several discrete circuits, the power consumption of a PLD may well be less than that of the combined discrete devices. As more PLDs are developed in CMOS technology, the option for even lower power becomes available, including zero standby power devices for systems which can tolerate only minute standby power consumption.

Reliability

Reliability is an area of increasing concern. As systems get larger and more complex, the increase in the amount of circuitry tends to reduce the reliability of the system; there are "more things to go wrong". Thus a solution which inherently reduces the number of chips in the system will contribute to higher reliability. A programmable logic approach can provide device quality levels up to 50 parts per million (ppm), while also providing a more reliable solution due to the smaller number of devices required.

With the reduction in units and board space, PC boards can be laid out less densely, which greatly improves the reliability of the board itself. This also reduces crosstalk and other potential sources of noise, making the operation of the system cleaner and more reliable.

Cost

For any design approach to be practical, it must be cost effective. Cost is almost always a factor in considering a new design or a design change. But the calculation of total system cost can be misleading if not all aspects are considered. Many of the costs

	Unit Cost Range	NREs/ Development Costs	Purchase Volume For Best Economics	Design Flexibility	Gate Count per Device	Engineering Design Time	Design Turnaround Time	Cost of Each Design Change
PLDs: BLANK	Low–Med	None	5K–200K	Med	200–2K	1/2 Week	Short (1–10 Days)	Very Low
PLDs: FACTORY PROGRAMMED	Low–Med	Low	10K–200K	Med	200–2K	3–10 Weeks	Moderate (8–10 Wks.)	Med
DISCRETE LOGIC	Low–Med	None	1K–10K	Low	10–30	1 Week	Short (1–10 Days)	Med
GATE ARRAYS	Low	Med–High	10K–200K	Med–High	1K–10K	12–40 Weeks	Long (3–9 Mos.)	High
STANDARD CELLS	Low	High	100K–300K	Med–High	1K–10K	26–52 Weeks	Long (6–12 Mos.)	High
FULL CUSTOM	Very Low	High	200K and Up	High	1K–60K	1–2 Yrs.	Long (6–12 Mos.)	High

Figure 4. Cost and Design-time Comparisons

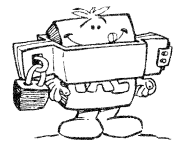
can be elusive or difficult to measure. For example, it is difficult to quantify the cost of market share lost due to late product introduction.

The greatest savings over a discrete design are derived from the fact that a single PLD can replace several discrete chips. Board space requirements can drop by 25% or more when PLDs are used. Figure 4 illustrates some of the costs of the various solutions discussed so far, with many of the factors that may not always be considered included for comparison. These involve such items as inventory costs, inspection costs, test costs, board materials costs, and of course the very costly time spent designing and debugging such systems, and isolating and replacing units which fail. With each design change, the cost of a custom solution rises dramatically, while that of a user-customizable approach is minimal. The relationship between the various alternatives is summarized in Figure 5.

Another economic benefit of the use of PLDs is that when one PAL device is used in several different designs, as is often the case, the user has not committed that device to any one of the particular designs until the device has been programmed. This means that inventory can be stocked for several different designs in the form of one device. As requirements change, the parts can be programmed to fit the need. And in the case of reprogrammable CMOS devices, one is not committed even after programming.

There is also a cost-effective PLD solution for high-volume production. Just as a ROM is a PROM which has been hard-wired for mass production, HAL® (Hard Array Logic) devices can be produced in high volumes for extra cost savings. This mask-programmed version can be produced in high volume with unparalleled quality. In addition, in the event that production quantities for your system show an unexpected increase, the equivalent PAL or ProPAL™ devices (in-factory programmed PAL devices) can be quickly obtained and programmed in your factory, by Advanced Micro Devices, or through distribution to cover the temporary shortage. More details on HAL and ProPAL devices are provided later in the Data Book.

One final subtle cost issue is derived from the ease with which a competitor can copy a design. PLDs have a unique feature called a security fuse, whose purpose is to protect a design from being copied. By using secured PLDs extensively in a system, one can safely avoid having one's system easily deciphered. The added design security provided by this feature can buy extra market time, forcing competitors to do their own original design work rather than copying the designs of others.



SUMMARY

Programmable logic provides the means of creating semi-custom designs with readily available standard components. There is a wide variety of PLDs; PAL devices are most widely used, and perform well for basic logic and some sequencing functions. Other dedicated sequencers provide the circuitry required to implement more complex designs.

By assuming some of the attributes of gate arrays, programmable logic provides the cost savings of any other semicustom device, without the extra engineering costs, risks, and design delays. Reliability is also enhanced as quality increases and board complexity decreases.

The design tasks are greatly simplified due to the design tools which are now available. Design software and device programmers allow top-down high-level designs, with a minimum of time spent on actual implementation issues. Simulation allows some design debug before a device is programmed.

For all of these reasons, programmable logic has become, and will continue to be, the design methodology of choice among digital systems designers.

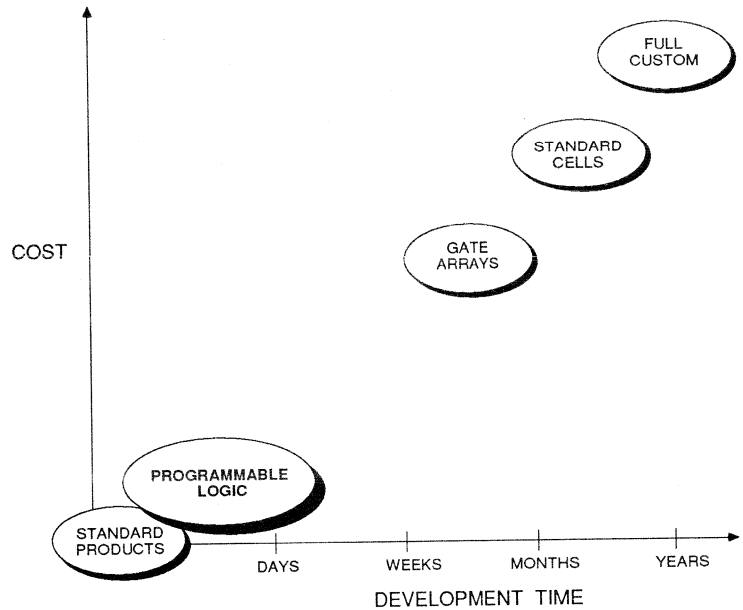


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Figure 5. Development Cost vs. Time for Alternative Logic Implementations

Advanced Micro Devices offers the industry's widest variety of PLDs, implemented in a variety of technologies. In this section, we will briefly discuss the device families, and look at the various architecture, speed, and power options. More specific device information can be found in the individual data sheets in sections 2–4. Discussions on some of the special architectural features of many of the devices can also be found in their respective data sheets.

There are six basic PLD areas addressed by Advanced Micro Devices' PLDs:

- High-speed PAL® devices
- Universal PAL devices
- Industry-standard PAL devices
- Low-power PAL devices
- Special architecture PLDs
- Programmable gate arrays

The largest application area is that covered by the PAL devices. There is a wide variety of PAL devices, ranging from simple devices that address general logic design problems to more sophisticated devices that deal with more complex problems.

Within the group of special architecture PLDs, there is also a series of sequencers that are not PAL devices, featuring architectures particularly well suited to sequencing operations. While there are PAL devices that work well as state machines in addition to their other applications, these dedicated sequencers have given up some of their generality to provide optimal state machine solutions.

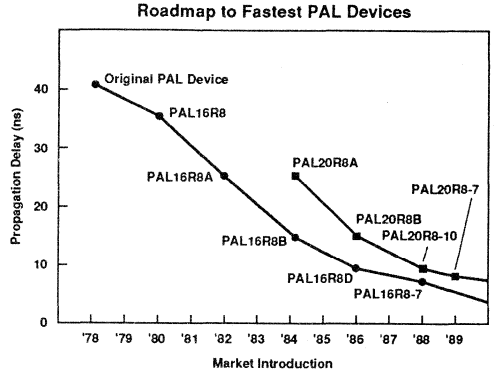
The final area, that of high-density design, is addressed by the programmable gate arrays (PGAs) which provide a PLD with thousands of gates. The PGAs are described briefly in this data book; for more detail, please refer to the PGA Handbook.

Design software radically simplifies the design of any circuit in a PLD. PALASM® software can be used for all PAL and PLS devices. PLD design software is discussed briefly in section 5.

HIGH-SPEED PAL DEVICES

AMD offers the fastest PAL devices on the market today. We were the first to introduce the 40-ns PAL device in 1978 and have been the first to market on all five successive generations. In the last decade, we have improved the performance of PAL devices almost six-fold. As the market leader in the PLD arena, we fully expect to introduce even faster devices in the future.

Roadmap to Fastest PAL Devices



Currently, we have the bipolar TTL PAL16R8 family of 20-pin devices in 7.5-ns speed grade and the PAL20R8 family of 24-pin devices, also in 7.5-ns speed grade, available in volume production. These families include both registered (16R4, 16R6, 16R8, 20R4, 20R6, 20R8) and combinational devices (16L8, 20L8). They are used in a wide variety of applications where performance and space are critical, often replacing FAST™ and AS SSI/MSI logic circuits. For applications where the absolute fastest devices are not needed, other speed grades are offered at a lower cost and/or lower power consumption.

AMD's new EE CMOS process also provides high-speed universal PAL devices. The PALCE16V8 has a 10-ns version; most other EE CMOS devices have a 15-ns t_{PD}, while using half or even a quarter of the power required by their bipolar equivalents.

For exceptionally high performance, AMD offers ECL in addition to bipolar TTL PAL devices. AMD's ECL PAL devices are the 24-pin PAL10H/10020EV8 and PAL10H/10020EG8. These are the industry's first ECL PAL devices with output logic macrocells, a variable product term distribution and other advanced features. They support state-machine applications running at 125 MHz and are available in both 10KH and 100K ECL logic level versions. Even higher performance ECL PAL devices will be available in the future.

High-Speed PAL Devices

Part Number	Functional Description							Commercial Specifications			
	Pin Count	ARRAY INPUTS			ARRAY OUTPUTS			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16L8	20	6	10	—	—	8	—	7	–7	7.5	74	180
PAL16R8		—	8	8	8	—	—	8				
PAL16R6		2	8	6	6	2	—	7–8	D	10	58.8	180
PAL16R4		4	8	4	4	4	—	7–8				
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	H–10**	10	55.5	90
									Q–15	15	45.5	55
									H–15	15	45.5	90
PAL20L8	24	6	14	—	—	8	—	7	–7	7.5	74	210
PAL20R8		—	12	8	8	—	—	8				
PAL20R6		2	12	6	6	2	—	7–8	–10	10	55.5	210
PAL20R4		4	12	4	4	4	—	7–8				
PALCE20V8	24	0–8	12–14	8–0	—	—	8	7–8	H–15	15	45.5	90
PAL24L10**	28	8	16	—	—	10	—	7	–10	10	55.5	210
PAL24R10**		—	14	10	10	—	—	8				
PAL24R8**		2	14	8	8	2	—	7–8				
PAL24R4**		6	14	4	4	6	—	7–8				
PALCE24V10**	28	0–10	14–16	10–0	—	—	10	7–8	H–15	15	45.5	90
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	H–15	15	50	90
PAL22V10	24	0–10	12	10–0	—	—	10	8–16	–10**	10	71	180
									–15	15	50	210
PALCE610**	24	0–16	4	16–0	—	—	16	8	H–15	15	45.5	90
PAL10H20EV8	24	0–8	12	8–0	—	—	8	8, 12	–6	6	125	260
PAL10020EV8	24	0–8	12	8–0	—	—	8	8, 12	–6	6	125	285
PAL10H20EG8	24	0–8	12	8–0	—	—	8***	8, 12	–6	6	—	260
PAL10020EG8	24	0–8	12	8–0	—	—	8***	8, 12	–6	6	—	285

* f_{MAX} is defined as $1/(t_s + t_{co})$ for the external feedback
** in development
*** latched

UNIVERSAL PAL DEVICES

Have your design needs included a non-standard mix of inputs and outputs or choosing a variable number of combinatorial/registered/latched inputs and/or outputs for the given application? How about stocking only one or two PLDs to reduce your inventory costs?

The solution to your problem is AMD's family of universal PAL devices. We pioneered the concept of user-programmable output logic macrocells with the PAL22V10. With this macrocell, you can configure an output for combinatorial or registered operation and active-low or active-high polarity. This is what makes the PAL22V10 universal, for it can substitute for virtually all of the standard 24-pin PAL devices on the market. The PALCE26V12 is a 28-pin version which provides more inputs and outputs for those designs that don't quite fit into a PAL22V10.

But we did not stop there. A second new feature pioneered with the PAL22V10 is variable product term distribution; the 10 outputs on this device are arranged in pairs with 16, 14, 12, 10 or eight product terms on each output. With

up to 16 product terms, the PAL22V10 can implement far more complex logic functions than can be supported by other 24-pin devices. No wonder the PAL22V10 is the most popular PAL device on the market today. And now both faster (15 ns, 50 MHz) and reprogrammable low-power CMOS (15, 25 ns; 55, 90 mA) versions are available from AMD.

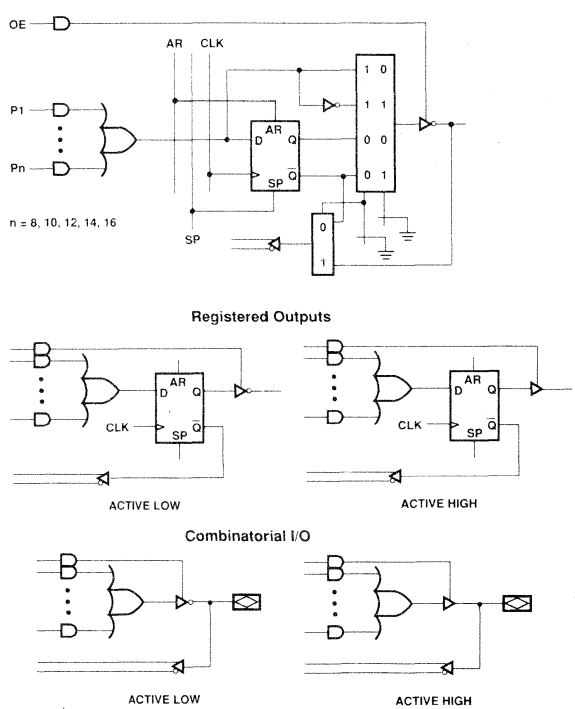
The PALCE16V8, PALCE20V8, and PALCE24V10 are EE CMOS universal devices that have the additional capability of directly taking the designs of standard 20-, 24-, and 28-pin PAL devices, respectively. They provide a cost-effective means of reducing inventory, lowering power, and reducing risk.

The PALCE610 adds to the basic macrocell by providing 16 I/O macrocells that can be configured with D, T, J-K, or S-R flip-flops.

The PALCE29M16 further enhances the macrocell concept. Its macrocell can be an input or an output macrocell that can be configured three ways: combinatorial, latched or registered. Sixteen of these macrocells are available in a 24-pin 300-mil package. And eight of the macrocells can be buried, allowing the connecting pins to be used as dedicated inputs. The PALCE29M16 also offers variable product term distribution.

For those applications where registers and latches are not needed, the AmPAL18P8 (20-pin) and AmPAL22P10 (24-pin) are perfect. These PAL devices with programmable polarity can flexibly replace almost all standard 20- and 24-pin combinatorial PAL devices. As a result, they significantly reduce your inventory. They are available in several speed-power grades to meet most application requirements.

PAL22V10 Logic Macrocell



The output logic macrocell makes the PAL22V10 universal, for it can substitute for virtually all of the standard 24-pin PAL devices on the market.

Universal PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	ARRAY INPUTS			ARRAY OUTPUTS			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	H–10**	10	55.5	90
									Q–15	15	45.5	55
									H–15	15	45.5	90
									Q–25	25	37	55
									H–25	25	37	90
									Z–20**	20	40	0.1
PALCE20V8	24	0–8	12–14	8–0	—	—	8	7–8	H–15	15	45.5	90
									H–25	25	37	90
PALCE24V10**	28	0–10	14–16	10–0	—	—	10	7–8	H–15	15	45.5	90
									H–25	25	37	90
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	H–15	15	50	90
									Q–25	25	33.3	55
									H–25	25	33.3	90
									Z–25**	25	33.3	0.1
PAL22V10	24	0–10	12	10–0	—	—	10	8–16	–10**	10	71	180
									–15	15	50	210
PALCE26V12	28	0–12	14	12–0	—	—	12	8–16	H–20	20	40	105
									H–25	25	33.3	105
PALCE610**	24	0–16	4	16–0	—	—	16	8	H–15	15	45.5	90
									H–25	25	37	90
PALCE29M16	24	8–16	5	16–8	—	—	16	8–16	H–25	25	28.5	120
									H–35	35	20	120
AmPAL18P8	20	8	10	—	—	8	—	8	B	15	—	180
									A	25	—	180
									AL	25	—	90
AmPAL22P10	24	10	12	—	—	10	—	8	B	15	—	210
									A	25	—	210
									AL	25	—	105

* f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback
** in development

1

Standard PAL Devices

Part Number	Functional Description							Commercial Specifications			
	Pin Count	ARRAY INPUTS			ARRAY OUTPUTS			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16L8	20	6	10	—	—	8	—	7	H–15	15	37	90
									B	15	37	180
PAL16R8		—	8	8	8	—	—	8	B–2	25	25	90
									A	25	25	180
PAL16R6		2	8	6	6	2	—	7–8	B–4	35	16	55
PAL16R4		4	8	4	4	4	—	7–8	A–2	35	18	90
PAL20L8	24	6	14	—	—	8	—	7	B	15	37	210
									B–2	25	25	105
PAL20R8		—	12	8	8	—	—	8	A	25	25	210
									A–2	35	16	105
PAL20R6		2	12	6	6	2	—	7–8	B–2	25	25	105
PAL20R4		4	12	4	4	4	—	7–8				
									B	15	—	210
AmPAL20L10	24	8	12	—	—	10	—	3	–20	20	—	165
									AL	25	—	105
PAL20L10	24	8	12	—	—	10	—	3	A	30	—	165
PAL20X10		—	10	10	10	—	—	4				
PAL20X8	24	2	10	8	8	2	—	3–4	A	30	22.2	180
PAL20X4		6	10	4	4	6	—	3–4				

* f_{MAX} is defined as $1/(t_s + t_{co})$ for the external feedback

INDUSTRY-STANDARD PAL DEVICES

As we have increased speed on the TTL PAL devices, we have also reduced the power consumption on the slower devices by as much as 75 percent. As a result, both the industry-standard 20-pin and 24-pin PAL device families are available in a variety of speed and power grades. This allows the designer to select the optimum performance at the lowest possible cost and power consumption. These 20- and 24-pin devices are used in applications where the advantages of reduced package count, such as higher reliability and lower power consumption, improve the overall price-performance of the end-product. Often these benefits are realized by replacing Schottky, ALS, LS and some CMOS SSI/MSI logic circuits with these PAL devices.

Low-Power PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	ARRAY INPUTS			ARRAY OUTPUTS			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	Z-20**	20	40	0.1
									Q-15	15	45.5	55
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	Z-25**	25	33.3	0.1
									Q-25	25	33.3	90

* f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback
** in development

LOW-POWER PAL DEVICES

AMD is the only major supplier of programmable logic devices to offer a broad line of low-power CMOS devices. And we are the only PLD supplier with such a comprehensive CMOS programmable logic line.

There are two basic types of CMOS PAL devices: those that dissipate essentially no power when in a quiescent state, and faster devices which draw nominal current even when quiescent. Devices are thus classified as "zero-power" or "low-power."

Zero-power PAL devices are particularly suited for products that are portable or battery operated. In a standby mode they consume less than 100 µA supply current. Low-power CMOS devices can cut system power consumption 50 percent by replacing equivalent 25-ns and 35-ns speed TTL PAL devices. In addition, these devices can also save significant board space by replacing several CMOS SSI/MSI devices from families such as FACT™, ACL, MC14000, etc. By consolidating several SSI/MSI packages into a single CMOS PAL device, the power consumption can be cut even further.

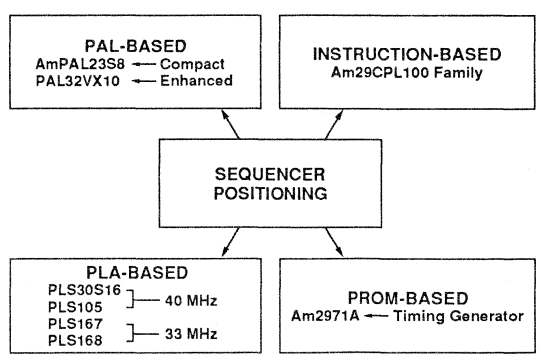
SPECIAL ARCHITECTURE PLDs

AMD offers a wide variety of programmable logic devices which have been enhanced architecturally to provide a high level of integration and performance. They include a family of sequencers optimized for state-machine applications, and asynchronous devices which have been designed to implement asynchronous design functions optimally. These products offer you unprecedented flexibility in selecting the right PLD for the application at hand.

Programmable Logic Sequencers

AMD's programmable logic sequencer family gives you high speed, functionality and a wide selection. Several devices are available in several speed-power grades so you can choose the appropriate one for your application. Four types of sequencers are offered: PAL-based, PLA (Programmable Logic Array)-based, PROM-based and instruction-based. Each has its own benefits, but together they offer you the choice of using a familiar and comfortable architecture.

The PAL-based AmPAL23S8 is a compact sequencer device that packs 14 registers into a space-saving 20-pin 300-mil DIP. With a 20-ns propagation delay and 33-MHz external/40-MHz internal cycle time, it is ideal for high-performance applications where board real estate is valuable. The PAL32VX10 offers all the benefits of the industry-standard PAL22V10 plus J-K flip-flops and the ability to bury its 10 registers, freeing valuable I/O pins.



The PLA-based family consists of the PLS105, PLS167, PLS168, and PLS30S16. The PLS105 and PLS30S16 run at a blazing 40 MHz and are available in a 28-pin 300-mil DIP. The PLS167/168 operate at 33 MHz but consume only 160 mA of supply current. The PLS105/167/168 come with six buried registers and 48 logical product terms which can be shared between all outputs and the buried registers. The PLS30S16 has up to 12 buried registers, allows combinatorial outputs, has 64 product terms, and allows registered inputs.

The Am2971A PEG™ (Programmable Event Generator) is a PROM-based, 100-MHz, general-purpose, user-programmable waveform generator. With 12 independent, registered, programmable outputs, it can be applied to a host of useful timing applications including general state machines.

The instruction-based family of sequencers consists of two members. They are single-chip, field-programmable controllers that can implement state machines and controllers by programming the appropriate sequence of instructions. With complete high-level software support, these devices are as easy to use as microprocessors. The Am29CPL151 operates at a maximum of 33 MHz. The Am29CPL154 offers a very deep PROM (512 words) so that larger state machines can be implemented. Both devices are manufactured in 28-pin, 300-mil packages.

A powerful instruction-set makes the Am29CPL100 family easy to use. Instruction types include conditional branching, looping and subroutine call. Each line of code in an Am29CPL100 program typically corresponds to one state in a state machine diagram. Program code is easy to write because it closely mimics the way the human mind logically thinks about control problems. Also, the number of lines of program code required to implement an application is significantly reduced in comparison to conventional Boolean equation-based approaches. This means more efficient use of program memory, faster design entry and debugging, and faster algorithm execution.

Finally, if you are looking for the fastest device to implement your state-machine application, consider our 74-MHz standard 20- and 24-pin registered devices (PAL16R4/R6/R8-7, PAL20R4/R6/R8-7). Although not optimized for state machine applications, they are the fastest available TTL logic and can easily be adapted as state machines.

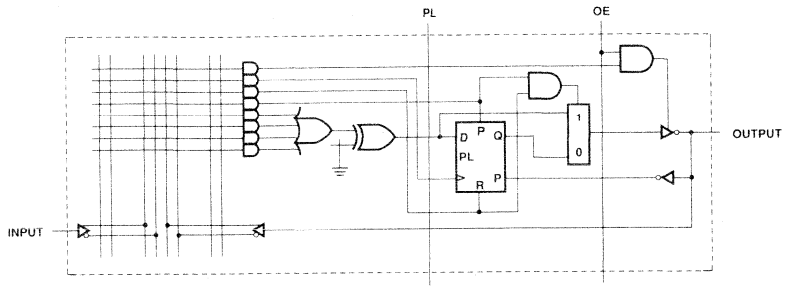
So there you have it—a wide selection of programmable logic sequencers to meet your application needs. And only AMD offers a complete solution.

Sequencer Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	ARRAY INPUTS			ARRAY OUTPUTS			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
AmPAL23S8	20	4–8	9	6–10	4	—	4	6–12	–20	20	33	210
									–25	25	28.5	210
PAL32VX10	24	10	12	10	—	—	10	8–16	A	25	25	180
									STD	30	22.2	180
PLS105	28	—	16	6	8	—	—	0–48	–40	—	40	200
PLSCE105	28	—	16	6	8	—	—	0–48	H–37**	—	37	100
PLS167	24	—	14	8	6	—	—	0–48	–33	—	33	160
PLSCE167	24	—	14	8	6	—	—	0–48	H–33**	—	33	80
PLS168	24	—	12	10	8	—	—	0–48	–33	—	33	160
PLSCE168	24	—	12	10	8	—	—	0–48	H–33**	—	33	80
PLS30S16	28	0–4	12–13	12	4	—	8	0–64	–40	20	40	225
Am2971	24	—	3	—	12	1	—	—	A	—	100	425
Am29CPL151	28	—	7	16	16	—	—	—	–33	—	33	115
Am29CPL154**	28	—	8	20	16	—	—	—	–30	—	30	115

*f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback
** in development

PAL20RA10
RA Cell Configuration



Asynchronous PAL Devices

Currently AMD makes six devices that are function-specific. They support asynchronous and bus interface applications. We expect to expand our offering to encompass even more functions over the next few years.

The 24-pin PAL20RA10 and its 20-pin counterpart, PAL16RA8, are optimized for asynchronous applications. They contain ten and eight D-type flip-flops, respectively, driven by a PAL array. Each flip-flop has individually programmable Clock, Reset and Preset product terms. In addition, programmable polarity is offered on each output. With such features, these devices are well suited to replacing glue logic in your system. Also, we now have available a faster (20 ns, 30 MHz) version of the PAL20RA10 for high-speed applications.

The CMOS PALCE29MA16 combines some of the advantages of the PALCE29M16 with the advantages of the PAL20RA10. It has one dedicated Clock/Latch Enable input as well as product terms for each of the 16 macrocells to allow individual clocking, asynchronous Reset and asynchronous Preset. It also features variable product term distribution. To top it off, the PALCE29MA16 is electrically reprogrammable in a plastic 300-mil package.

The PAL22IP6 Interface Protocol Asynchronous Cell (IPAC) offers a unique patented architecture, which makes it ideal for implementing bus-interface protocol applications, self-timed circuits and asynchronous state-machine designs. It is a 24-pin device with six high-drive (48 mA and 64 mA) output macrocells.

These macrocells contain totally new logic storage elements. The logic storage elements are edge-activated flips-flops which do not require a separate clock for storing data signals. Instead the signals are stored in the flip-flops in direct response to their rising or falling edges. This provides a convenient way of implementing asynchronous handshake protocols. Please refer to the device data sheet for more information.

Asynchronous PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	ARRAY INPUTS			ARRAY OUTPUTS			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16RA8	20	8	8	—	—	—	8	4	STD	30/35**	20	170
PAL20RA10	24	10	10	—	—	—	10	4	–20	20	30	200
									STD	30/35**	20	200
PALCE29MA16	24	8–16	5	16–8	—	—	16	4–12	–25	25	28.5	120
									–35	35	20	120
PAL22IP6	24	6	16	—	—	—	6	9	–25	25	—	210

*f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback
**polarity fuse programmed (active-high)

PROGRAMMABLE GATE ARRAYS

The Programmable Gate Array (PGA) is the first device to successfully bridge the gap between field-programmable logic and gate arrays. The PGA effectively combines the benefits of low-power CMOS LSI technology and the advantages of user programmability with the gate density and logic flexibility previously obtainable only with gate arrays.

The PGA provides a quantum jump in field-programmable logic device capability extending its usable functional density into a realm beyond that of more conventional programmable logic devices. Much greater density is achieved with the PGA by use of a flexible array-type architecture more versatile than that of conventional PLDs, which are increasingly inefficient as gate density is increased. The AMD Am2018 1800-gate PGA device can replace as many as six 1200-gate PLD devices in some applications.

Gate arrays, on the other hand, may provide densities higher than those of current PGAs. However, gate arrays typically require longer development times, design risks and higher development cost.

The PGA is the ideal option for the PLD designer wishing to achieve a new level of system functional density and for the gate array user looking for a low-cost, low-risk, and easy-to-use alternative which provides instant prototyping through the power of in-system verification.

Programmable Gate Arrays

Part Number	Speed Grade	Package	Description
Am2064-100 Am2064-70 Am2064-50	100 70 50	28J, 48P, 68J, 68G	8 x 8 Logic Cell Array —1200 gates
Am2018-100 Am2018-70 Am2018-50	100 70 50	44J, 68J, 84J, 68G, 84G	10 x 10 Logic Cell Array —1800 gates
Am3020-100 Am3020-70 Am3020-50	100 70 50	68J, 84J	8 x 8 Logic Cell Array —2000 gates
Am3030-100 Am3030-70 Am3030-50	100 70 50	84J, 84G	10 x 10 Logic Cell Array— 3000 gates
Am3042-100 Am3042-70 Am3042-50	100 70 50	84J, 84G, 132G	12 x 12 Logic Cell Array—4200 gates
Am3064-100* Am3064-70* Am3064-50*	100 70 50	132G	14 x 16 Logic Cell Array—6400 gates
Am3090-100 Am3090-70 Am3090-50	100 70 50	175G	16 x 20 Logic Cell Array —9000 gates
Am1736		8-Pin Mini DIP, 20 PLCC	36K Serial EPROM
Am1765		8-Pin Mini DIP, 20 PLCC	65K Serial EPROM

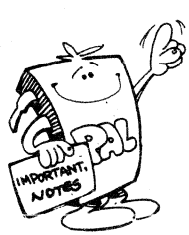
Notes: Package Types — P = Plastic DIP; J = Plastic Leaded Chip Carrier; G = Pin Grid Array

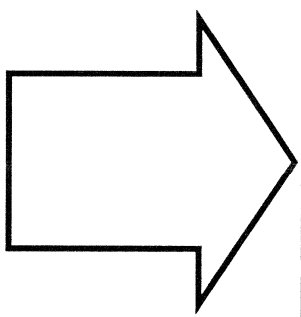
* in development

Development Software Support for PGAs

Part Number	Description
AmPGA151*	PGA Bundled Development System
AmPGA251*	PGA Bundled Development System with Simulation
AmPGA051	FPGA Design System
AmPGA351	FPGA Development System
AmPGA451	FPGA Development System with Simulation
AmPGA434	FPGA Design System with Mentor Interface and Libraries
AmPGA081	Programmer for Serial Configuration PROM

*These will be replaced by AmPGA351 and AmPGA451.


IMPORTANT
NOTES



PAL Device Data Sheets

Alphanumeric Product Index

PAL® Device/ Sequencer/FPGA Menu

Standard PAL Devices

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
16R8	PAL16L8-7 PAL16R8-7 PAL16R6-7 PAL16R4-7	20P,D,J	TTL	10 8 8 8	6 Comb - 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	7.5	74	180
	PAL16L8D PAL16R8D PAL16R6D PAL16R4D	20N,J,NL	TTL					10	58.8	180
	PAL16L8H-15 PAL16R8H-15 PAL16R6H-15 PAL16R4H-15	20P,D,J	TTL					15	37	100
	PAL16L8B PAL16R8B PAL16R6B PAL16R4B	20N,J,NL	TTL					15	37	180
	PAL16L8B-2 PAL16R8B-2 PAL16R6B-2 PAL16R4B-2	20N,J,NL	TTL					25	25	90
	PAL16L8A PAL16R8A PAL16R6A PAL16R4A	20N,J,NL	TTL					25	25	155 180 180 180
	PAL16L8B-4 PAL16R8B-4 PAL16R6B-4 PAL16R4B-4	20N,J,NL	TTL					35	16	55
	PAL16L8A-2 PAL16R8A-2 PAL16R6A-2 PAL16R4A-2	20N,J,NL	TTL					35	18	80 90 90 90
20R8	PAL20L8-7 PAL20R8-7 PAL20R6-7 PAL20R4-7	24P,D,28J	TTL	14 12 12 12	6 Comb - 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	7.5	74	210
	PAL20L8-10 PAL20R8-10 PAL20R6-10 PAL20R4-10	24P,D,28J	TTL					10	55.5	210
	PAL20L8B PAL20R8B PAL20R6B PAL20R4B	24NS,JS, 28NL	TTL					15	37	210
	PAL20L8B-2 PAL20R8B-2 PAL20R6B-2 PAL20R4B-2	24NS,JS, 28FN	TTL					25	25	105
	PAL20L8A PAL20R8A PAL20R6A PAL20R4A	24NS,JS, 28NL	TTL					25	25	210

Standard PAL Devices *(Cont.)*

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
20R8 (Cont.)	PAL20L8A-2	24NS,JS, 28NL	TTL	14	6 Comb	2 Comb	7	35	16	105
	PAL20R8A-2			12	–	8 Reg	8			
	PAL20R6A-2			12	2 Comb	6 Reg	7,8			
	PAL20R4A-2			12	4 Comb	4 Reg	7,8			
24R10	PAL24L10-10	28P	TTL	16	8 Comb	2 Comb	7	10	55.5	210
	PAL24R10-10			14	-	10 Reg	8			
	PAL24R8-10			14	2 Comb	6 Reg	7,8			
	PAL24R4-10			14	6 Comb	4 Reg	7,8			
20X10/ 20L10	PAL20L10A	24NS,JS, 28NL	TTL	10	10 Comb	-	3	30	22.2	165
	PAL20X10A			10	-	10 RegXOR	4			180
	PAL20X8A			10	2 Comb	8 RegXOR	3,4			180
	PAL20X4A			10	6 Comb	4RegXOR	3,4			180
	AmPAL20L10B	24P,D,28J						15	–	210
	AmPAL20L10-20							20		165
	AmPAL20L10AL							25		105

Universal PAL Devices

Family	Part Number	Package	Technology	Inputs	I/O	Product Terms/Output	Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
29M16	PALCE29M16H-25	24P,D,28J	EE CMOS	5	16 Macro	8-16	Advanced	25	33.3	100
	PALCE29M16H-35						I/O Macrocell	35	25	
610	PALCE610H-15	24P,28J	EE CMOS	4	16 Macro	8	J-K	15	45	90
	PALCE610H-25						Async.	25	28.6	
26V12	PALCE26V12H-20	28P,J	EE CMOS	14	12 Macro	8-16	28 pin	20	40	105
	PALCE26V12H-25						22V10	25	33.3	
22V10	PAL22V10-10	24P,D,28J	TTL	12	10 Macro	8-16	Varied Term	10	71	180
	PAL22V10-15						Distribution	15	50	
	AmPAL22V10A							25	28.5	
	AmPAL22V10							35	18	
	PALCE22V10H-15		EE CMOS					15	50	90
	PALCE22V10Q-25							25	33.3	55
	PALCE22V10H-25							25	33.3	90
	PALCE22V10Z-25							25	33.3	0.1
24V10	PALCE24V10H-15	28P,J	EE CMOS	14	10 Macro	8	GAL®	15	45.5	90
	PALCE24V10H-25						type	25	37	
20V8	PALCE20V8H-15	24P,28J	EE CMOS	12	8 Macro	8	GAL device	15	45.5	90
	PALCE20V8H-25						equivalent	25	37	
16V8	PALCE16V8H-10	20P,J	EE CMOS	8	8 Macro	8	GAL device	10	55.5	90
	PALCE16V8Q-15						equivalent	15	45.5	55
	PALCE16V8H-15							15	45.5	90
	PALCE16V8Q-25							25	37	55
	PALCE16V8H-25							25	37	90
	PALCE16V8Z-20							20	40	0.1
18P8	AmPAL18P8B	20P,D,J	TTL	10	8 Comb	8	Polarity	15	–	180
	AmPAL18P8AL							25		90
	AmPAL18P8A							25		180
	AmPAL18P8L							35		90
22P10	AmPAL22P10B	24P,D,28J	TTL	12	10 Comb	8	Polarity	15	–	180
	AmPAL22P10AL							25		90
	AmPAL22P10A							25		180

Asynchronous PAL Devices

Family	Part Number	Package	Technology	Inputs	Macro-Cells	Product Terms/ Output	Clock	Other Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
29MA16	PALCE29MA16H-25 PALCE29MA16H-35	24P,D,28J	EE CMOS	5	16	4-12	Program-mable	Advanced I/O Macrocell	25 35	33.3 25	100
20RA10	PAL20RA10-20 PAL20RA10	24NS,JS,28FN 24NS,JS,28NL	TTL	10	10	4	Program-mable		20 30/35*	30 20	200
16RA8	PAL16RA8	20N,J,NL	TTL	8	8	4	Program-mable		30/35*	20	170
IPAC™	PAL22IP6-25	24P,D,28J	TTL	16	6	9	Edge-Activated Flip-Flops	48-64 mA I_{OL}	25	–	210

* Active HIGH

Sequencer PAL Devices

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/ Output	Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
23S8	AmPAL23S8-20 AmPAL23S8-25	20P,D	TTL	9	4 Macro	4 Reg	6-12	6 Buried Flip-Flops	20 25	33.3 25	210
32VX10	PAL32VX10A PAL32VX10	24JS	TTL	12	10 Macro	–	8-16	Buried Flip-Flops, J-K Flip-Flops	25 30	25 22.2	180

Programmable Logic Sequencers

Family	Part Number	Package	Technology	Inputs	Outputs	Output or Buried Register	Buried Registers	Product Terms	Features	f_{MAX} MHz	I_{CC} mA
PLS	PLS30S16-40	28P,J	TTL	12-17	8-12Macro	–	4-12	64	PLA structure,	40	225
	PLS105-40	28R,P,D,J	TTL	16	8 Reg	–	6	48	complement	40	200
	PLSCE105H-37	28R,P,D,J	EE CMOS	16	8 Reg	–	6	48	array	37	100
	PLS167-33	24NS,JS,28FN	TTL	14	4 Reg	2	6	48		33	160
	PLSCE167H-33	24P,J	EE CMOS	14	4 Reg	2	6	48		33	100
	PLS168-33	24NS,JS,28FN	TTL	12	4 Reg	4	6	48		33	160
	PLSCE168H-33	24P,J	EE CMOS	12	4 Reg	4	6	48		33	100

Memory/Instruction-Based Sequencers

Family	Part Number	Package	Technology	Inputs	Outputs	Array Size	Features	f_{MAX} MHz	I_{CC} mA
Field-Program-mable Controllers	Am29CPL151H-33	28P,D,J	UV CMOS	8	16 Reg	64 x 32	Instruction-based with Counter and Stack	33	115
	Am29CPL151H-25							25	115
	Am29CPL154H-30			7	16 Reg	512 x 36		30	125
	Am29CPL154H-25							25	125
PEG™	Am2971A	24D,44L	TTL	3	12 Reg	32 x 18	Frequency-multiplying phase-locked loop	100	425

ECL PAL Devices

Family	Part Number	Package	Technology	Inputs	I/O	Product Terms/Output	Features	t_{PD} ns	f_{MAX} MHz	I_{EE} mA
ECL	PAL10H20EV8-6	24P,D,28J	ECL 10KH	12	8 Macro	8-12	Prog. Polarity	6	125	260
	PAL10020EV8-6		ECL 100K		(Reg)			6	125	285
	PAL10H20EG8-6		ECL 10KH		8 Macro			6	–	260
	PAL10020EG8-6		ECL 100K		(Latched)			6	–	285

Field-Programmable Gate Arrays

Family	Part Number	Package	Technology	I/O Blocks	Configurable Logic Blocks	Flip-Flops	Equivalent Gates	f_{MAX} MHz	I_{CC} mA
Logic Cell™ Array 2000 Series	Am2018-100 Am2018-70 Am2018-50	44J,68J,G 84J,G	CMOS RAM	74	100	174	1800	100 70 50	5
	Am2064-100 Am2064-70 Am2064-50	28J,48P,68J,G	CMOS RAM	58	64	122	1200	100 70 50	5
Logic Cell Array 3000 Series	Am3020-100 Am3020-70 Am3020-50	68J,G,84J,G	CMOS RAM	64	64	256	2000	100 70 50	1
	Am3030-100 Am3030-70 Am3030-50	84J,G	CMOS RAM	80	100	360	3000	100 70 50	1.3
	Am3042-100 Am3042-70 Am3042-50	84J,G,132G	CMOS RAM	96	144	480	4200	100 70 50	1.65
	Am3064-100 Am3064-70 Am3064-50	132G	CMOS RAM	120	224	688	6400	100 70 50	2.15
	Am3090-100 Am3090-70 Am3090-50	175G	CMOS RAM	144	320	928	9000	100 70 50	3

Package Designators

MMI Devices	AMD Devices	Package	MMI Devices	AMD Devices	Package
N	P	Plastic DIP	–	J	Windowed SKINNYDIP
NS	P	Plastic SKINNYDIP®	NL	J	PLCC-20-pin
–	R	Plastic SKINNYDIP Option	NL	–	PLCC-28-pin non-JEDEC
J	D	Ceramic DIP	FN	J	PLCC-28-pin JEDEC
JS	D	Ceramic SKINNYDIP	–	L	Leadless Chip Carrier
			–	G	Pin Grid Array

"MMI" devices are those produced by Monolithic Memories, Inc. before the companies merged.

PAL16R8 Family

20-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns maximum propagation delay
- Popular 20-pin architectures: 16L8, 16R8, 16R6, 16R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization on most devices
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 20-pin DIP and PLCC packages save space

GENERAL DESCRIPTION

The PAL16R8 Family (PAL16L8, PAL16R8, PAL16R6, PAL16R4) is AMD's standard 20-pin PAL device family. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL16L8	10	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication # 10240 Rev. B Amendment /0
Issue Date: January 1990

PERFORMANCE OPTIONS

(Commercial)

Speed (t_{PD}, ns)				
	35	B–4	A-2	
	25		B-2	A
	15		H-15	B
	10			D
	7.5			-7
		55	80–100	155–180

Power (I_{CC}, mA)

Note:

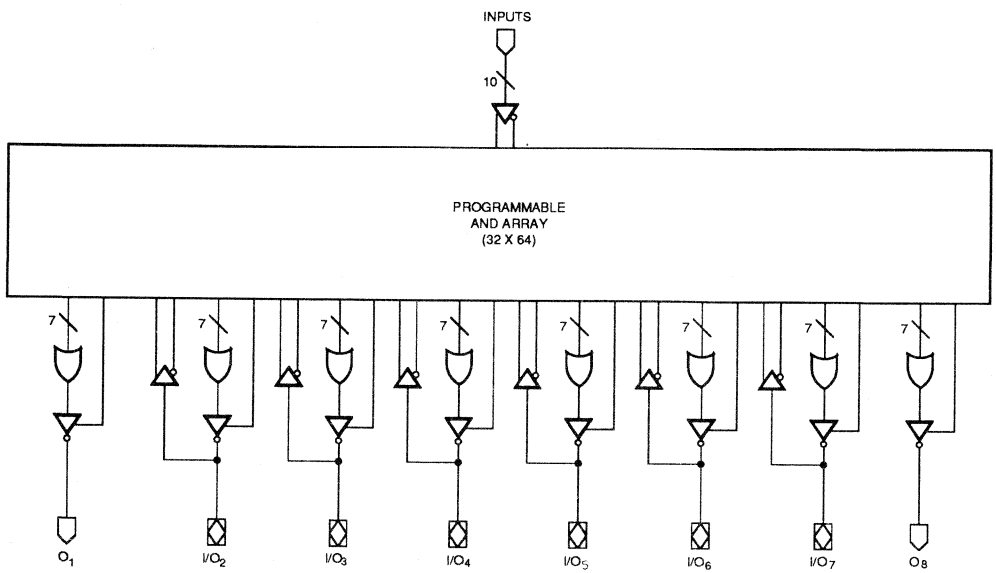
For low power and high speed, the EE CMOS PALCE16V8 can directly replace the PAL16R8 Family.

OPERATING RANGES

Commercial	Military
-7	-12
D (10 ns)	D (15 ns)
H-15	
B (15 ns)	B (20 ns)
B-2 (25 ns)	B-2 (30 ns)
A (25 ns)	A (30 ns)
B-4 (35 ns)	B-4 (50 ns)
A-2 (35 ns)	A-2 (50 ns)

BLOCK DIAGRAMS

PAL16L8



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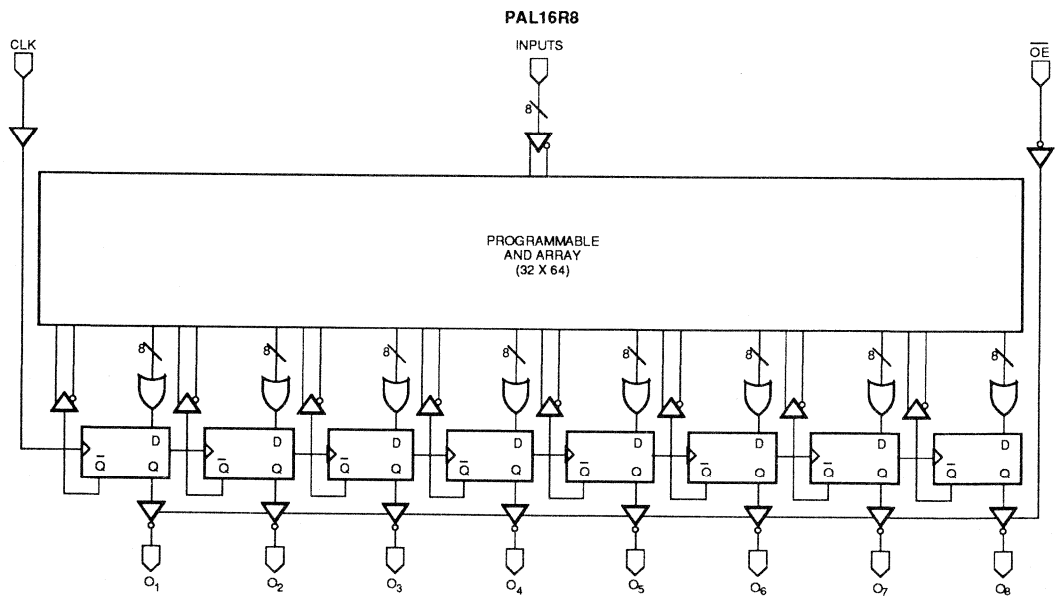
PAL16R8



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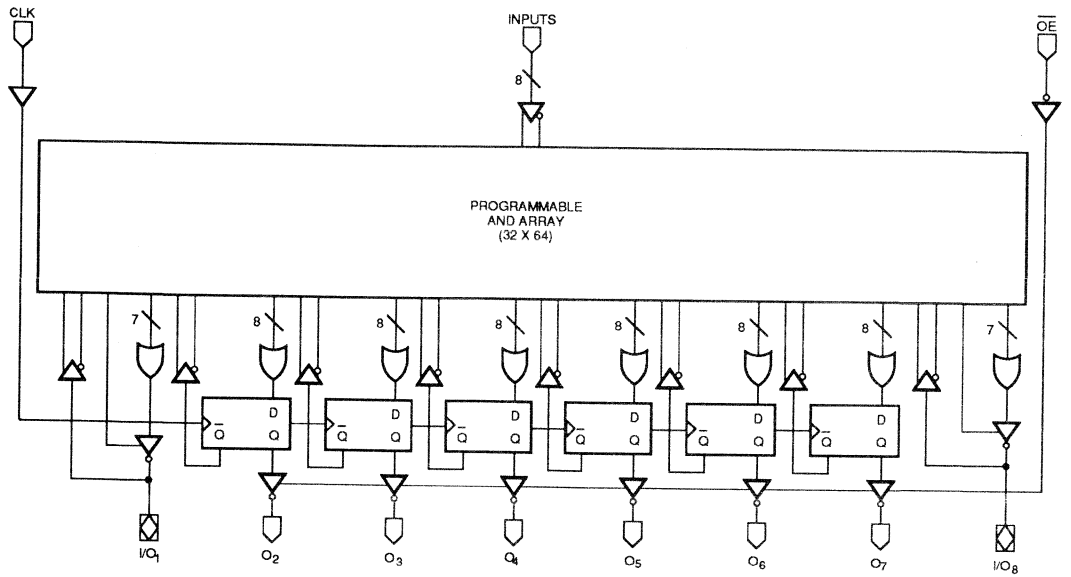
BLOCK DIAGRAMS

PAL16R6



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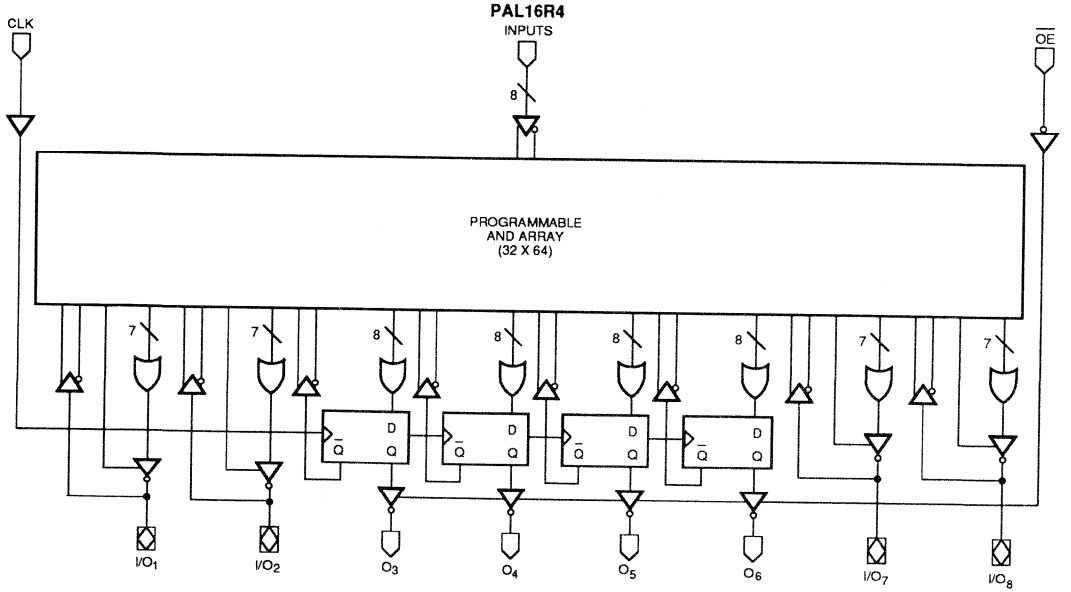
PAL16R4



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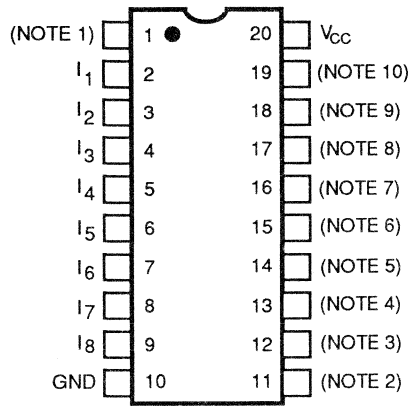
CONNECTION DIAGRAMS
Top View

DIP/FLATPACK



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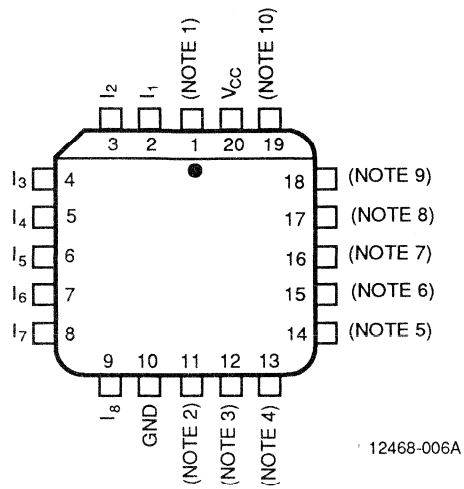
PLCC/LCC



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Note	16L8	16R8	16R6	16R4
1	I_0	CLK	CLK	CLK
2	I_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

PIN DESIGNATIONS

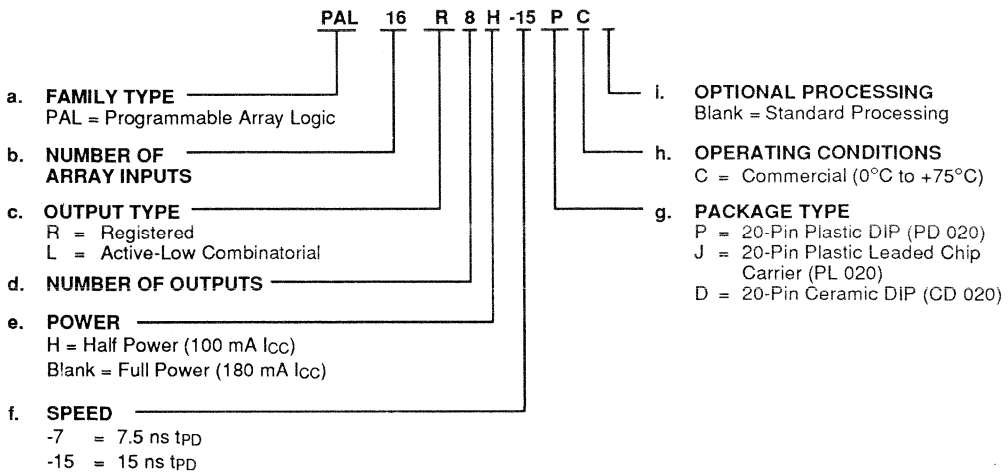
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products (AMD Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Power**
f. **Speed**
g. **Package Type**
h. **Operating Conditions**
i. **Optional Processing**



Valid Combinations		
PAL16L8	-7, H-15	PC, JC, DC
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

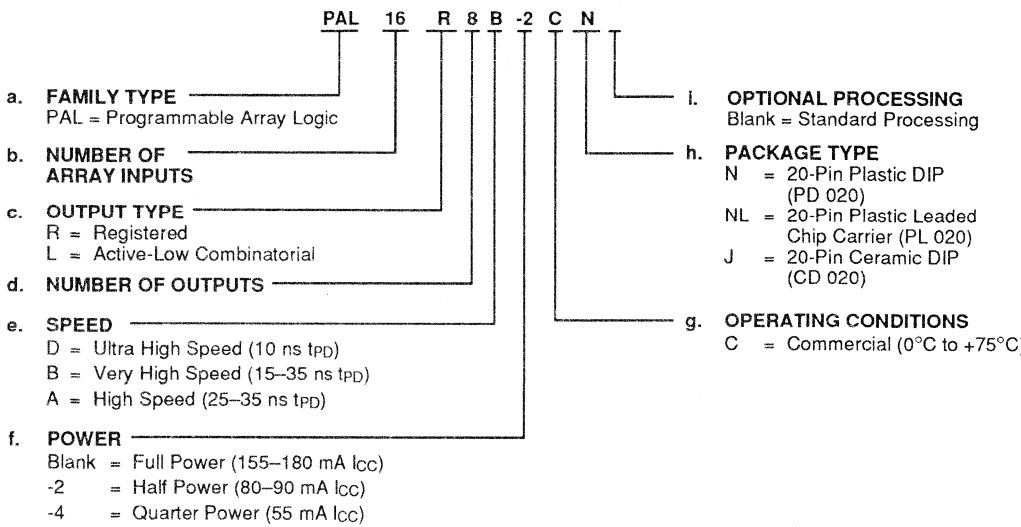
Note: Marked with AMD logo.

ORDERING INFORMATION

Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Power
g. Operating Conditions
h. Package Type
i. Optional Processing



Valid Combinations		
PAL16L8	D, B	CN, CNL, CJ
PAL16R8	B-2, A	
PAL16R6	B-4, A-2	
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

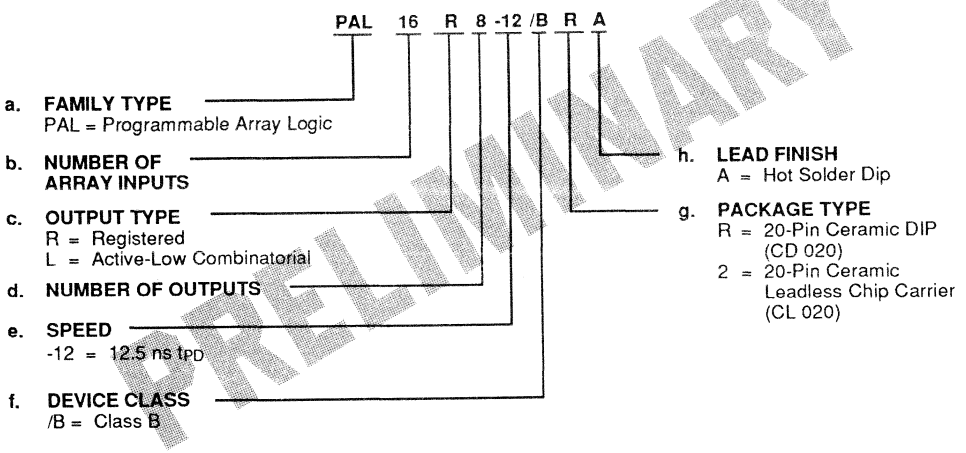
Note: Marked with MMI logo.

ORDERING INFORMATION

APL Products (AMD Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Device Class**
g. **Package Type**
h. **Lead Finish**



Valid Combinations		
PAL16L8	-12	/BRA, /B2A
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

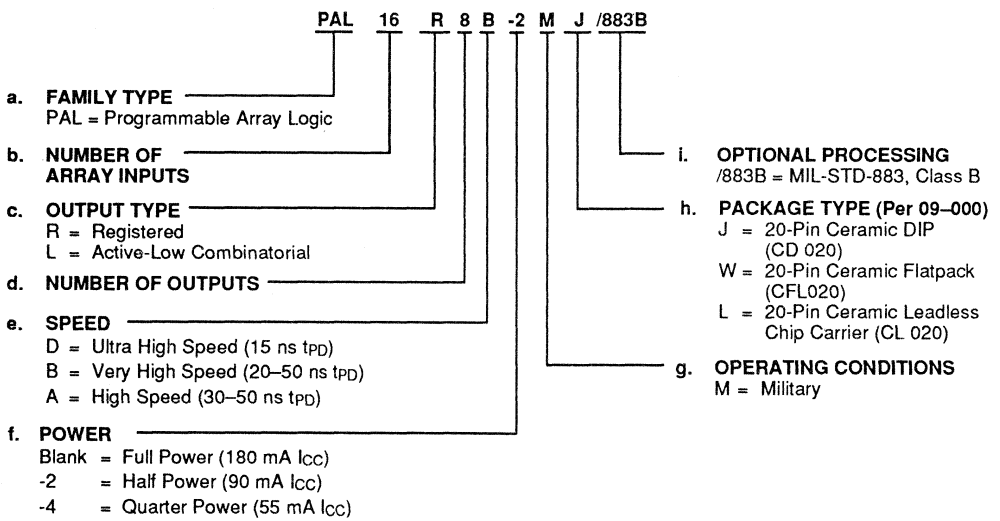
Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

ORDERING INFORMATION
APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Power
g. Operating Conditions
h. Package Type
i. Optional Processing



Valid Combinations		
PAL16L8	D, B,	MJ/883B,
PAL16R8	B-2, A,	MW/883B,
PAL16R6	B-4, A-2	ML/883B
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional information on AMD's Standard Military grade products.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 20-pin PAL Family

The standard bipolar 20-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The PAL16L8 has ten dedicated input lines and six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin and may be configured as a dedicated input if the output buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

Applies to -7 (-12 Mil), H-15, B, B-2, A, A-2 Series Only

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the listed Series will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

Applies to -7 (-12 Mil), H-15 Series Only

The register on the listed Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL16R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact. Exceptions are the -7 (-12 Mil) Series, where the array will read as if every fuse is programmed.

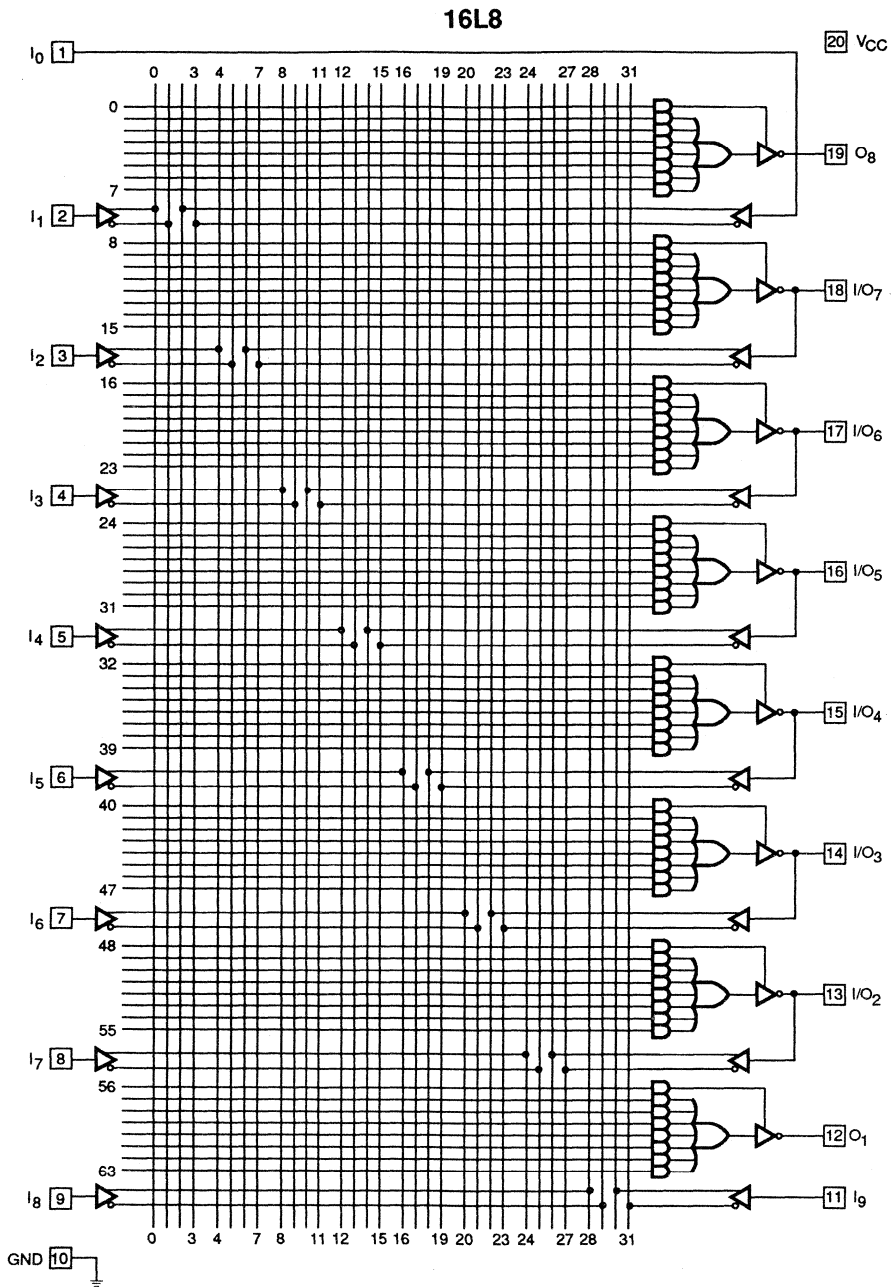
Quality and Testability

The PAL16R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed -7 (-12 Mil), D, and H-15 Series are fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for the -7 Series and TiW fuses for the D and H-15 Series. The remaining Series are fabricated with AMD's junction-isolated process, utilizing TiW fuses.

LOGIC DIAGRAM



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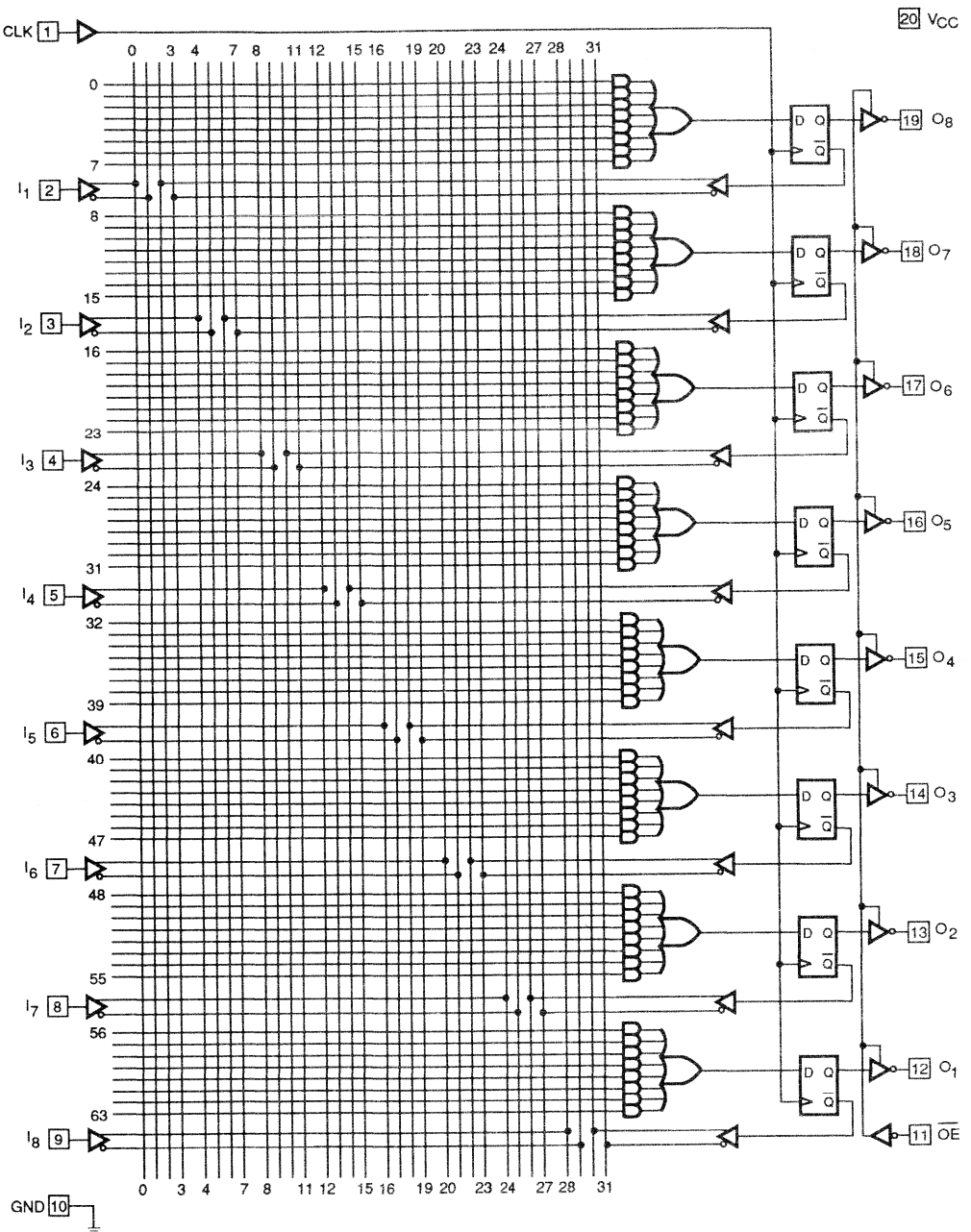
LOGIC DIAGRAM

16R8



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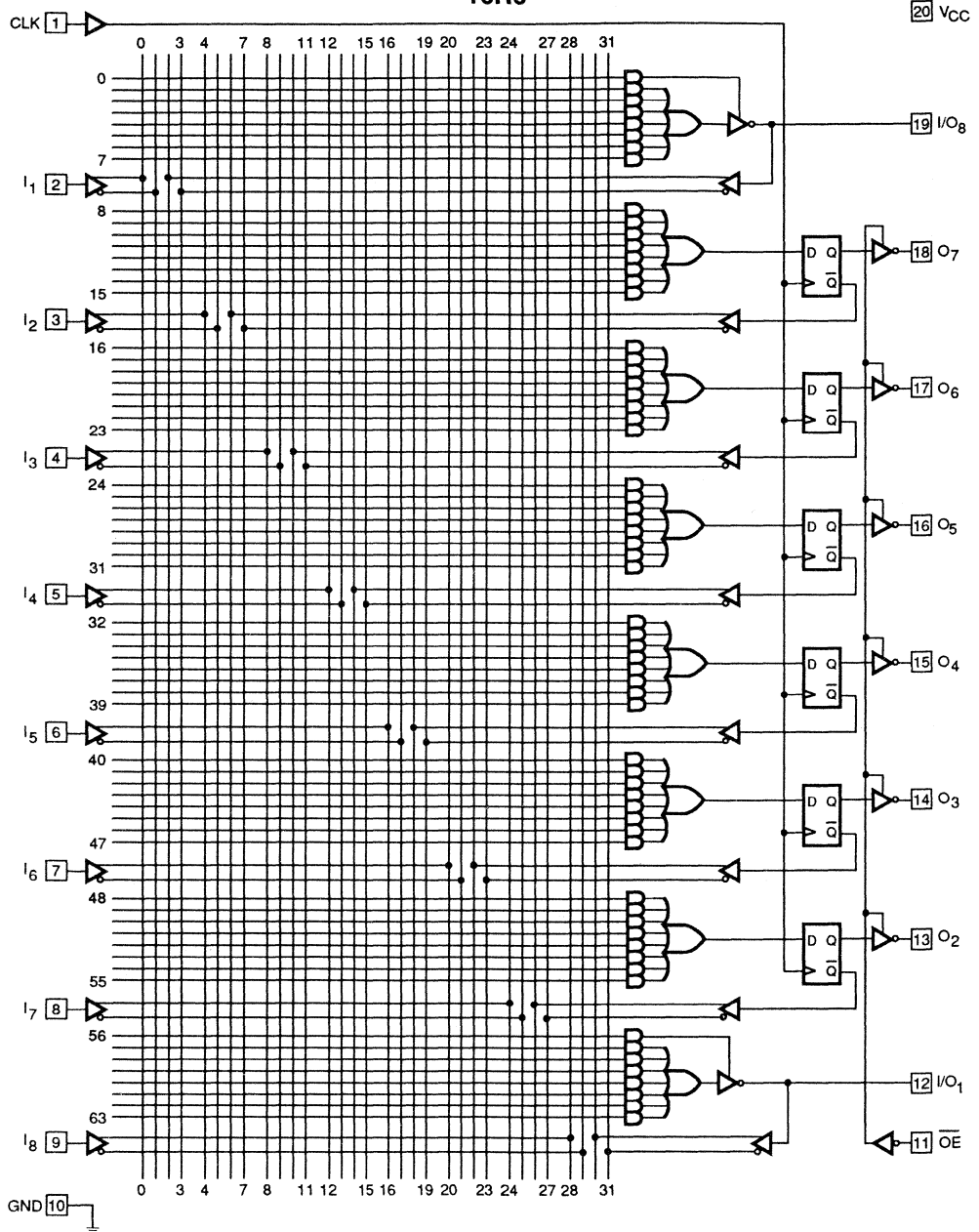
LOGIC DIAGRAM



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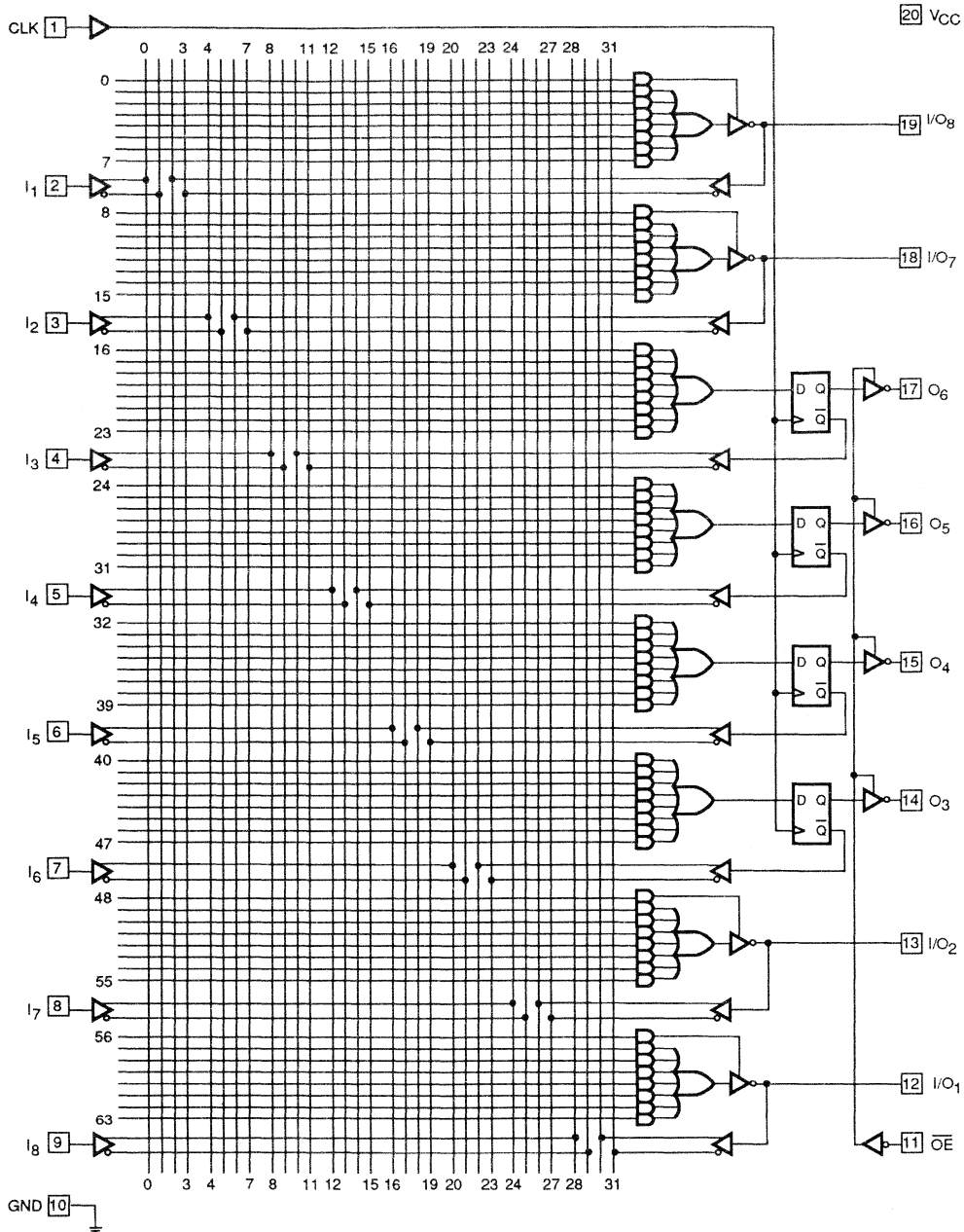
LOGIC DIAGRAM

16R4



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to +7.0 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6	3	7.5	ns
		1 Output Switching		16R4	3	7	
t_S	Setup Time from Input or Feedback to Clock				7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	6.5	ns
t_{CF}	Clock to Feedback (Note 4)					3	ns
t_{SKEW}	Skew Between Registered Outputs (Note 5)			16R8, 16R6		1	ns
t_{WL}	Clock Width	LOW		16R4	5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			16R4	3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

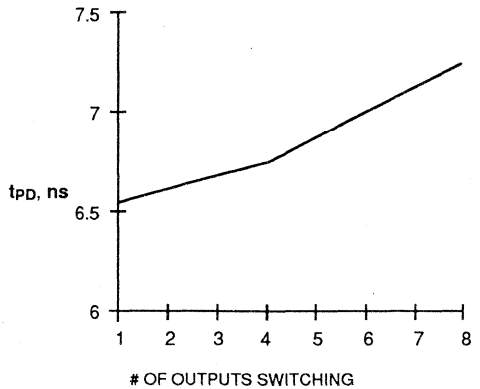
Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6	3	12.5	ns
		1 Output Switching		16R4	3	12	
t_S	Setup Time from Input or Feedback to Clock				12		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	11	ns
t_{CF}	Clock to Feedback (Note 4)					6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 5)					1	ns
t_{WL}	Clock Width	LOW		16R8, 16R6	10		ns
t_{WH}		HIGH		16R4	8		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$		43.4		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		54		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		55.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 7)				3	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 7)				3	10	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 7)			16L8, 16R6 16R4	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 7)				3	12	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f_{MAX} internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

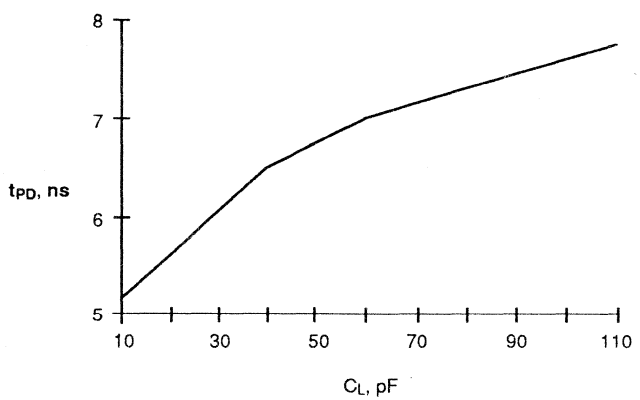
MEASURED SWITCHING CHARACTERISTICS

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

10240-001A



t_{PD} vs. Load Capacitance

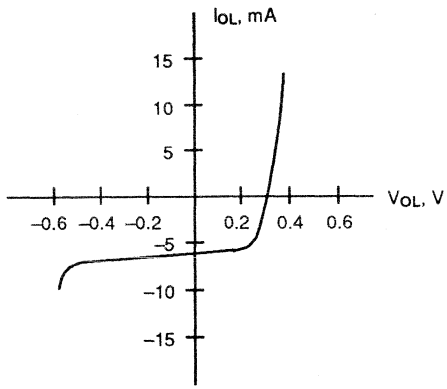
10240-002A

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

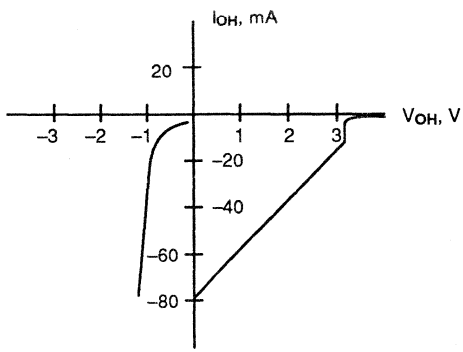
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



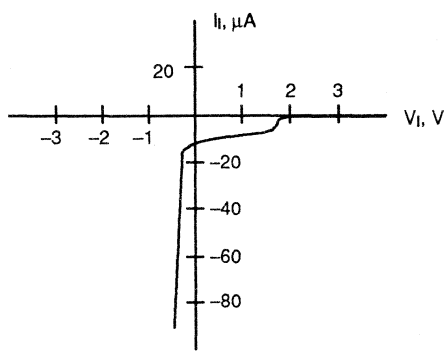
Output, LOW

10240-003A



Output, HIGH

10240-004A



Input

10240-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to +5.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	9	pF
			T_A = 25°C	Other Inputs	2	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	4	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	7	ns
t_{CF}	Clock to Feedback (Note 4)				2	6.5	ns
t_{WL}	Clock Width	LOW			8		ns
t_{WH}		HIGH			8		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		58.8		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		60		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6 16R4	1	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				1	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	9	pF
			T_A = 25°C	Other Inputs	2	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	4	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4	3	15	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback				2	12	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			8		ns
f_{MAX}	Max. Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				3	12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				3	10	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)			16L8, 16R6 16R4	1	17	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				1	13	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output Current	16 mA
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		100	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	9	pF
			T_A = 25°C	Other Inputs	2	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	4	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		15	ns
t_S	Setup Time from Input or Feedback to Clock				15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					12	ns
t_{CF}	Clock to Feedback (Note 3)			16R8, 16R6		11	ns
t_{WL}	Clock Width	LOW		16R4	10		ns
t_{WH}		HIGH			9		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		38.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		52.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6		15	ns
t_{ER}	Input to Output Disable Using Product Term Control			16R4		15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		15	ns
t_S	Setup Time from Input or Feedback to Clock				15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					12	ns
t_{WL}	Clock Width	LOW		16R8, 16R6	10		ns
t_{WH}		HIGH		16R4	10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					15	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6		15	ns
t_{ER}	Input to Output Disable Using Product Term Control			16R4		15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to + 5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		25	ns
t_S	Setup Time from Input or Feedback to Clock				25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{CF}	Clock to Feedback (Note 3)			16R8, 16R6		10	ns
t_{WL}	Clock Width	LOW		16R4	15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		90	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		30	ns
t_S	Setup Time from Input or Feedback to Clock				30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW		16R8, 16R6	20		ns
t_{WH}		HIGH		16R4	20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6 16R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					30	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage		I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current		V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current		V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current		V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	16L8	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		155	mA
		16R8/6/4			180	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{CC} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{CF}	Clock to Feedback (Note 3)					10	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6 16R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					30	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		55	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V as been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		35	ns
t_S	Setup Time from Input or Feedback to Clock				35		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback			16R8, 16R6		25	ns
t_{WL}	Clock Width	LOW		16R4	25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		16		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					25	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6		35	ns
t_{ER}	Input to Output Disable Using Product Term Control			16R4		35	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		55	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		50	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	50		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		13.3		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			16L8, 16R6 16R4		45	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					45	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage		I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current		V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current		V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current		V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	16L8	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		80	mA
		16R8/6/4			90	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V as been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		35	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6 16R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		18		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					25	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6 16R4		35	ns
t_{ER}	Input to Output Disable Using Product Term Control					35	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		90	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

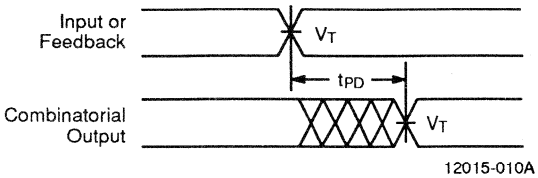
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6 16R4		50	ns
t_S	Setup Time from Input or Feedback to Clock				50		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW		16R8, 16R6 16R4	25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		13.3		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6 16R4		45	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					45	ns

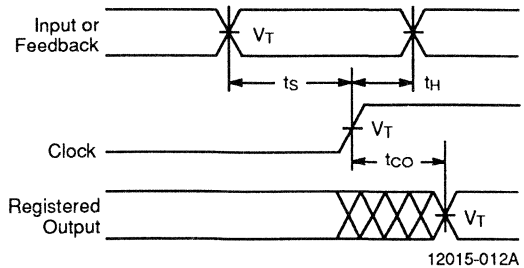
Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

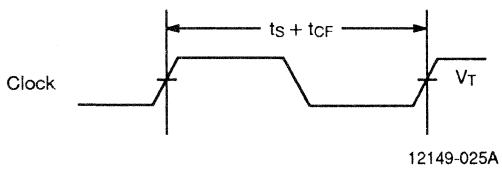
SWITCHING WAVEFORMS



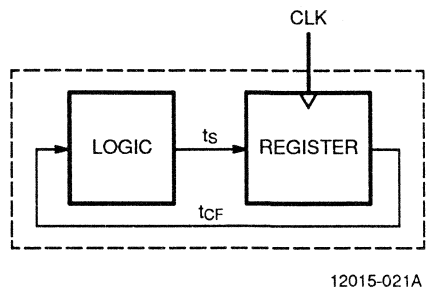
Combinatorial Output

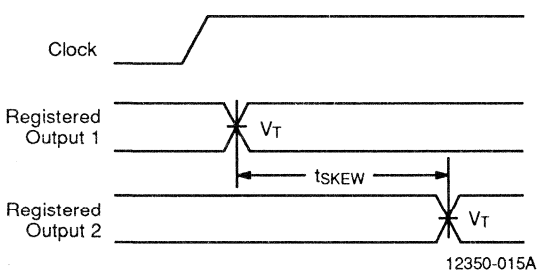


Registered Output

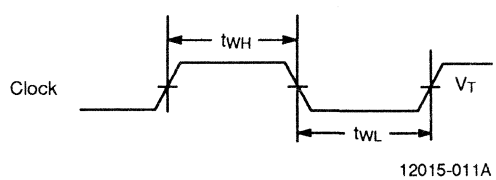


Clock to Feedback (f_{MAX} Internal)
See Path at Right

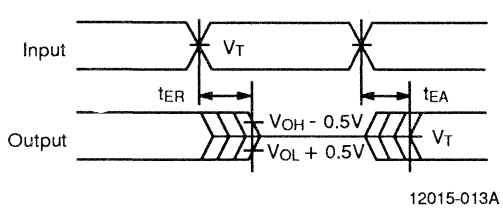




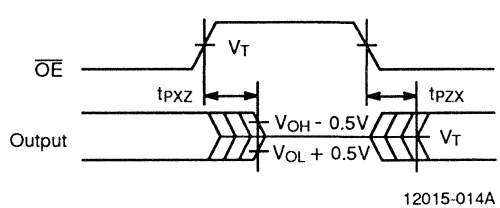
Registered Output Skew for Outputs Switching in the Same Direction



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

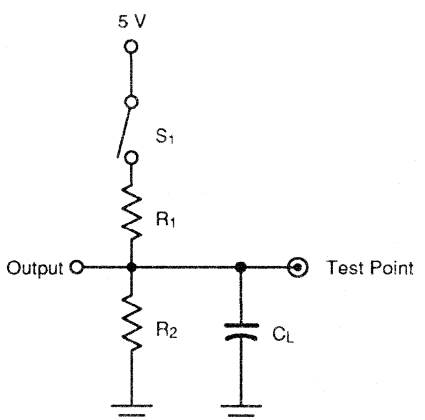
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.
   (2–4 ns for -7 (-12 Mil) Series)

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

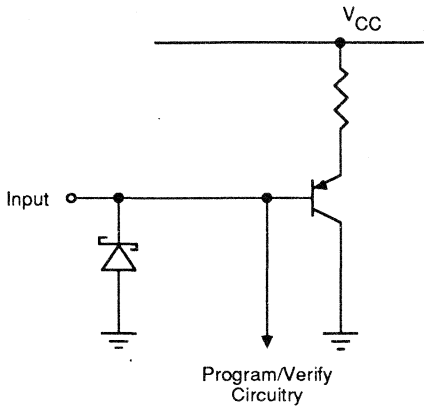


12350-019A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	B-4: 800 Ω	B-4: 1.56 KΩ	B-4: 800 Ω	B-4: 1.56 KΩ	H → Z: V_{OH} − 0.5 V L → Z: V_{OL} + 0.5 V

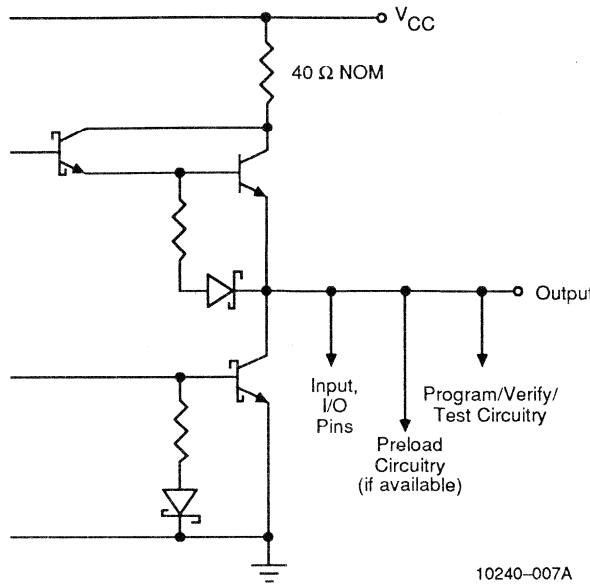
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



10240-006A

Typical Output



10240-007A

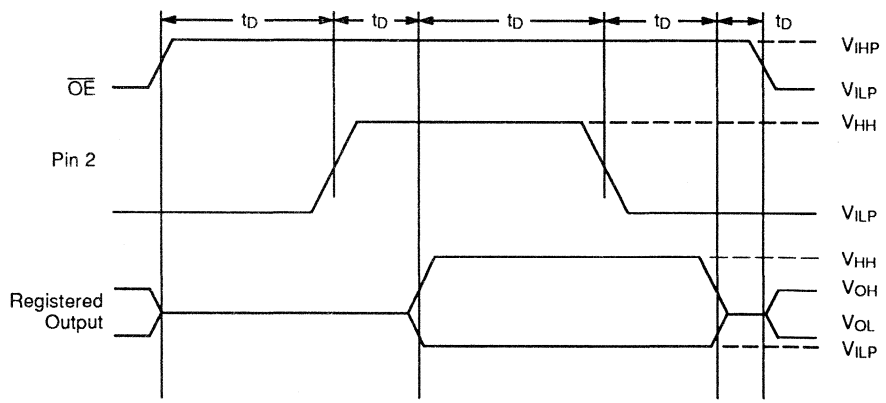
OUTPUT REGISTER PRELOAD

Applies to -7 (-12 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Raise pin 2 to V_{HH} to enter preload mode.
4. Apply either V_{HH} or V_{ILP} to all registered outputs. Use V_{HH} to preload a LOW in the flip-flop; use V_{ILP} to preload a HIGH in the flip-flop. Leave combinatorial outputs floating.
5. Lower pin 2 to V_{ILP}.
6. Remove V_{ILP}/V_{HH} from all registered output pins.
7. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	10	11	12	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload	5.4	5.7	6.0	V
t_D	Delay time	100	200	1000	ns



10294-003A

Output Register Preload Waveform

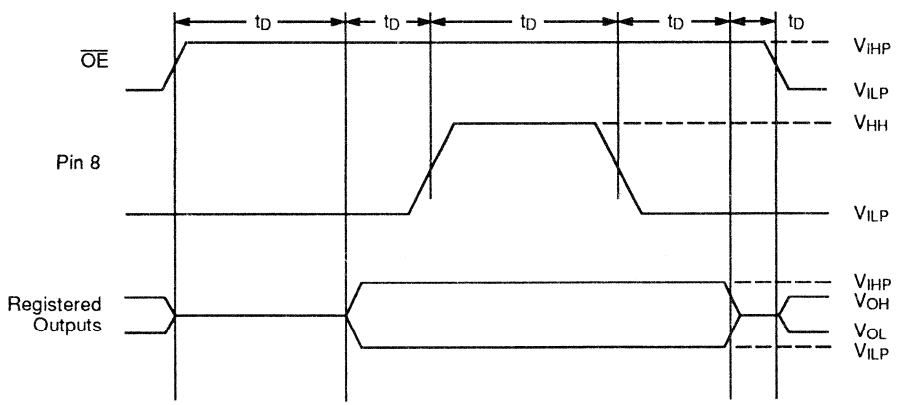
OUTPUT REGISTER PRELOAD

Applies to H-15 Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 4.5 V.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
4. Pulse pin 8 to V_{HH}, then back to 0 V.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
7. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19	20	21	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns



10240-008A

Output Register Preload Waveform

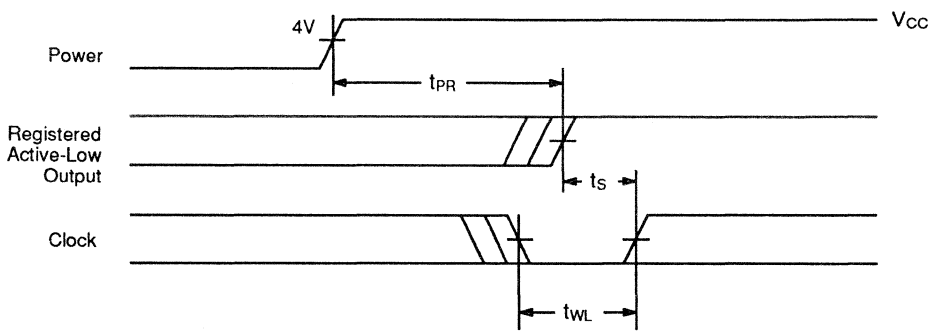
POWER-UP RESET

Applies to -7 (-12 Mil), H-15, B, B-2, A, A-2 Series Only

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform

PAL16RA8

20-pin Asynchronous TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 30 ns maximum propagation delay and 20 MHz f_{MAX}
- Individually programmable asynchronous clock, preset, reset, and enable
- Registered or combinatorial outputs
- Programmable polarity
- Programmable replacement for high-speed TTL logic
- TTL-level register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 20-pin DIP and 20-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL16RA8 offers asynchronous clocking for each of the eight flip-flops in the device. The eight macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PAL16RA8 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

The PAL16RA8 utilizes Advanced Micro Devices' advanced junction-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

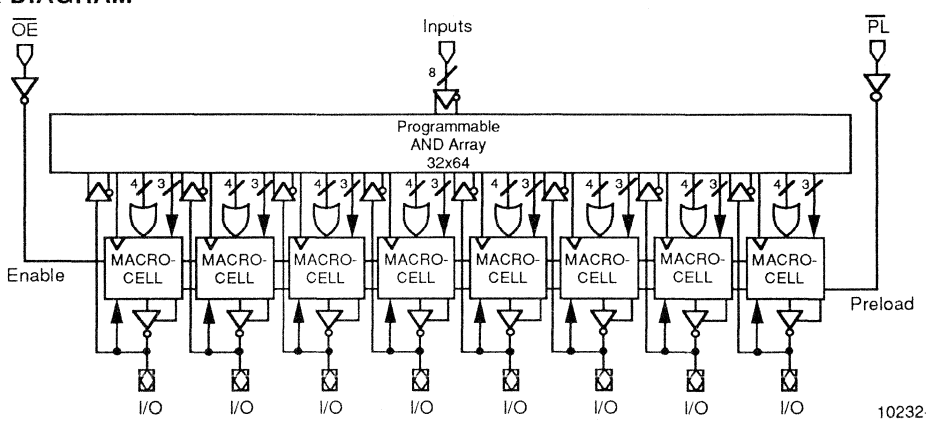
The PAL16RA8 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers.

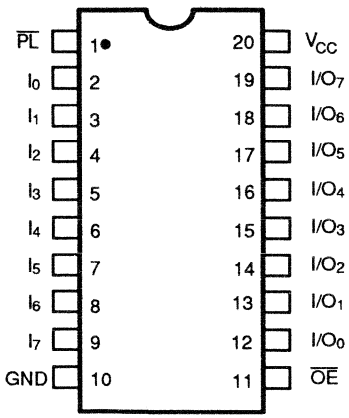
BLOCK DIAGRAM



Publication # 10232 Rev. B Amendment /0
Issue Date: January 1990

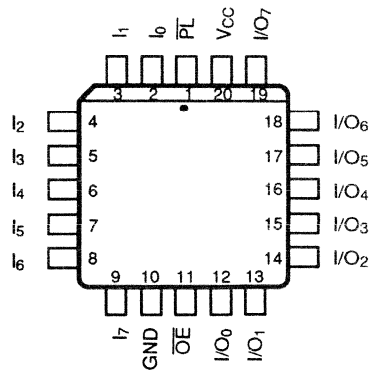
CONNECTION DIAGRAMS

DIP



10232-002A

PLCC



Note:
Pin 1 is marked for orientation.

10232-003A

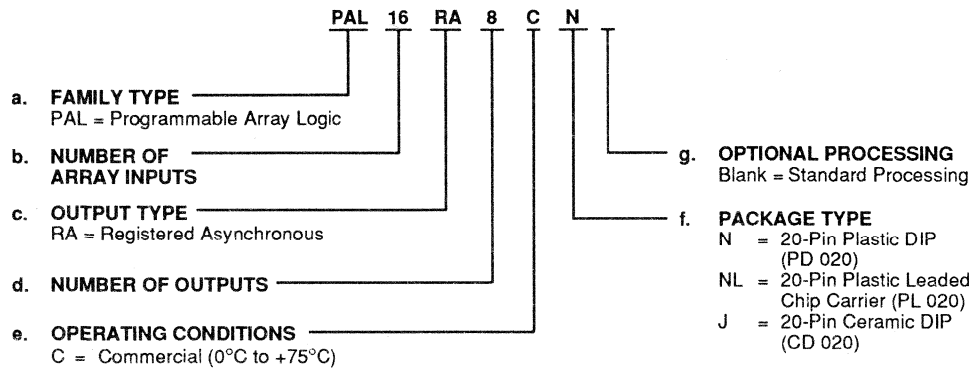
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
$\overline{OE}$	Output Enable
$\overline{PL}$	Preload
Vcc	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Operating Conditions**
f. **Package Type**
g. **Optional Processing**



Valid Combinations	
PAL16RA8	CN, CNL, CJ

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

FUNCTIONAL DESCRIPTION

The PAL16RA8 has eight dedicated input lines and eight programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 11 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PAL16RA8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes logic 1. If the reset product line is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed (Bypass Mode) and the output becomes combinatorial. Otherwise, the output is from the register (Registered Mode). Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flop-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

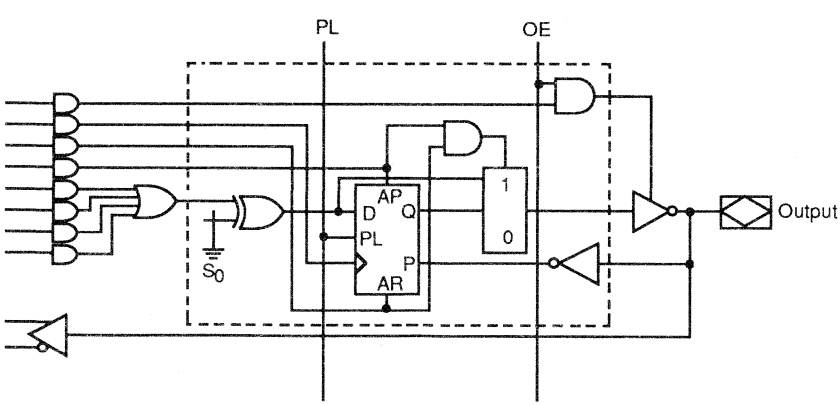
Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Fuse

A security fuse is also provided to prevent unauthorized copying of PAL device patterns. Once the fuse is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every array fuse is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer.

2



10232-004A

Figure 1. PAL16RA8 Macrocell

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PAL16RA8 logic diagram. When the output polarity fuse is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity fuse is intact, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming

The PAL16RA8 can be programmed on standard logic programmers. Programmers approved by Advanced Micro Devices are listed in the Programmer Reference Guide.

Register Preload

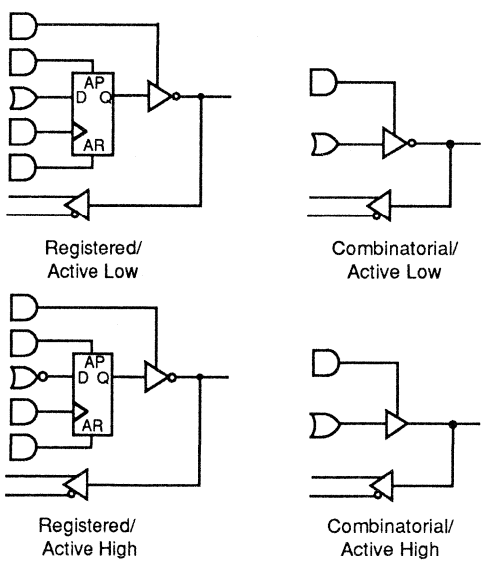
The register on the PAL16RA8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function.

Quality and Testability

The PAL16RA8 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL16RA8 is fabricated with AMD's junction-isolated process, utilizing TiW fuses.

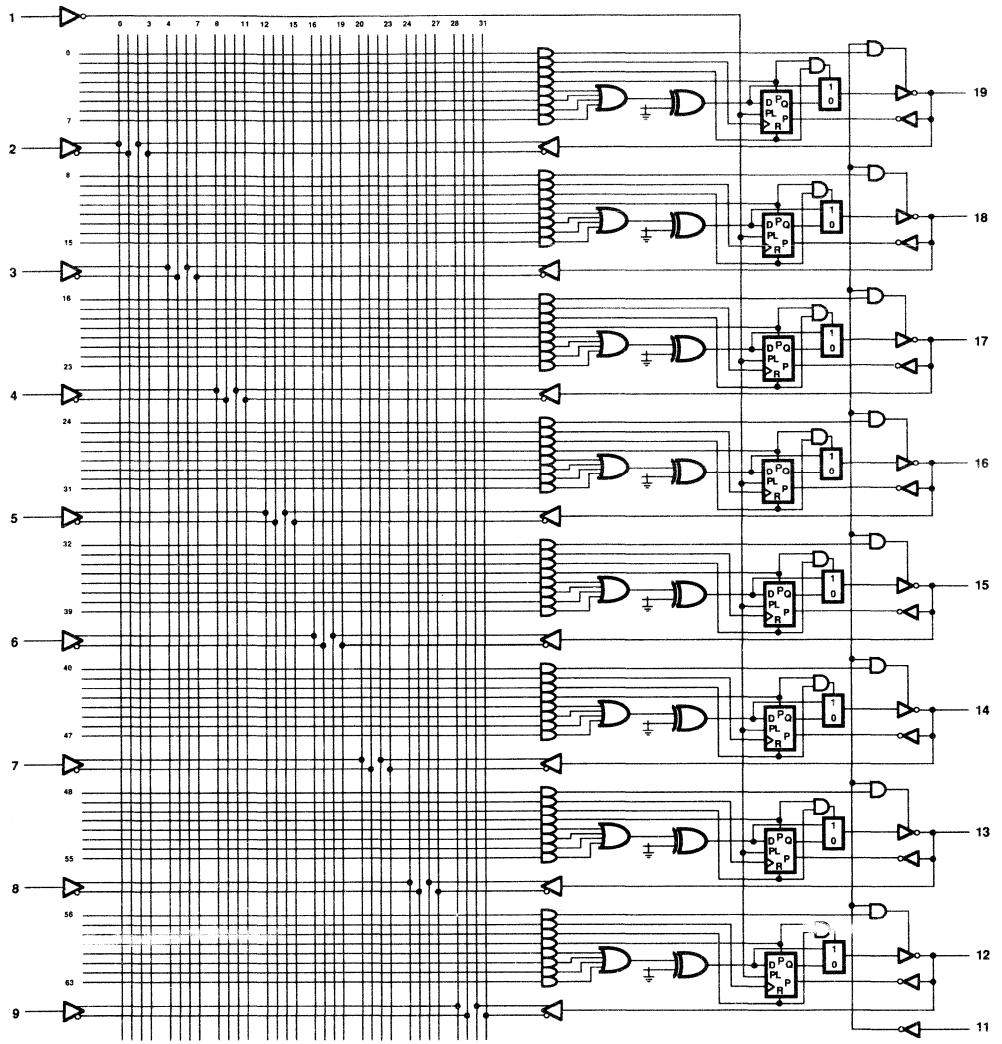


10232-005A

Figure 2. Macrocell Configurations

LOGIC DIAGRAM

PAL16RA8



10232-006A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		170	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

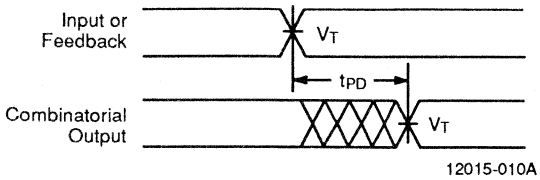
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			Min. (Note 2)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output	Active Low			30	ns
		Active High			35	ns
t_S	Setup Time from Input or Feedback to Clock			20		ns
t_H	Hold Time	Active Low		10		ns
		Active High		0		ns
t_{CO}	Clock to Output or Feedback			10	30	ns
t_{AP}	Asynchronous Preset to Registered Output				35	ns
t_{APW}	Asynchronous Preset Width			20		ns
t_{AR}	Asynchronous Reset to Registered Output				40	ns
t_{ARW}	Asynchronous Reset Width			20		ns
t_{WL}	Clock Width	LOW		20		ns
t_{WH}		HIGH		20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				20	ns
t_{EA}	Input to Output Enable Using Product Term Control				30	ns
t_{ER}	Input to Output Disable Using Product Term Control				30	ns

Notes:

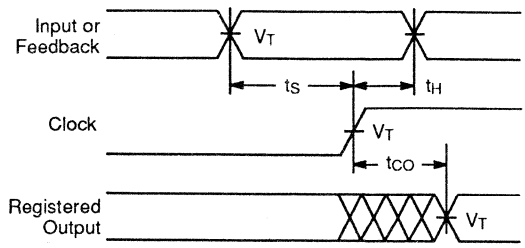
1. See Switching Test Circuit for test conditions.
2. Output delay minimums are measured under best-case conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



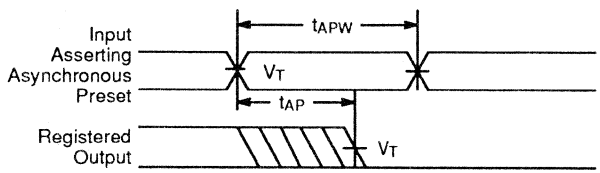
12015-010A

Combinatorial Output



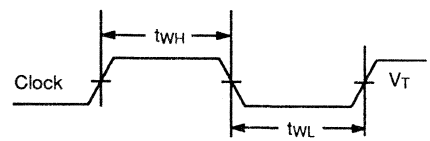
12015-012A

Registered Output



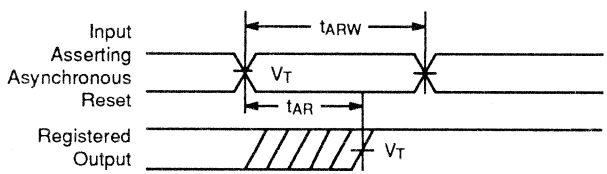
10232-007A

Asynchronous Preset



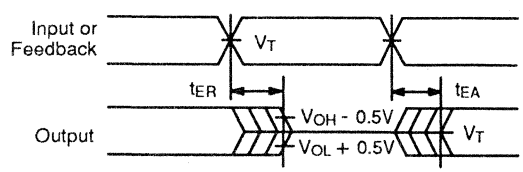
12015-011A

Clock Width



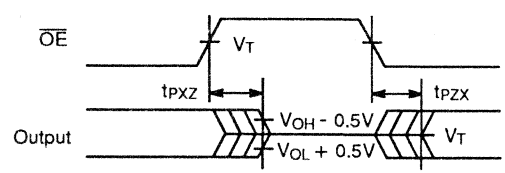
10232-009A

Asynchronous Reset



10232-008A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

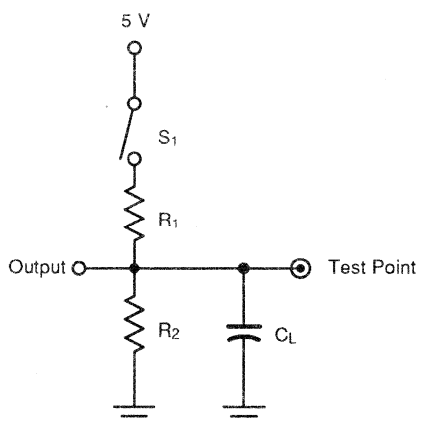
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

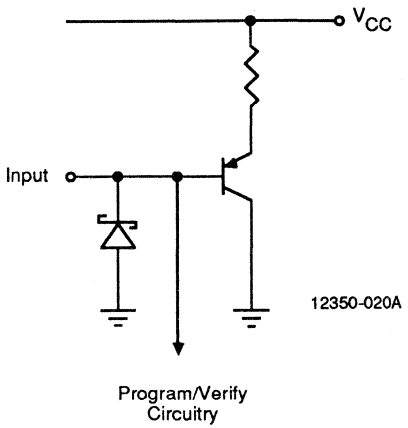


12350-019A

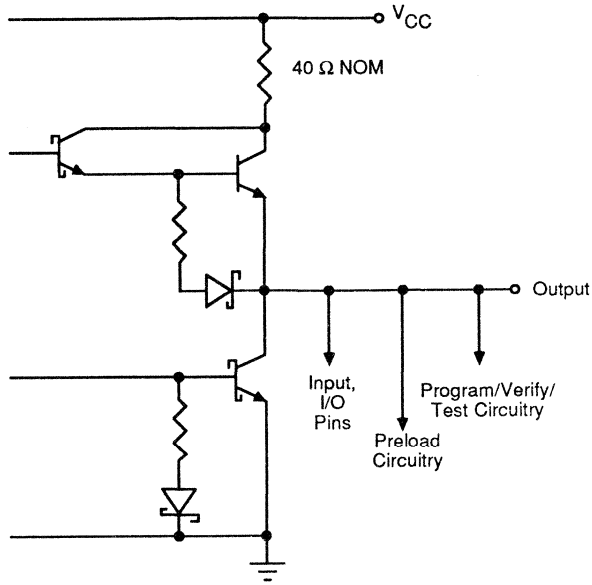
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	560 Ω	1.1 kΩ	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output

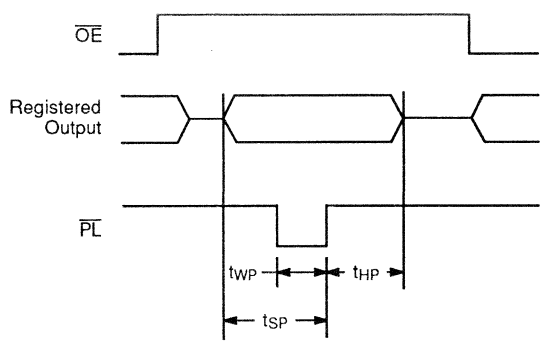


OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable output registers.
2. Apply either V_{IHP} or V_{ILP} to all registered outputs. Leave combinatorial outputs floating.
3. Pulse $\overline{PL}$ from V_{IHP} to V_{ILP} to V_{IHP}.
4. Remove V_{ILP}/V_{IHP} from all registered output pins.
5. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
6. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_{SP}	Preload setup time	25			ns
t_{WP}	Preload pulse width	35			ns
t_{HP}	Preload hold time	25			ns



10232-010A

Output Register Preload Waveform


IMPORTANT
NOTES

PALCE16V8

EE CMOS 20-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Pin, function and fuse-map compatible with all 20-pin GAL® devices
- Electrically erasable CMOS technology provides reconfigurable logic and full testability
- High speed CMOS technology
  - 10 ns propagation delay for "-10" version
  - 15 ns propagation delay for "-15" version
  - 25 ns propagation delay for "-25" version
- Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series
- Outputs programmable as registered or combinatorial in any combination
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Cost-effective 20-pin plastic DIP and PLCC packages
- Programmable on standard device programmers
- Supported by PALASM® software
- Fully tested for 100% programming and functional yields and high reliability

2

GENERAL DESCRIPTION

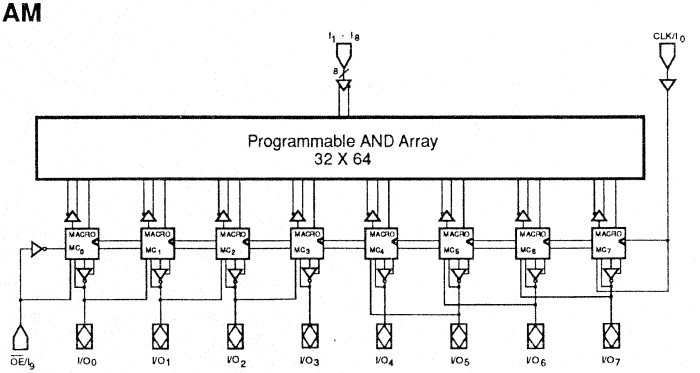
The PALCE16V8 is an advanced PAL® device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM

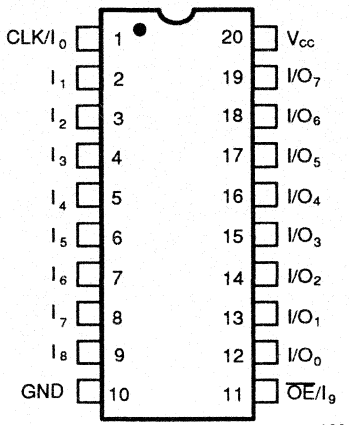


12467-001A

Publication # 12015 Rev. C Amendment/0
Issue Date: January 1990

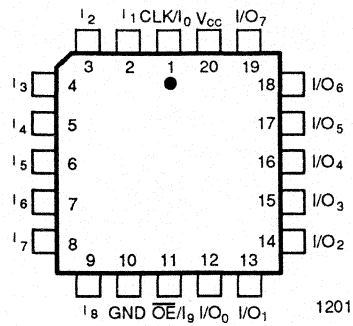
CONNECTION DIAGRAMS
Top View

DIP



12015-002A

PLCC/LCC



12015-003A

Note: Pin 1 is marked for orientation

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
V_{CC}	=	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Flip-Flops
f. Power
g. Speed
h. Package Type
i. Operating Conditions
j. Programming Designator

PAL CE 16 V 8 H -15 P C

a. FAMILY TYPE
PAL = Programmable Array Logic

b. TECHNOLOGY
CE = CMOS Electrically Erasable

c. NUMBER OF ARRAY INPUTS

d. OUTPUT TYPE
V = Versatile

e. NUMBER OF FLIP-FLOPS

f. POWER
H = Half Power (90 mA I_{CC})
Q = Quarter Power (55 mA I_{CC})

g. SPEED
-10 = 10 ns t_{PD}
-15 = 15 ns t_{PD}
-25 = 25 ns t_{PD}

h. PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
J = 20-Pin Plastic Leaded Chip Carrier (PL 020)

i. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

j. PROGRAMMING DESIGNATOR
Blank = Initial Release
/4 = First Revision
(May require different programmer revisions)

Valid Combinations		
PALCE16V8H-10	PC, JC	Blank, /4
PALCE16V8H-15		
PALCE16V8H-25		
PALCE16V8Q-15		
PALCE16V8Q-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Flip-Flops
f. Power
g. Speed
h. Programming Designator
i. Device Class
j. Package Type
k. Lead Finish

PAL CE 16 V 8 H -20 /B R A

a. FAMILY TYPE
PAL= Programmable Array Logic

b. TECHNOLOGY
CE = CMOS Electrically Erasable

c. NUMBER OF ARRAY INPUTS

d. OUTPUT TYPE
V = Versatile

e. NUMBER OF FLIP-FLOPS

f. POWER
H = Half Power (90 mA I_{CC})

g. SPEED
-20 = 20 ns t_{PD}
-25 = 25 ns t_{PD}

k. LEAD FINISH
A = Hot Solder Dip

j. PACKAGE TYPE
R = 20-Pin Ceramic DIP (CD 020)
2 = 20-Pin Ceramic Leadless Chip Carrier (CL 020)

i. DEVICE CLASS
/B = Class B

h. PROGRAMMING DESIGNATOR
Blank = Initial Release
E4 = First Revision
(May require different programmer revisions)

Valid Combinations		
PALCE16V8H-20	Blank, E4	/BRA, /B2A
PALCE16V8H-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 7, 8, 9, 10 and 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

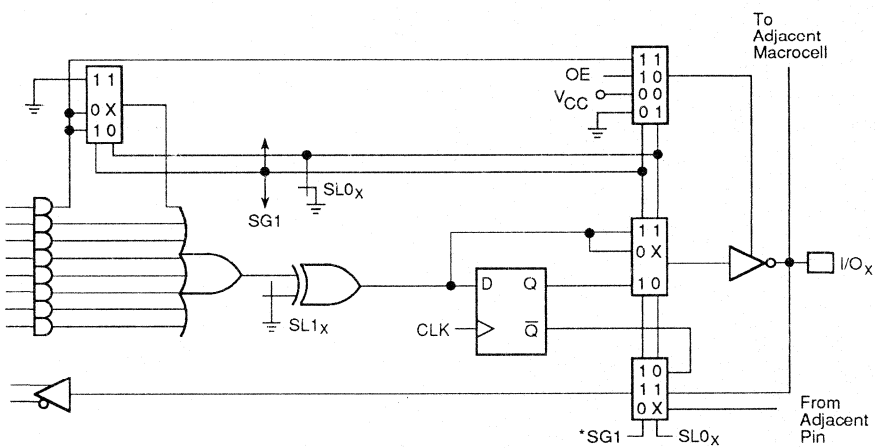
FUNCTIONAL DESCRIPTION

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



*In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

12015-004B

PALCE16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Because the macrocell is a dedicated output, the feedback is not used. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

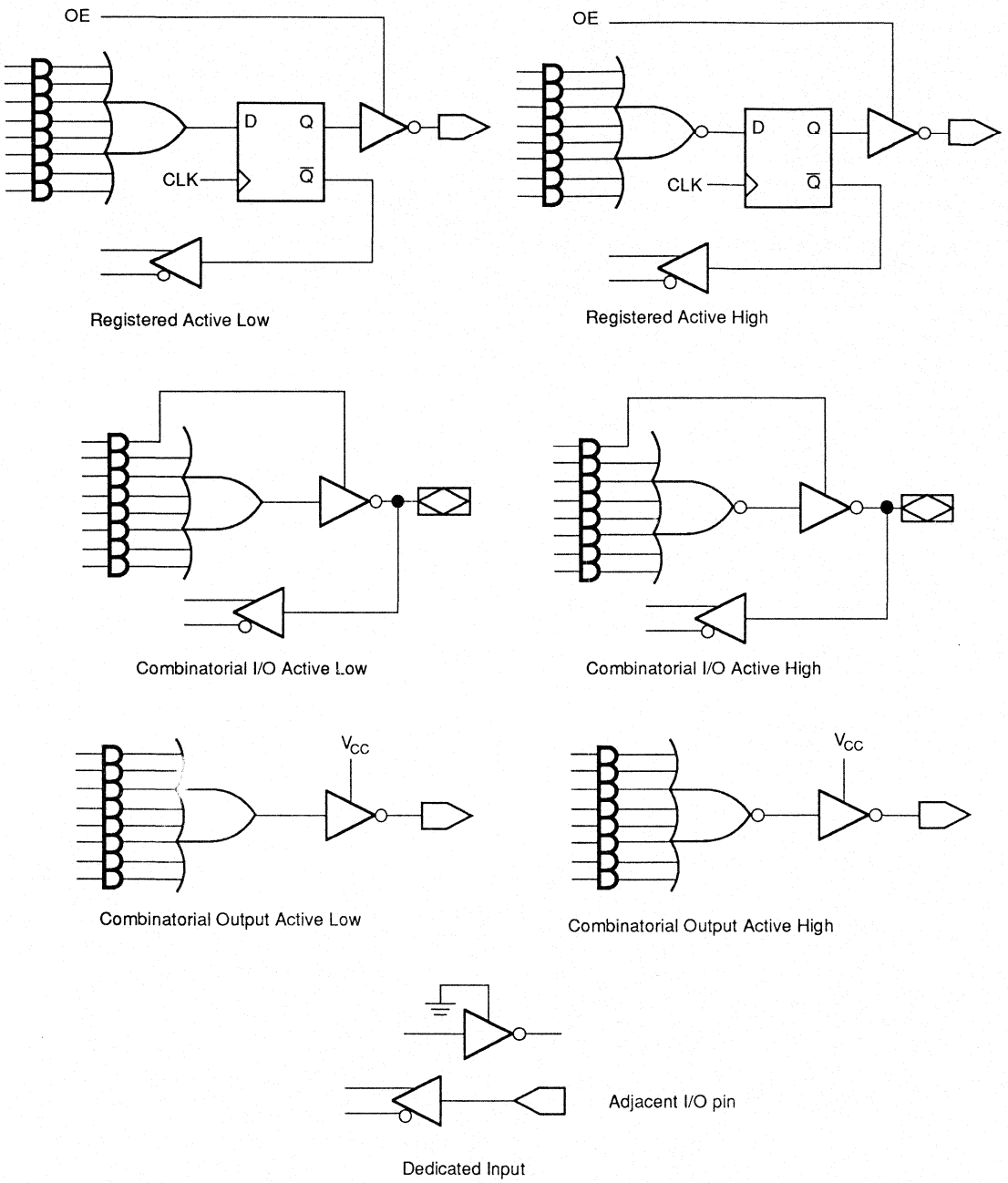
Table 1. Macrocell Configuration

SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Dedicated Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



12015-005A

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

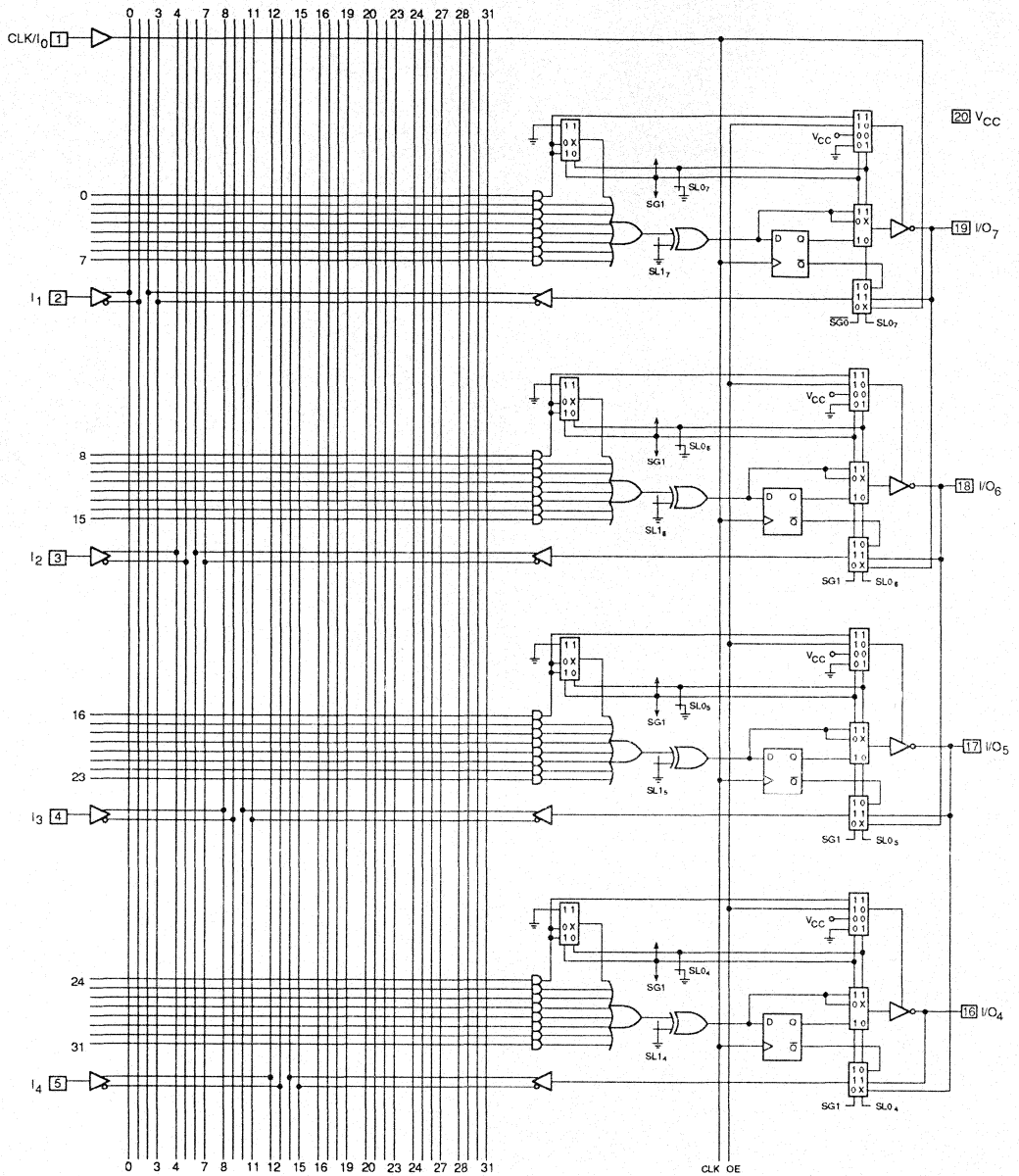
An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PALCE16V8 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

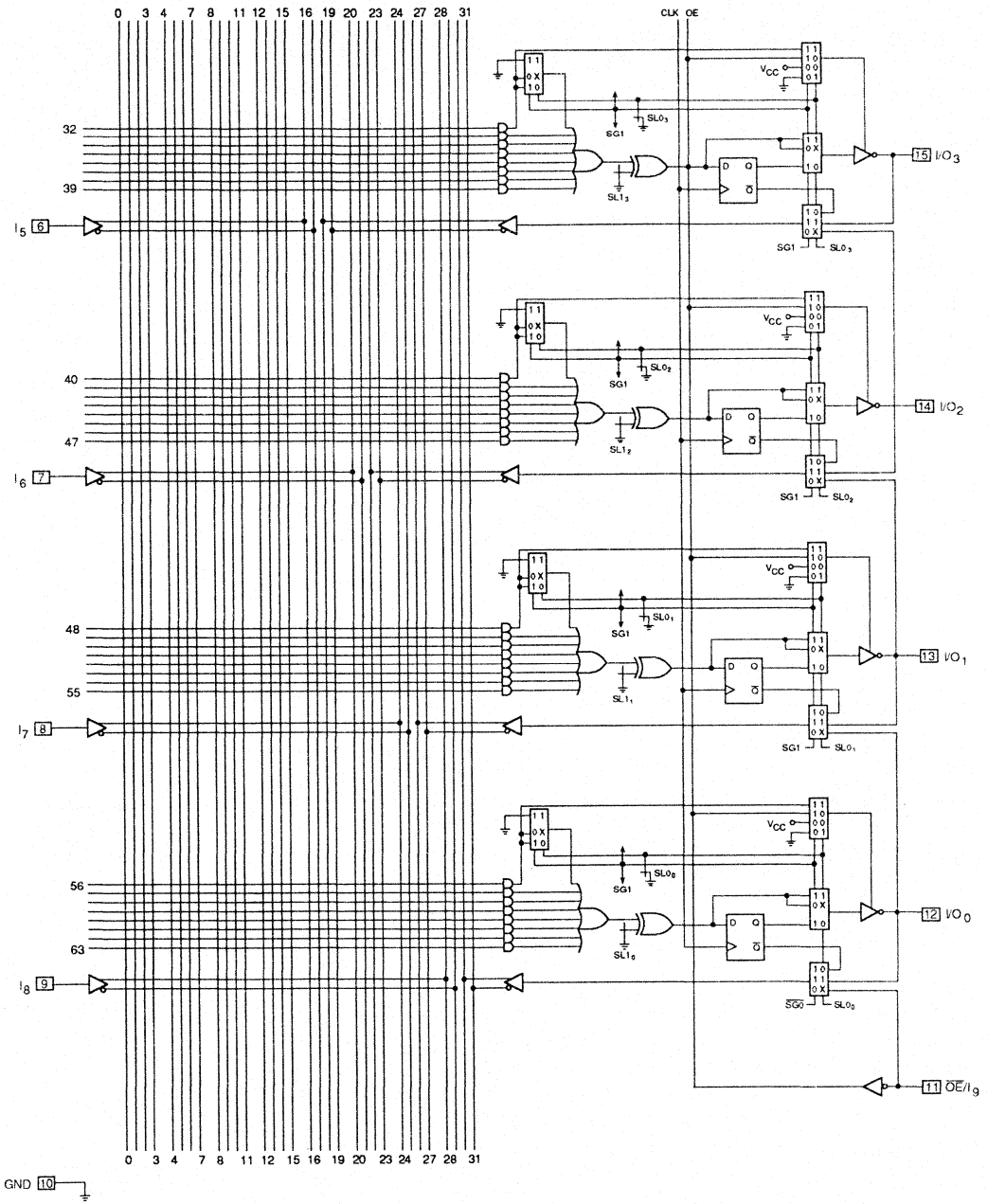
LOGIC DIAGRAM



12015-009A

Figure 6. PALCE16V8 Logic Diagram

LOGIC DIAGRAM (Continued)



12015-009A
Concluded

Figure 6. PALCE16V8 Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min.	-10 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input or Feedback to Clock			10		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{CF}	Clock to Feedback (Note 3)					ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	55.5		MHz
		Internal Feedback	$1/(t_S+t_{CF})$			MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA)	H		90	mA
		V_{CC} = Max., f = 15 MHz	Q		55	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{CF}	Clock to Feedback (Note 3)				8		10	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback	$1/(t_S+t_{CF})$	50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		90	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

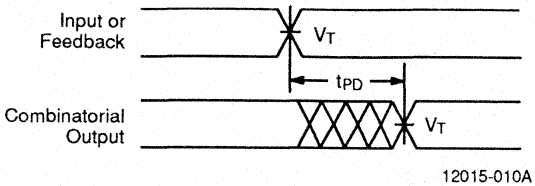
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input or Feedback to Clock			15		15		ns
t_H	Hold Time (Note 5)			0		0		ns
t_{CO}	Clock to Output				15		20	ns
t_{CF}	Clock to Feedback (Note 3)				13		18	ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	33.3		28.6		MHz
		Internal Feedback	$1/(t_S+t_{CF})$	35.7		30.3		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	41.7		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				20		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				20		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				20		25	ns

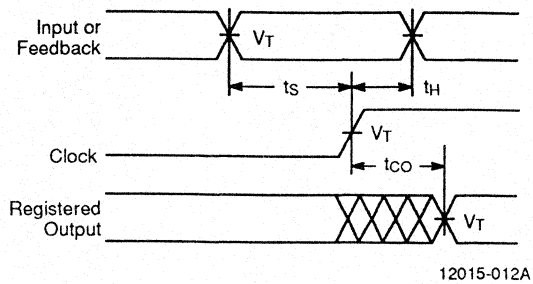
Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

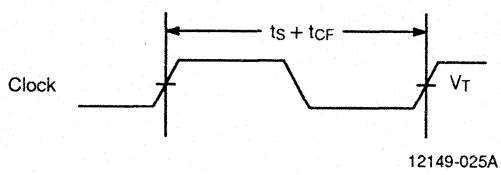
SWITCHING WAVEFORMS



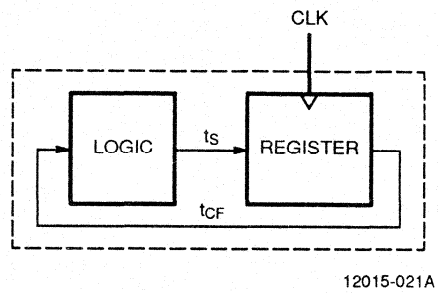
Combinatorial Output

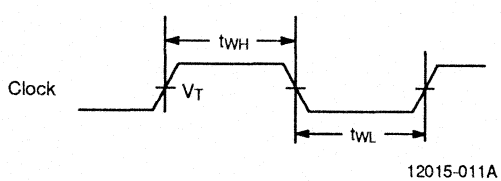


Registered Output

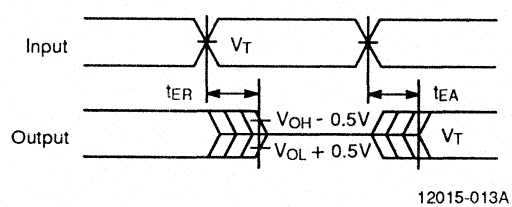


Clock to Feedback (f_{MAX} Internal)
See Path at Right

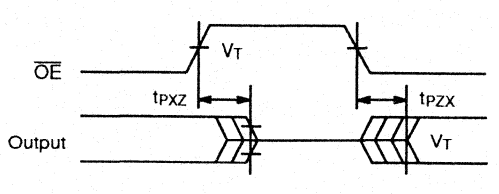




Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

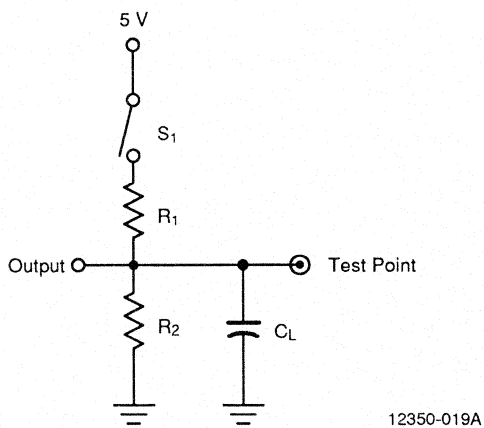
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

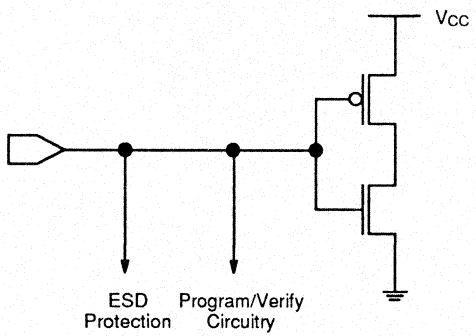
ENDURANCE CHARACTERISTICS

The PALCE16V8 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

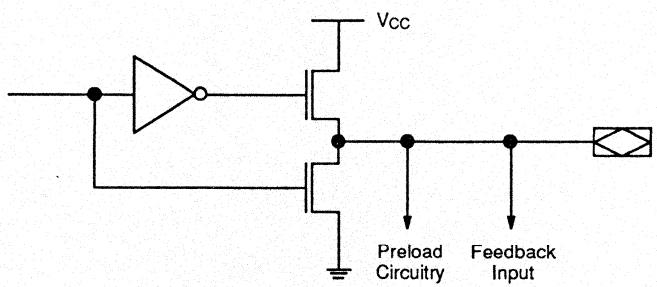
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

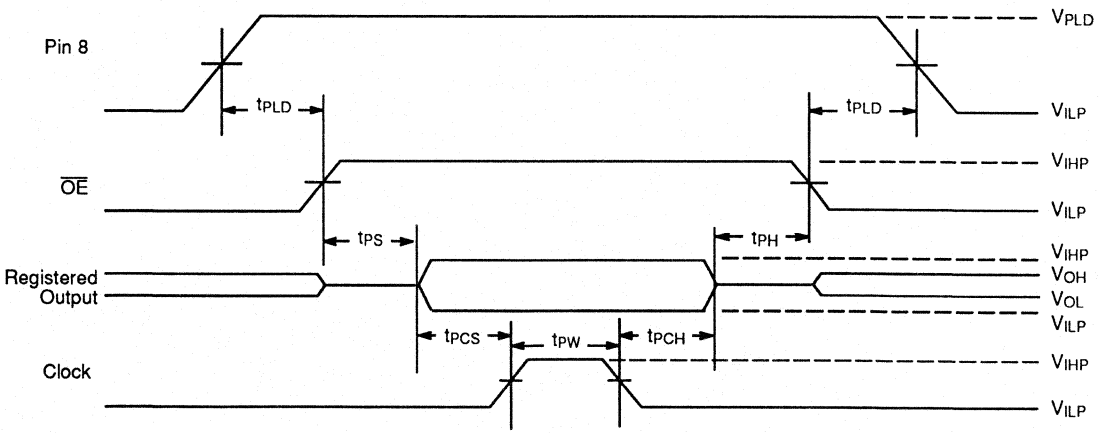
12197-013A

OUTPUT REGISTER PRELOAD

The Preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pin 8 to V_{PLD}.
3. Set $\overline{OE}$ HIGH.
4. Apply the desired value (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial output pins floating.
5. Clock pin 1 from V_{IL} to V_{IH}.
6. Remove V_{IL}/V_{IH} from all registered outputs.
7. Enable the output registers by lowering $\overline{OE}$.
8. Lower pin 8 to V_{IL}/V_{IH}.
9. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will be the inverse of the preload input.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_{PLD}	Setup and Hold Time from Preload (pin 8) to $\overline{OE}$	50	50		µs
t_{PS}	Setup Time from $\overline{OE}$ to Data	1	1		µs
t_{PH}	Hold Time from Data to $\overline{OE}$	1	1		µs
t_{PCS}	Setup Time from Data to Clock	1	1		µs
t_{PCH}	Hold Time from Clock to Data	1	1		µs
dV_r/dt	V_{PLD} Rising Slew Rate (pin 8)	10		100	V/µs
dV_f/dt	V_{PLD} Falling Slew Rate (pin 8)		2	3	V/µs
V_{PLD}	Super-level Input Voltage	9.5	10	10.5	V
V_{IHP}	High-level Input Voltage	2.4	5.0	5.5	V
V_{ILP}	Low-level Input Voltage	0	0	0.5	V



12015-015A

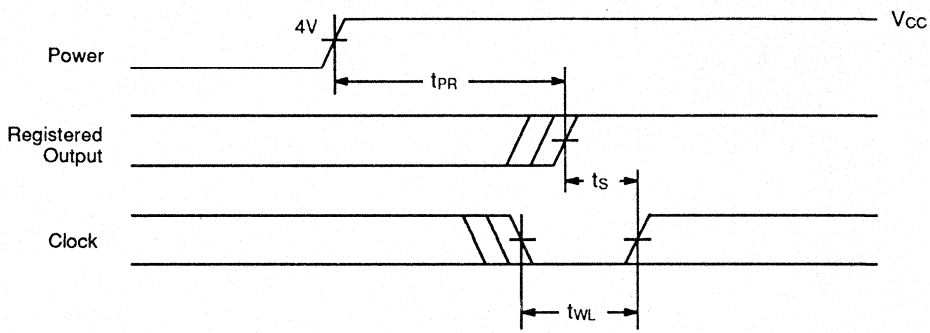
Output Register Preload Waveform

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

PALCE16V8Z-20

Zero Power EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Pin, function and fuse-map compatible with all 20-pin GAL® devices
- Electrically-erasable CMOS technology provides reconfigurable logic and full testability
- Zero-Power CMOS technology
  - 100 µA Standby Current
  - 20 ns propagation delay
- Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series
- Outputs programmable as registered or combinatorial in any combination
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Cost-effective 20-pin plastic DIP and PLCC packages
- Programmable on standard device programmers
- Supported by PALASM® software
- Fully tested for 100% programming and functional yields and high reliability

2

GENERAL DESCRIPTION

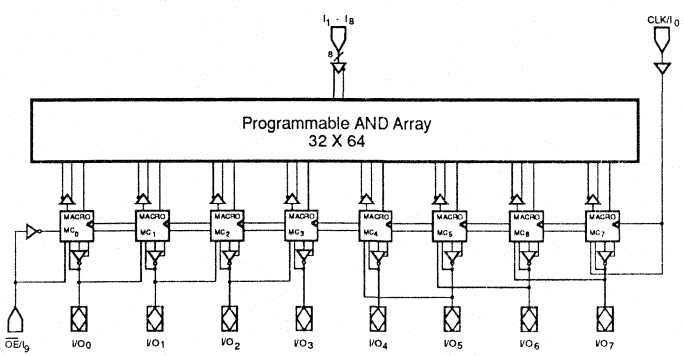
The PALCE16V8 is an advanced PAL® device built with zero-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 100 µA maximum standby current, the PALCE16V8Z allows battery powered operation for an extended period.

The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

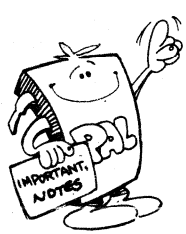
The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM



12467-001A

Publication # 13061 Rev. A Amendment/0
Issue Date: January 1990


IMPORTANT
NOTES

AmPAL18P8B/AL/A/L

20-pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 15 ns maximum propagation delay
- Universal combinatorial architecture
- Programmable output polarity
- Programmable replacement for high-speed TTL logic
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 20-pin DIP and 20-pin PLCC packages save space

GENERAL DESCRIPTION

The AmPAL18P8 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL18P8 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

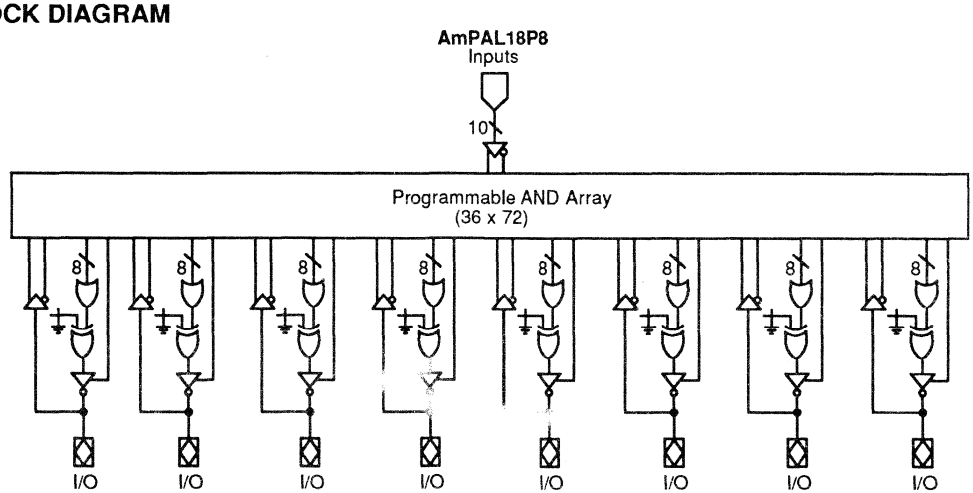
- Variable input/output pin ratio
- Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

2

BLOCK DIAGRAM



05799-001A

Publication # 05799 Rev. F Amendment /0
Issue Date: January 1990

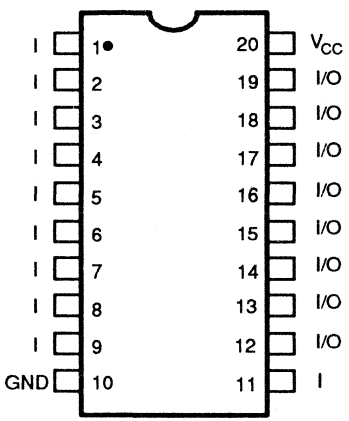
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max.)	I_{CC} mA (Max.)	I_{OL} mA (Min.)
Very High-Speed ("B") Versions	15	180	24
High-Speed ("A") Versions	25	180	24
High-Speed, Half-Power ("AL") Versions	25	90	24
Half-Power ("L") Versions	35	90	24

CONNECTION DIAGRAMS

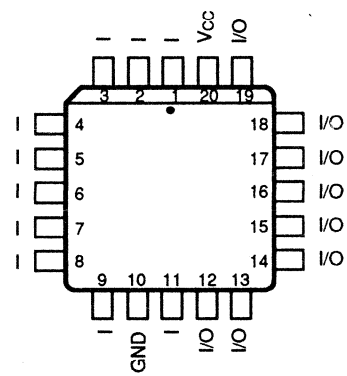
Top View

DIP



05799-002A

PLCC



Note:
Pin 1 is marked for orientation.

05799-003A

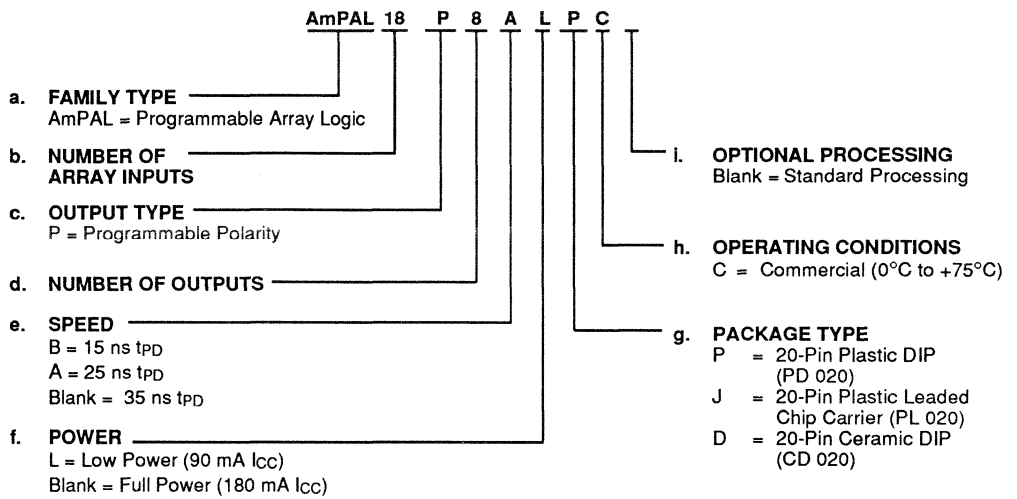
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Power**
g. **Package Type**
h. **Operating Conditions**
i. **Optional Processing**



Valid Combinations		
AmPAL18P8	B, AL, A, L	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL18P8 has ten dedicated input lines, and all eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts. Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL18P8 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

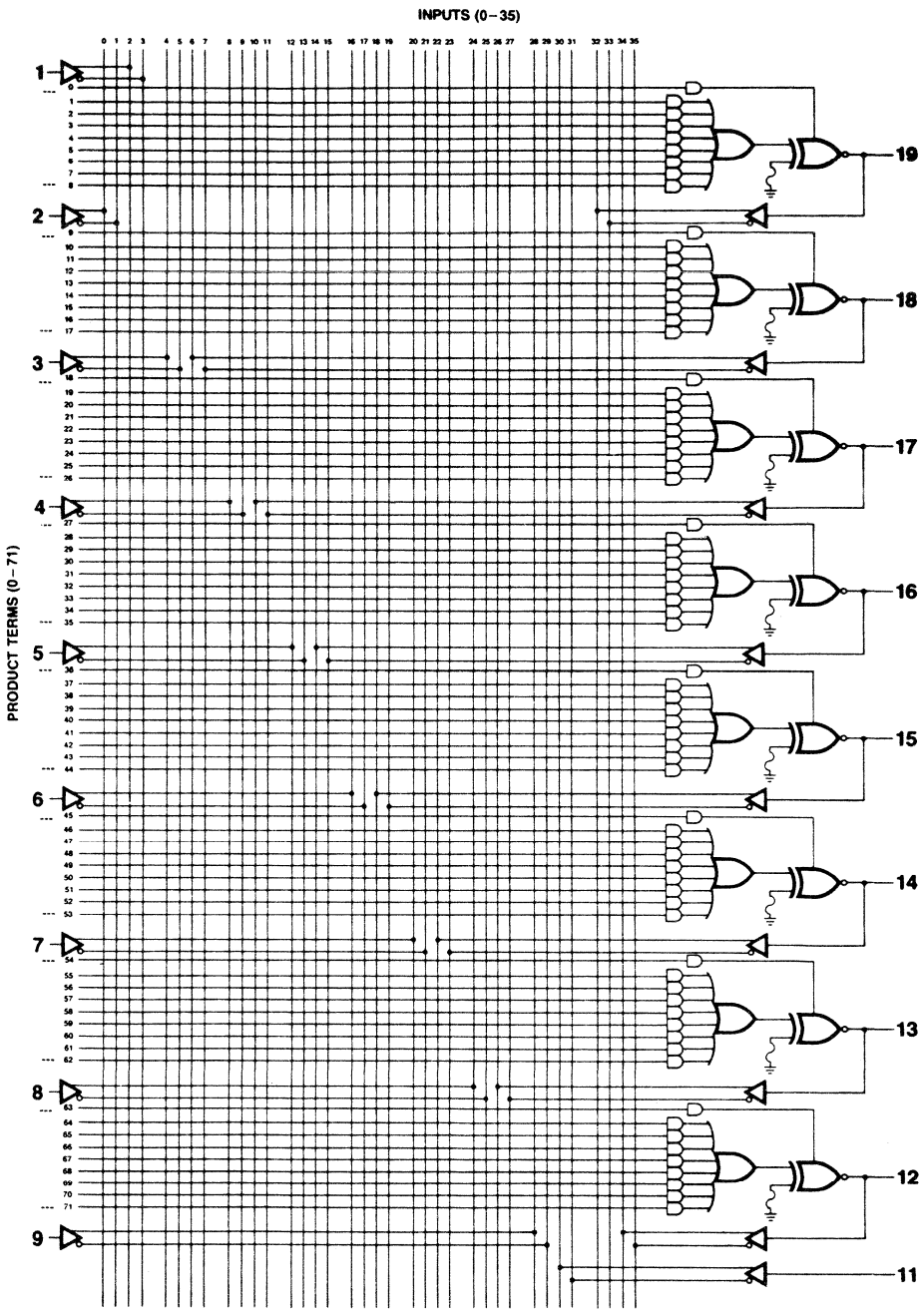
Quality and Testability

The AmPAL18P8 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL18P8 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM



LD000040

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to + 5.5 V
DC Input Current	–30 mA to +5 mA
DC I/O Pin Voltage	–0.5 V to V_{CC} Max.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–250	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	B, A		180	mA
			AL, L		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

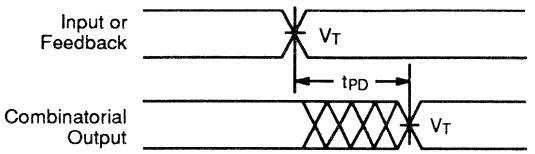
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		25		35	ns
t_{EA}	Input to Output Enable Using Product Term Control		15		25		35	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25		35	ns

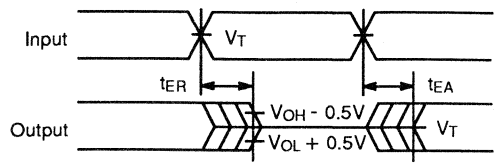
Note:

2. See Switching Test Circuit for test conditions.

SWITCHING WAVEFORMS



Combinatorial Output



Input to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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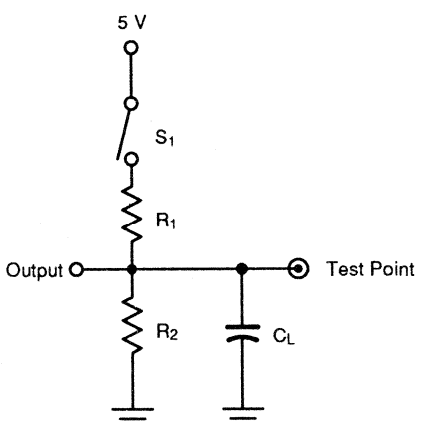
2

SWITCHING TEST CIRCUIT

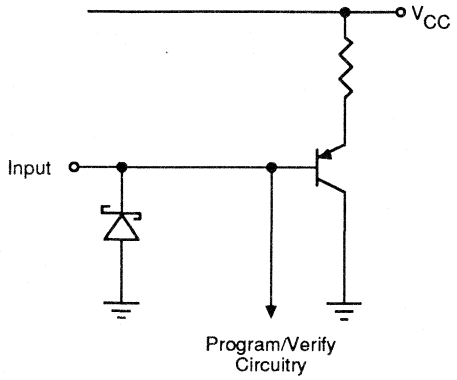


12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

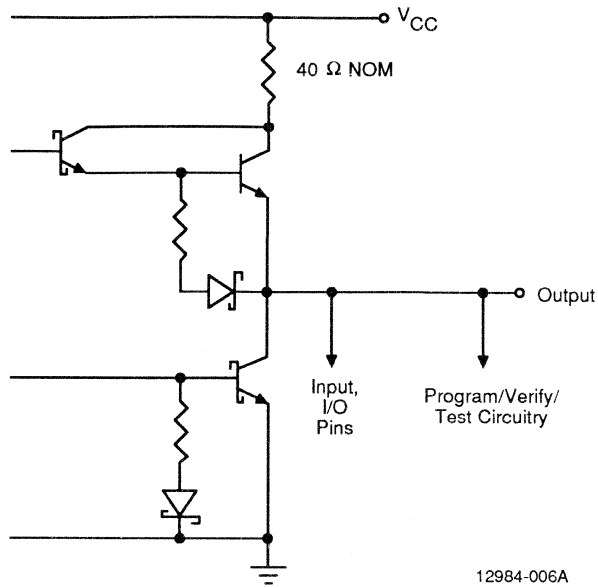
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



12350-020B

Typical Output



12984-006A

PAL20R8 Family

24-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns maximum propagation delay
- Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) is AMD's standard 24-pin PAL device family. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL20L8	14	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication # 10294 Rev. B Amendment /0
Issue Date: January 1990

PERFORMANCE OPTIONS

(Commercial)

Speed (t_{PD}, ns)	Power (I_{CC}, mA)		
	35	A-2	
	25	B-2	A
	15		B
	10		-10
	7.5		-7
		105	210

Note:

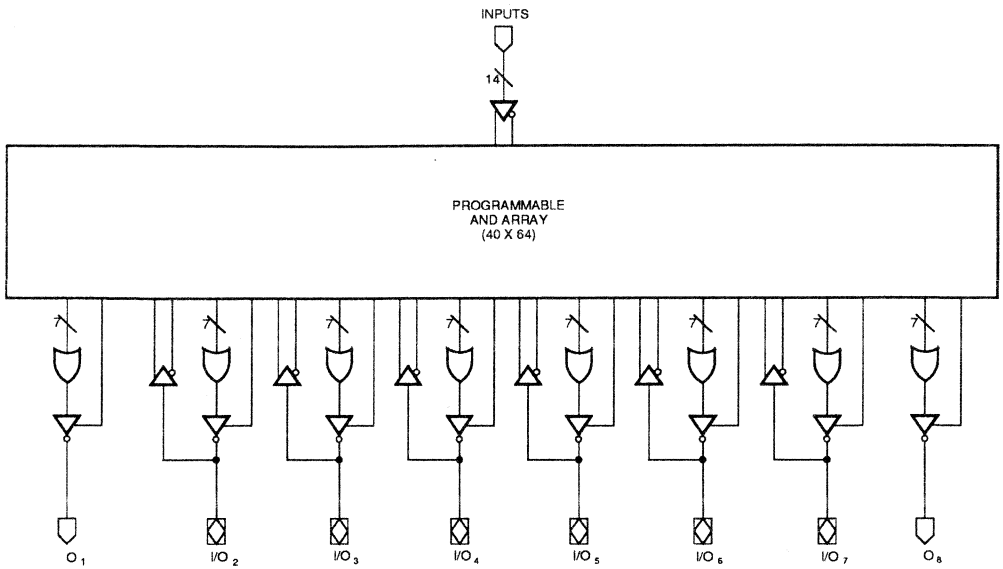
For low power and high speed, the EE CMOS PALCE20V8 can directly replace the PAL20R8 Family.

OPERATING RANGES

Commercial	Military
-7	-12
-10	-15
B (15 ns)	B (20 ns)
B-2 (25 ns)	
A (25 ns)	A (30 ns)
A-2 (35 ns)	A-2 (50 ns)

BLOCK DIAGRAMS

PAL20L8



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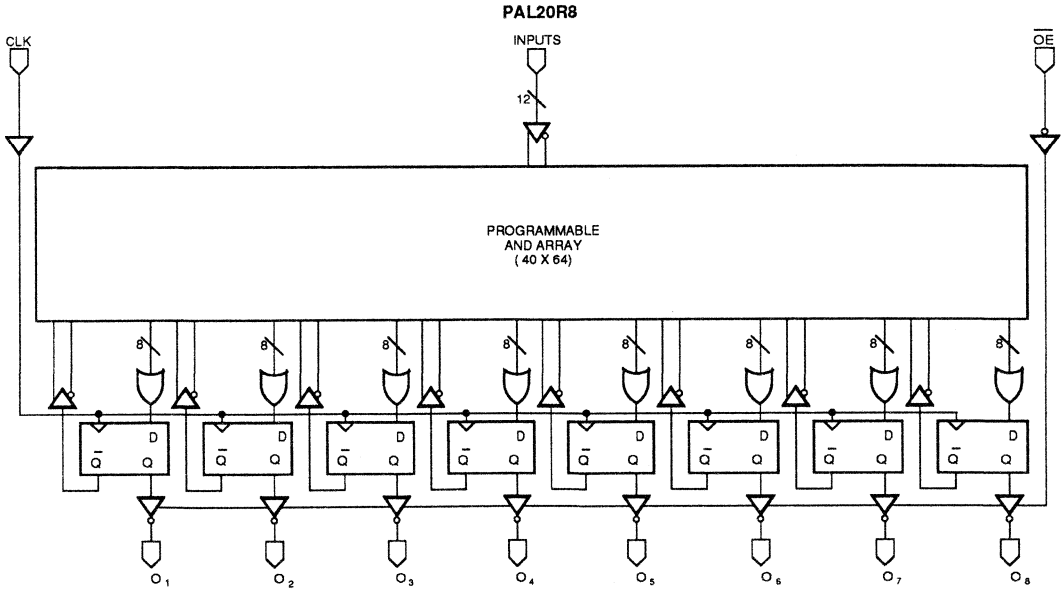
PAL20R8



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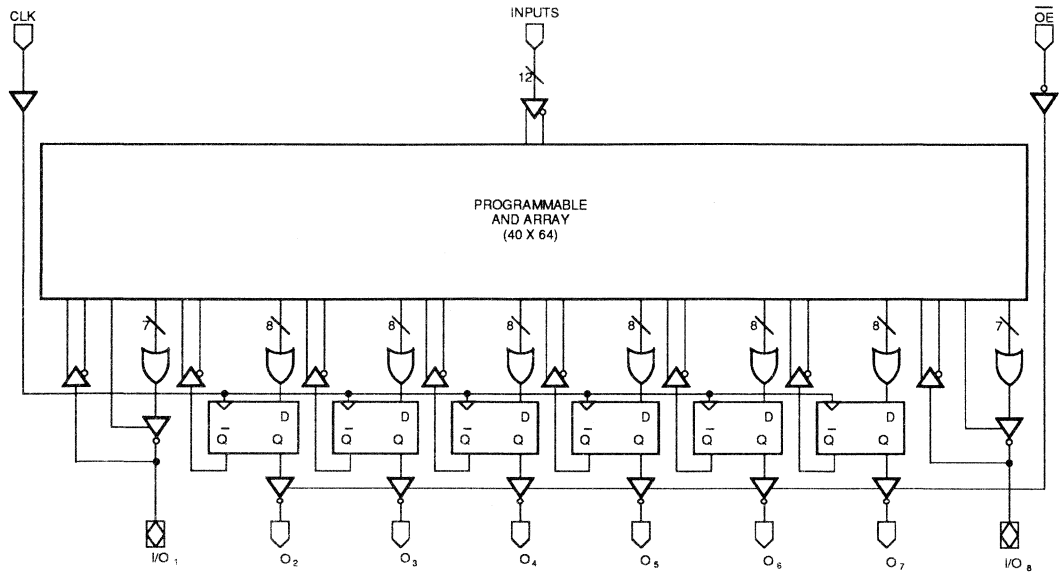
BLOCK DIAGRAMS

PAL20R6



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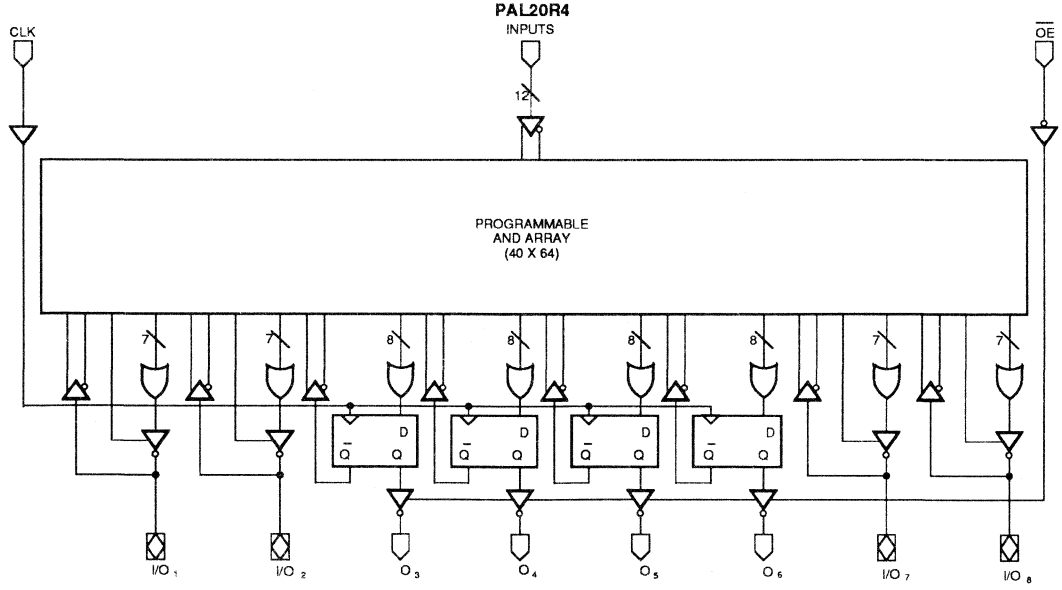
PAL20R4



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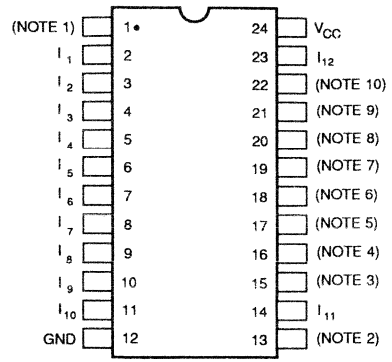
CONNECTION DIAGRAMS
Top View

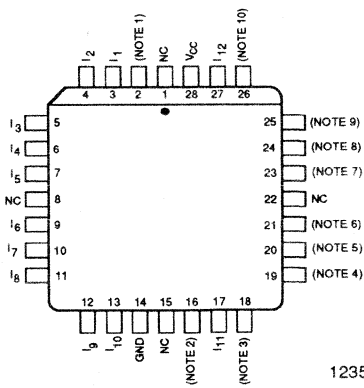
SKINNYDIP/FLATPACK



12350-005A

PLCC/LCC

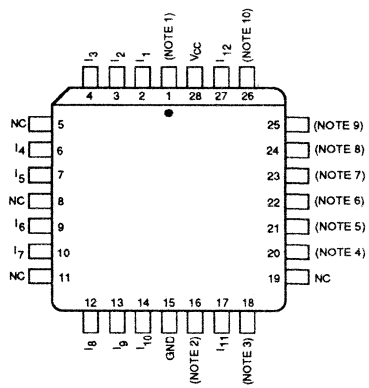
JEDEC: Applies to -7(-12 mil), -10(-15 mil), B-2 Series Only



12350-006A

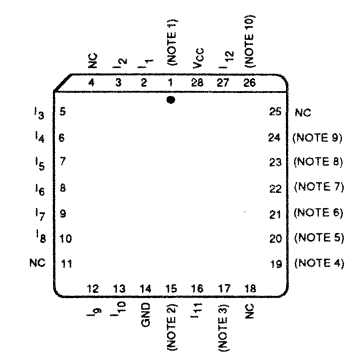
PLCC

Applies to B, A, A-2 Series Only



LCC

Applies to B, A, A-2 Series Only



Note:
Pin 1 is marked for orientation.

Note	20L8	20R8	20R6	20R4
1	I_0	CLK	CLK	CLK
2	I_{13}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

PIN DESIGNATIONS

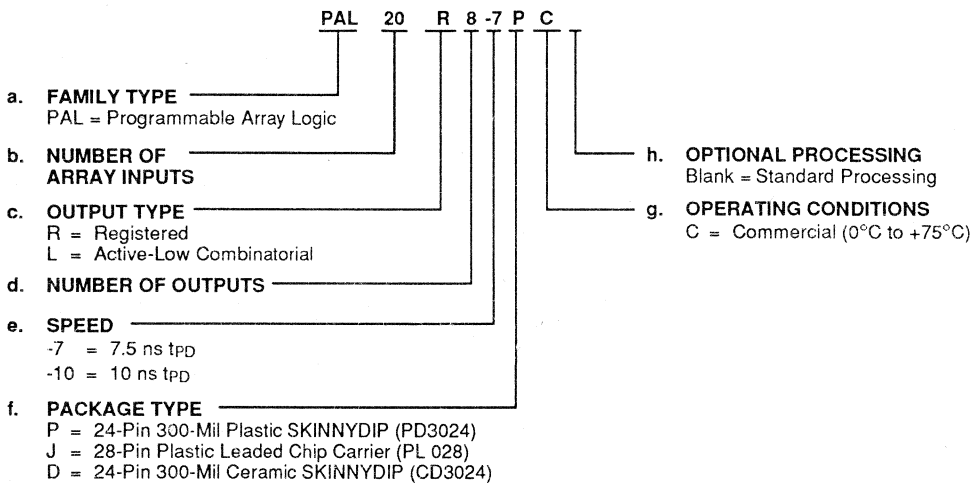
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products (AMD Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Package Type
g. Operating Conditions
h. Optional Processing



Valid Combinations		
PAL20L8	-7, -10	PC, JC, DC
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

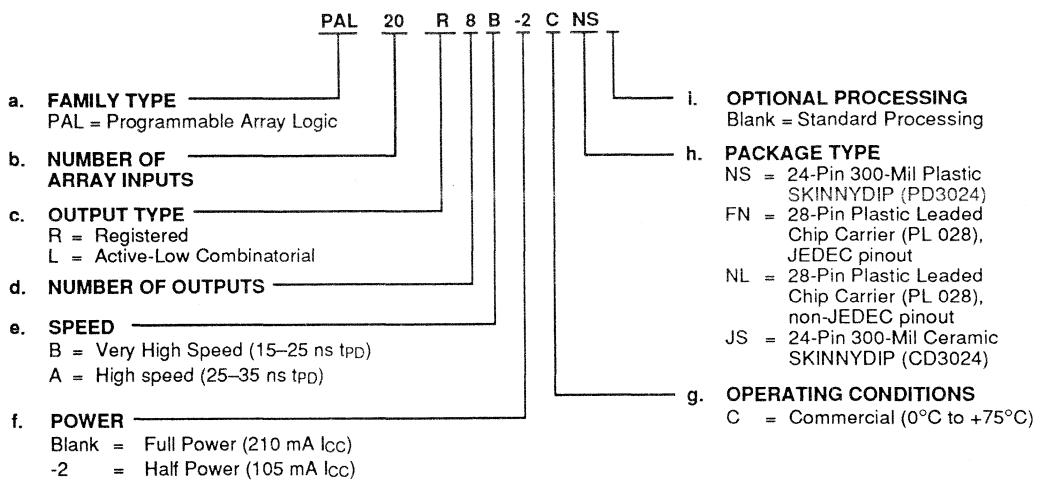
Note: Marked with AMD logo.

ORDERING INFORMATION

Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Power**
g. **Operating Conditions**
h. **Package Type**
i. **Optional Processing**



Valid Combinations		
PAL20L8,	B-2	CNS, CFN, CJS
PAL20R8, PAL20R6, PAL20R4	B, A, A-2	CNS, CNL, CJS

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

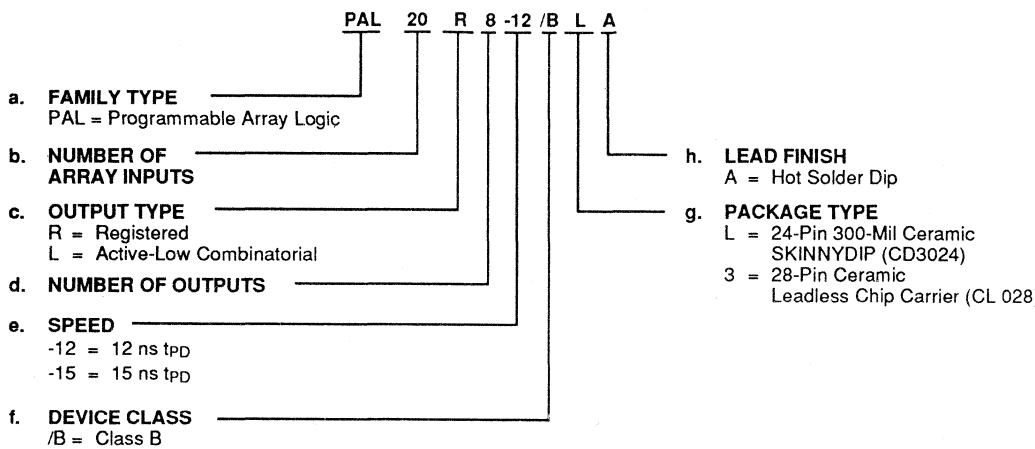
Note: Marked with MMI logo.

ORDERING INFORMATION

APL Products (AMD Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Device Class**
g. **Package Type**
h. **Lead Finish**



Valid Combinations		
PAL20L8	-12, -15	/BLA, /B3A
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

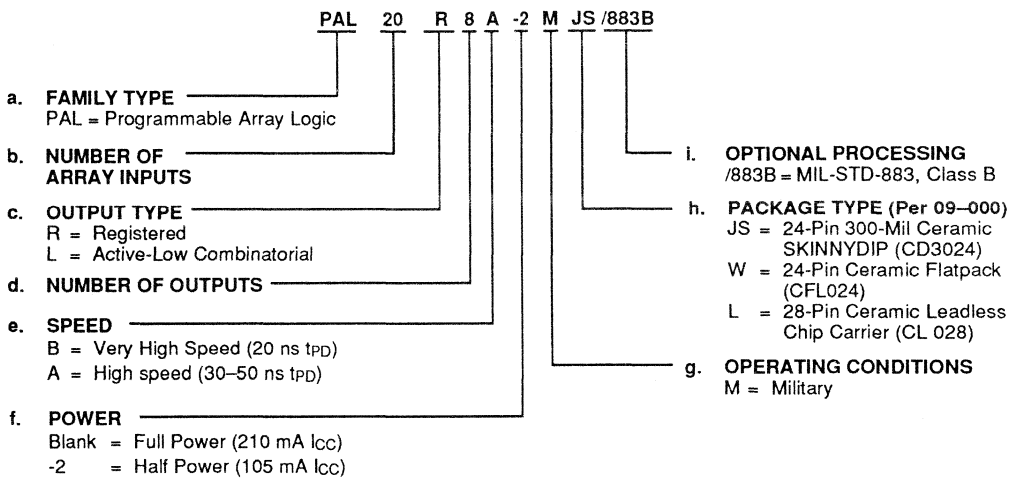
Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

ORDERING INFORMATION

APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Power**
g. **Operating Conditions**
h. **Package Type**
i. **Optional Processing**



Valid Combinations		
PAL20L8	B, A, A-2	MJS/883B, MW/883B, ML/883B
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 24-pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

Applies to -7 (-12 Mil), -10 (-15 Mil), Series Only

The register on the listed Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is unprogrammed. An exception is the -7 (-12 Mil) Series, where the array will read as if every fuse is programmed.

Pinouts

All members of the PAL20R8 Family have the same SKINNYDIP pinouts independent of technology, performance, and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. Newer devices and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The devices following this pinout are the -7, -10, and B-2 Series. Older devices retain their original pinouts, with no-connects on pins 5, 8, 11, and 19. These include the B, A, and A-2 Series.

PAL20R8 Family devices with the MMI marking indicate the PLCC pinout by the package designator: FN indicates JEDEC, and NL indicates non-JEDEC. Devices with the AMD marking all follow the JEDEC pinout.

Two different LCC pinouts are offered for military products. Newer devices and all future devices will follow the JEDEC pinout with no-connects on pins 1, 8, 15, and 22. These include the -12 and -15 Series. Older devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25. These include the B, A, and A-2 Series.

Series	Com'l PLCC No-connects	Mil LCC No-connects
-7, -10, B-2	1, 8, 15, 22 (JEDEC)	N/A
-12, -15	N/A	1, 8, 15, 22 (JEDEC)
B, A, A-2	5, 8, 11, 19	4, 11, 18, 25

Quality and Testability

The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

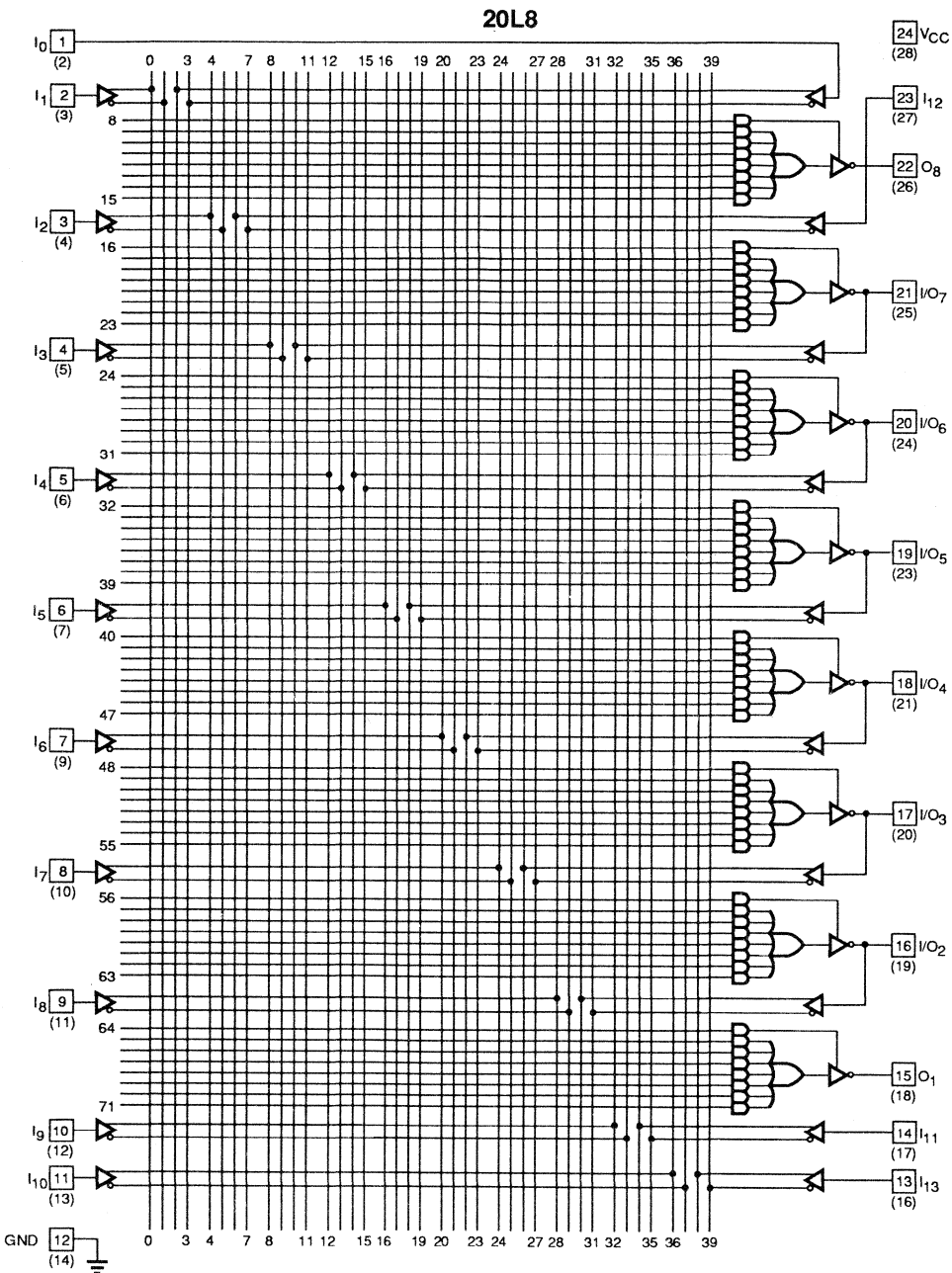
Technology

The high-speed -7 (-12 Mil) and -10 (-15 Mil) Series are fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for the -7 and TiW fuses for the -10. The B, B-2, A, and A-2 Series are fabricated with AMD's junction-isolated process, utilizing TiW fuses.

LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

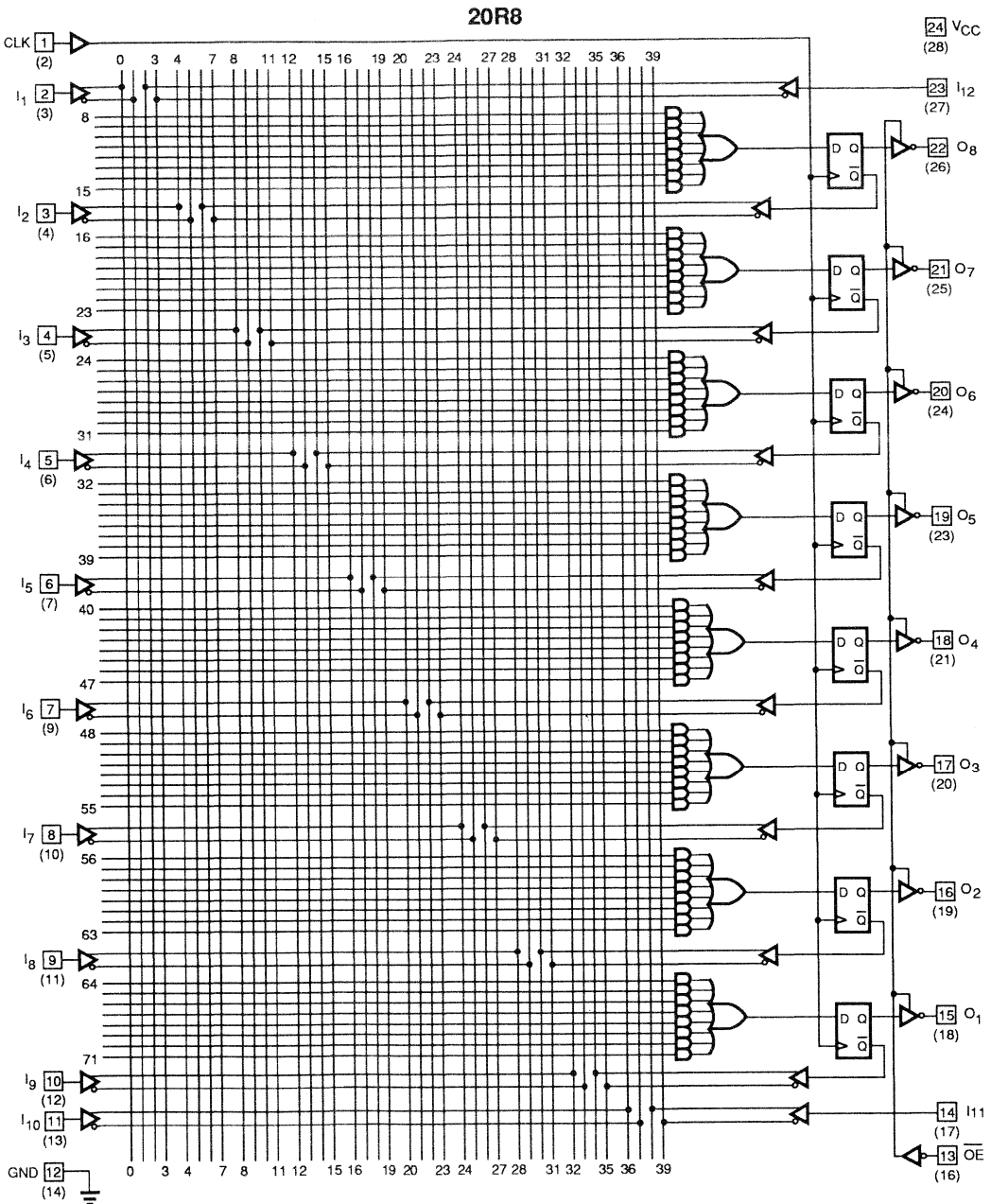


12350-007A

LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

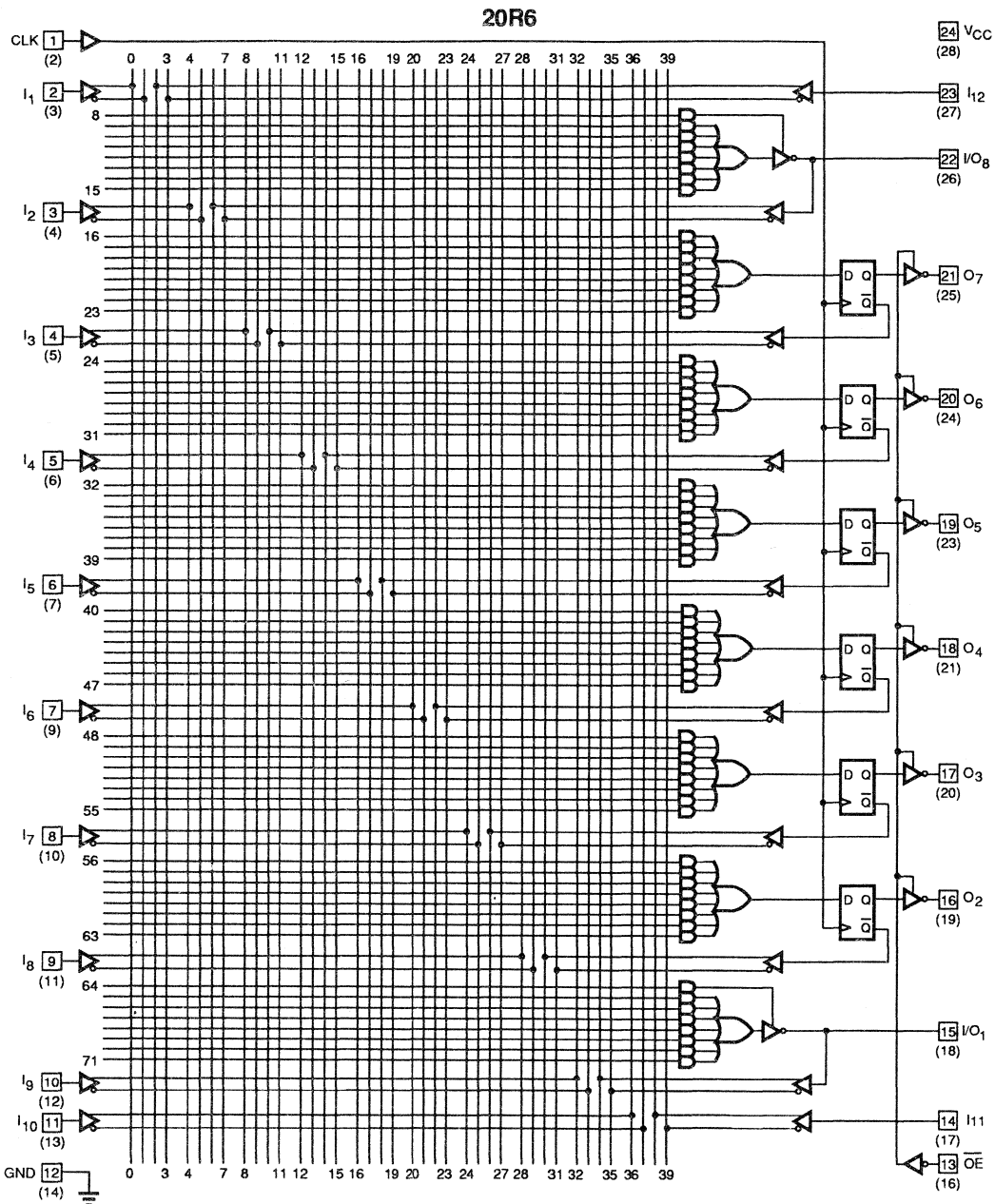


12350-008A

LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

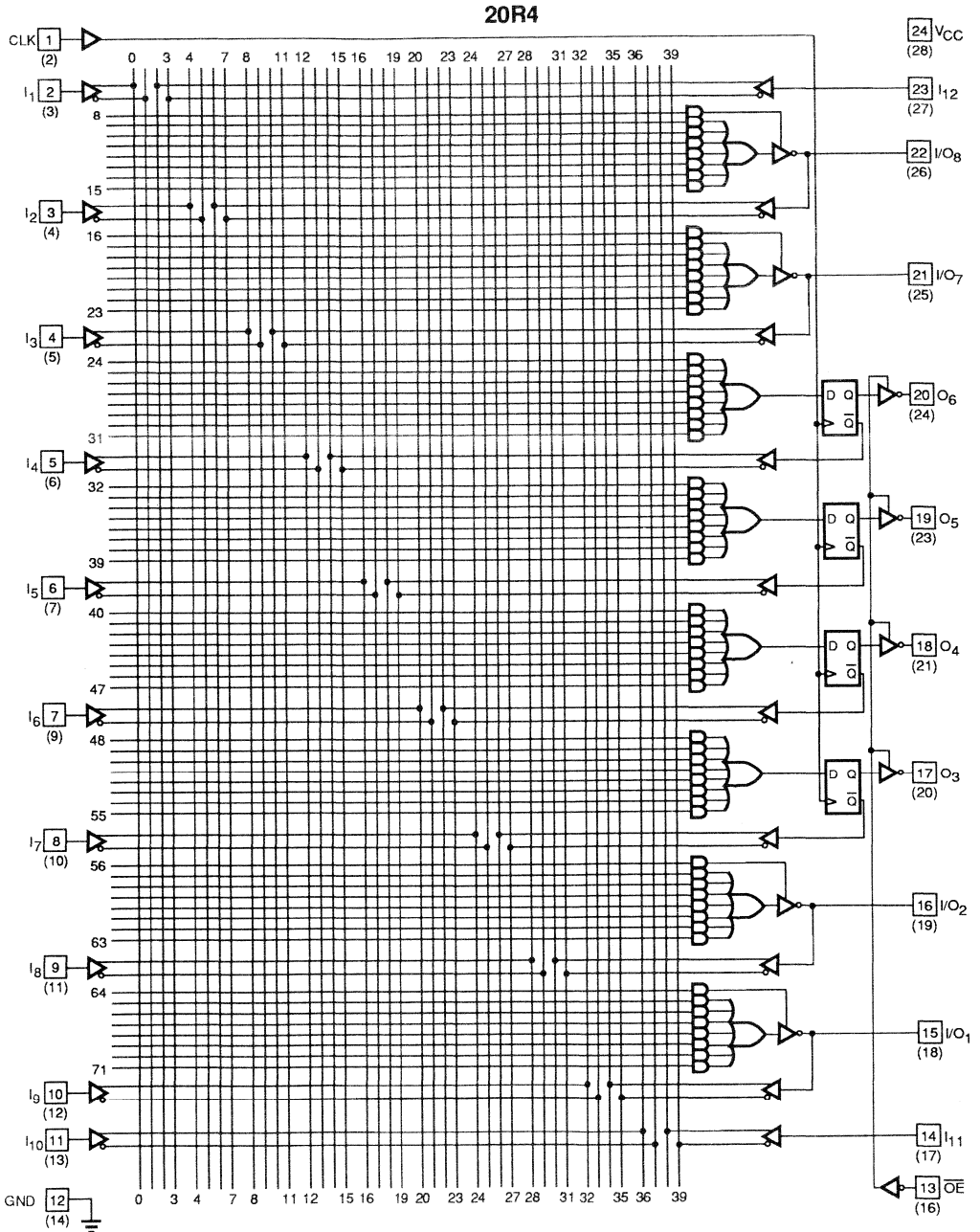


12350-009A

LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts



12350-010A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6	3	7.5	ns
		1 Output Switching		20R4	3	7	
t_S	Setup Time from Input or Feedback to Clock				7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	6.5	ns
t_{CF}	Clock to Feedback (Note 4)					3	ns
t_{SKEW}	Skew Between Registered Outputs (Note 5)			20R8, 20R6, 20R4		1	ns
t_{WL}	Clock Width	LOW			5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4	3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case (T_C) Temperature	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C , +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

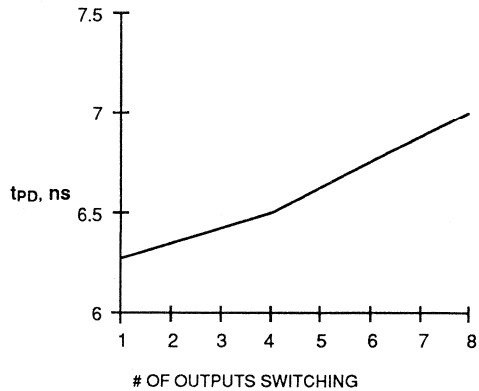
Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6	3	12.5	ns
		1 Output Switching		20R4	3	12	
t_S	Setup Time from Input or Feedback to Clock				12		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	11	ns
t_{CF}	Clock to Feedback (Note 4)					6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 5)					1	ns
t_{WL}	Clock Width	LOW		20R8, 20R6	10		ns
t_{WH}		HIGH		20R4	8		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$		43.4		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		54		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		55.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 7)				3	20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 7)				3	20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 7)			20L8, 20R6 20R4	3	20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 7)				3	20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f_{MAX} internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

MEASURED SWITCHING CHARACTERISTICS

V_{CC} = 5.25 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

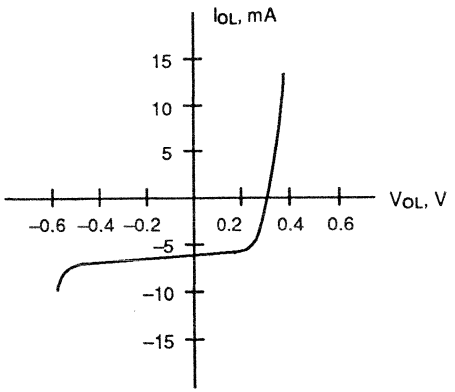
10294-005A

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

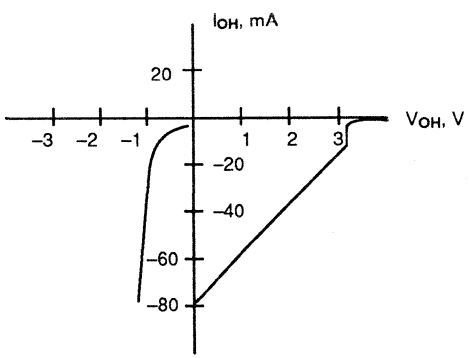
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



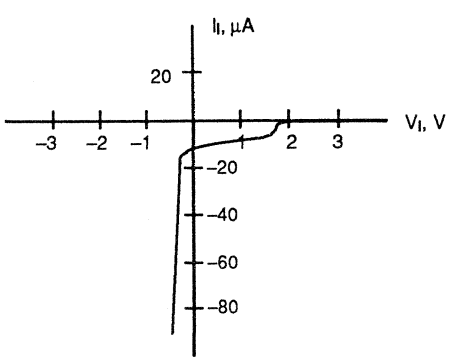
Output, LOW

10240-003A



Output, HIGH

10240-004A



Input

10240-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	12	pF
			T_A = 25°C	Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	8	ns
t_{CF}	Clock to Feedback (Note 4)					7	ns
t_{WL}	Clock Width	LOW			7		ns
t_{WH}		HIGH			7		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		55.5		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		71.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to + 5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	CLK, $\overline{OE}$	12	pF
				Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4	3	15	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	13	ns
t_{CF}	Clock to Feedback (Note 4)					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		35.7		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 6)				1	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 6)				1	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 6)			20L8, 20R6 20R4	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 6)				3	15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		15	ns
t_S	Setup Time from Input or Feedback to Clock				15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback			20R8		12	ns
t_{WL}	Clock Width	LOW		20R6	10		ns
t_{WH}		HIGH		20R4	12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		45		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					12	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6		18	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4		15	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to + 5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883 .

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					20	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock				25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{CF}	Clock to Feedback (Note 2)			20R8, 20R6		10	ns
t_{WL}	Clock Width	LOW		20R4	15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6		25	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4		25	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f_{MAX} internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{CF}	Clock to Feedback (Note 2)					10	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f_{MAX} internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883 .

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6 20R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					30	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		35	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	35		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		16		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					25	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6		35	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4		35	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA $V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

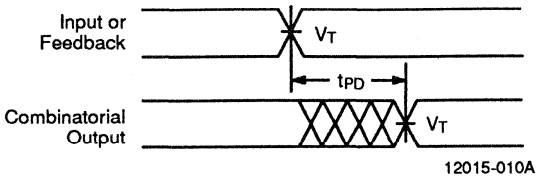
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		50	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	50		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		13.3		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6 20R4		45	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					45	ns

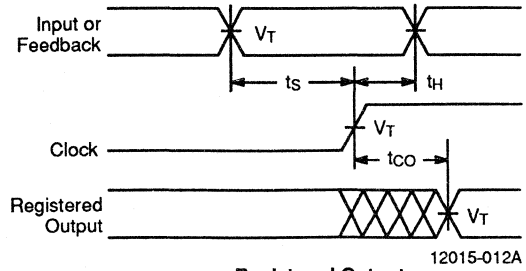
Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

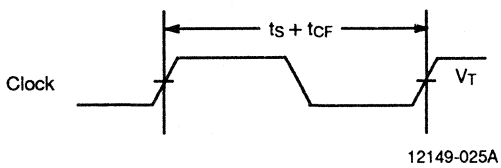
SWITCHING WAVEFORMS



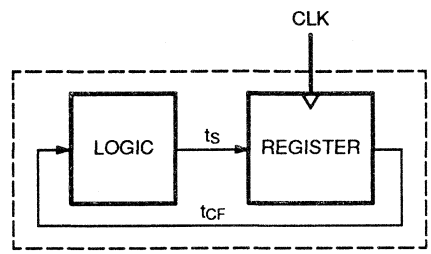
Combinatorial Output

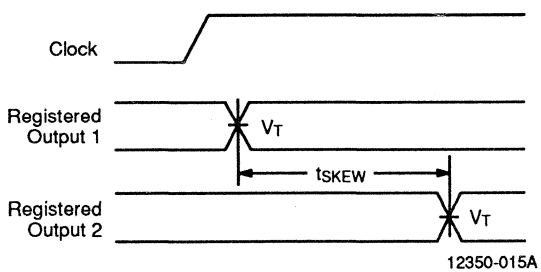


Registered Output

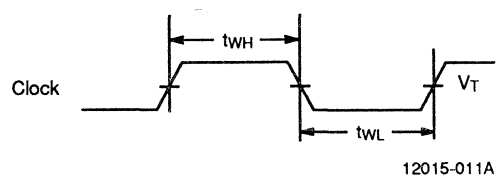


Clock to Feedback (f_{MAX} Internal)
See Path at Right

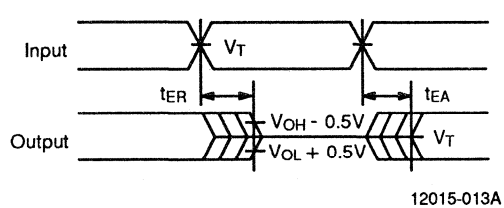




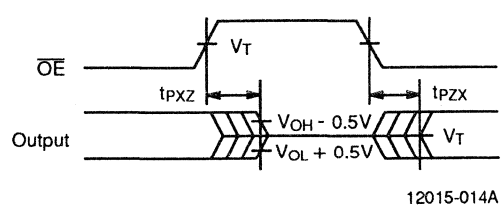
Registered Output Skew for Outputs Switching in the Same Direction



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.
   (2–4 ns for -7 (-12 Mil) and -10 (-15 Mil) Series)

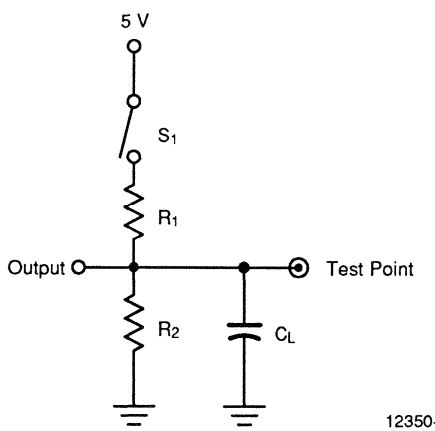
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

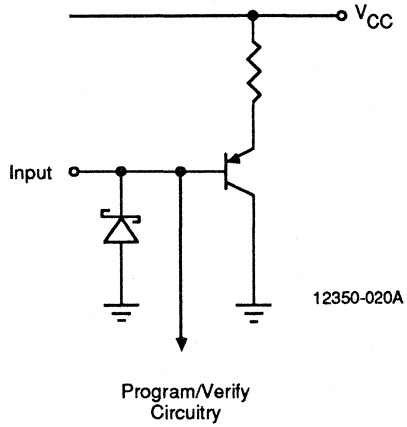


12350-019A

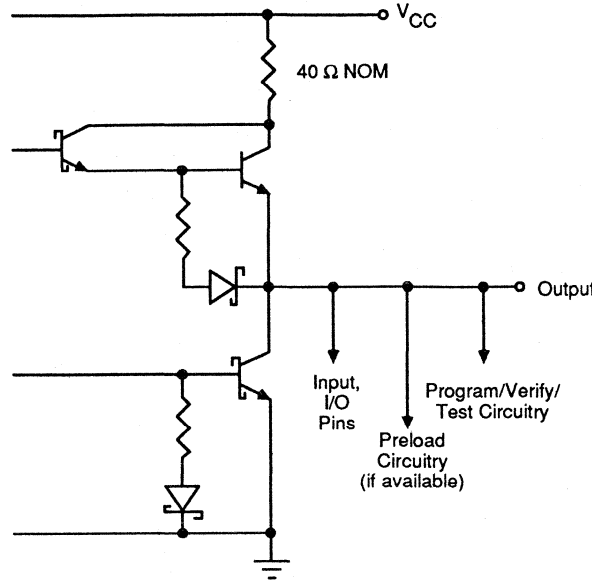
Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output



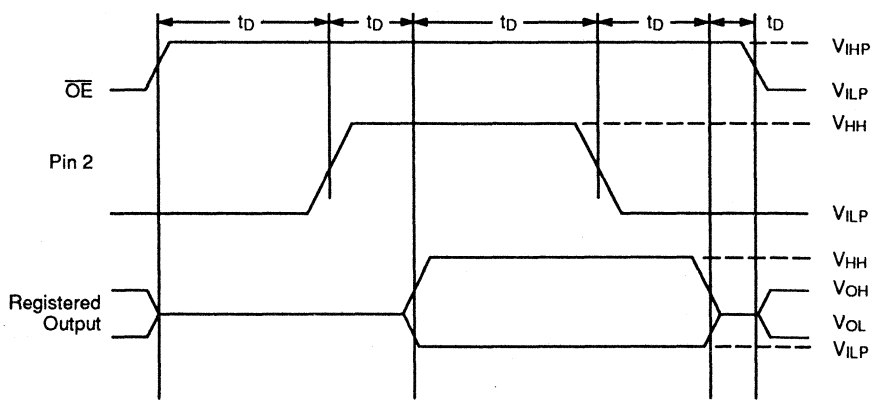
OUTPUT REGISTER PRELOAD

Applies to -7 (-12 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Raise pin 2 to V_{HH} to enter preload mode.
4. Apply either V_{HH} or V_{ILP} to all registered outputs. Use V_{HH} to preload a LOW in the flip-flop; use V_{ILP} to preload a HIGH in the flip-flop. Leave combinatorial outputs floating.
5. Lower pin 2 to V_{ILP}.
6. Remove V_{ILP}/V_{HH} from all registered output pins.
7. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	10	11	12	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload	5.4	5.7	6.0	V
t_D	Delay time	100	200	1000	ns



10294-003A

Output Register Preload Waveform

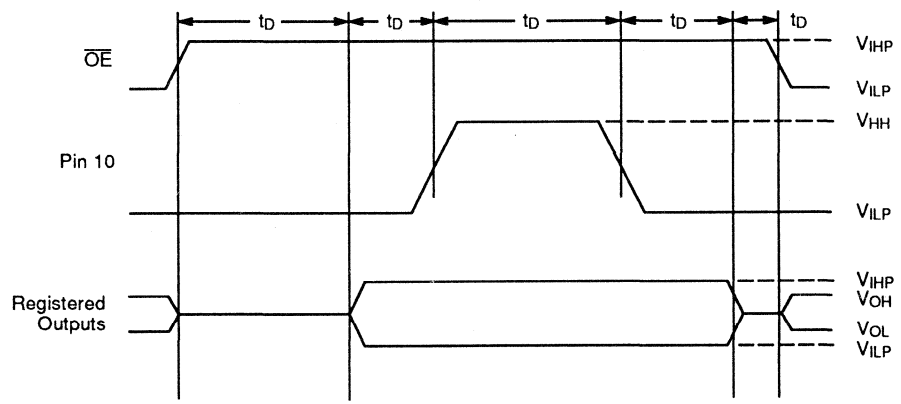
OUTPUT REGISTER PRELOAD

Applies to -10 (-15 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 4.5 V.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
4. Pulse pin 10 to V_{HH}, then back to 0 V.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
7. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19	20	21	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns



10294-004A

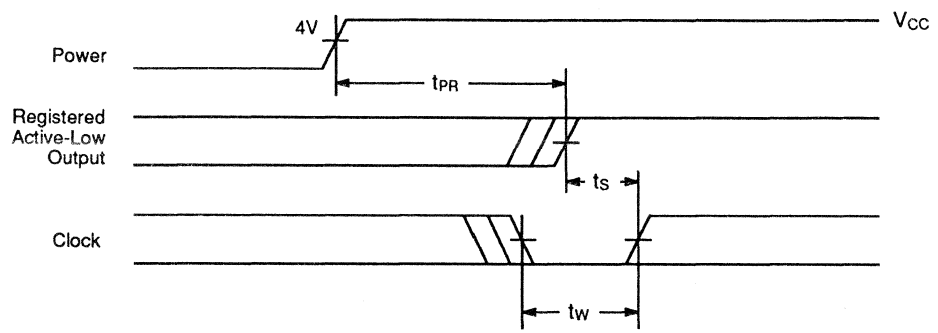
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

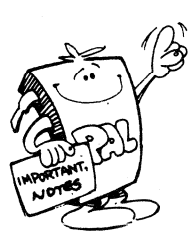
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform


IMPORTANT
NOTES

PAL20RA10/-20

24-pin Asynchronous TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 20 ns maximum propagation delay and 30 MHz f_{MAX}
- Individually programmable asynchronous clock, preset, reset, and enable
- Registered or combinatorial outputs
- Programmable polarity
- Programmable replacement for high-speed TTL logic
- TTL-level register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20RA10 offers asynchronous clocking for each of the ten flip-flops in the device. The ten macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PAL20RA10 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

The PAL20RA10 utilizes Advanced Micro Devices' advanced oxide- and junction-isolated bipolar processes and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL20RA10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

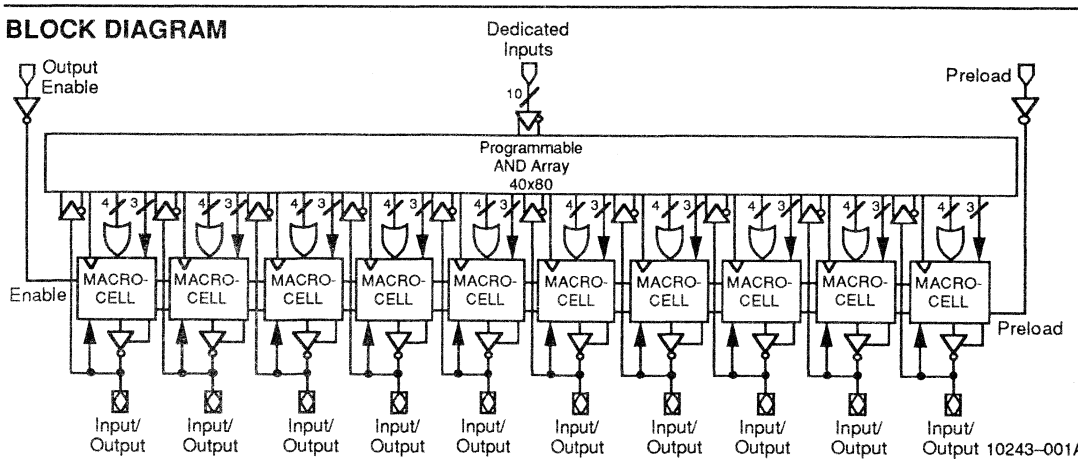
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers.

2

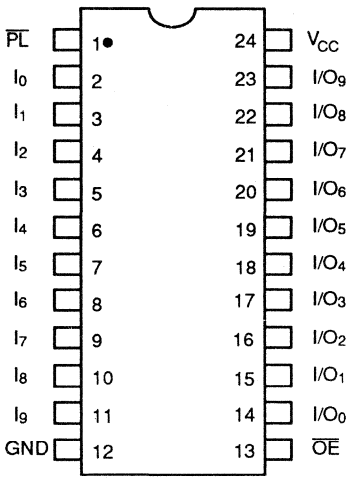
BLOCK DIAGRAM



Publication # 10243 Rev. C Amendment /0
Issue Date: January 1990

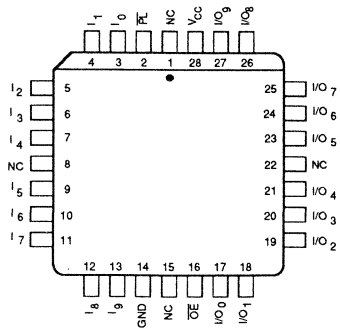
CONNECTION DIAGRAMS
Top Views

SKINNYDIP/FLATPACK



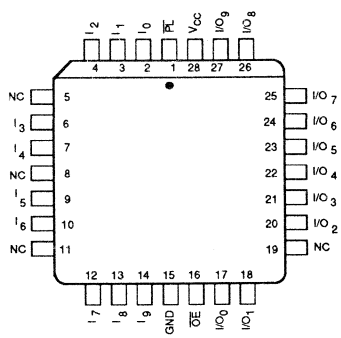
12350–005A

PLCC (-20 only)



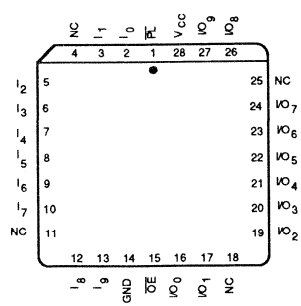
10243–003A

PLCC (std only)



10243–004A

LCC



10243–005A

Note:
Pin 1 is marked for orientation

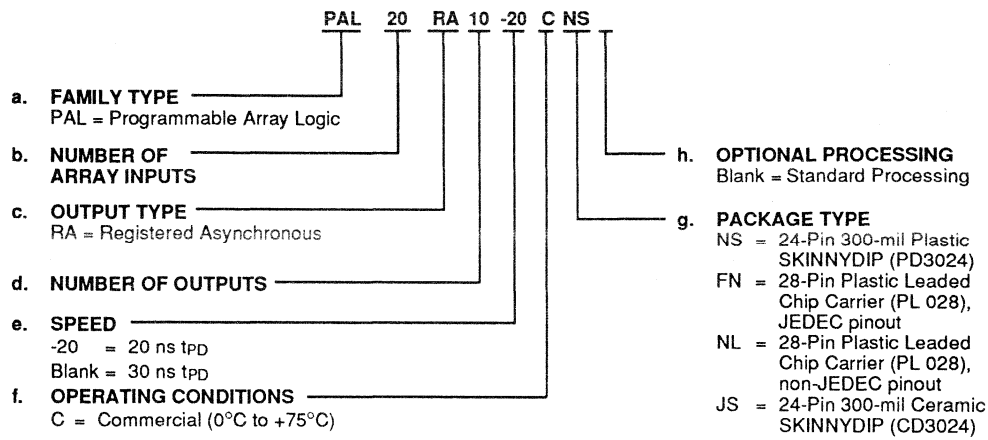
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
$\overline{OE}$	Output Enable
$\overline{PL}$	Preload
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Operating Conditions**
g. **Package Type**
h. **Optional Processing**



Valid Combinations	
PAL20RA10-20	CNS, CFN, CJS
PAL20RA10	CNS, CNL, CJS

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

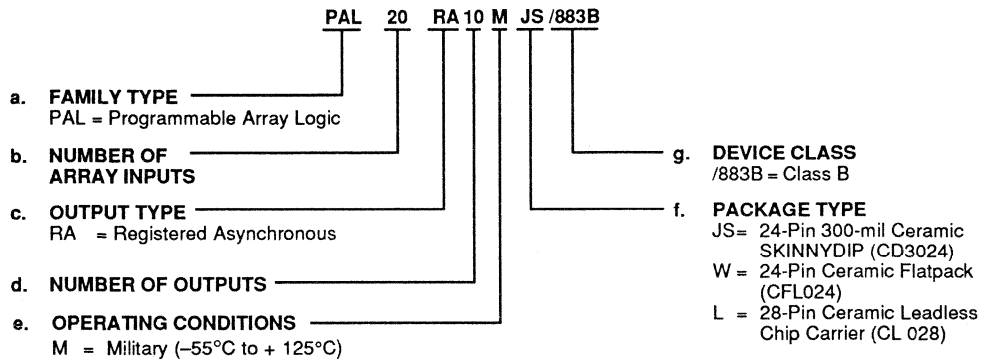
Note: Marked with MMI logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Operating Conditions
f. Package Type
g. Device Class



Valid Combinations	
PAL20RA10	MJS/883B, MW/883B, ML/883B

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

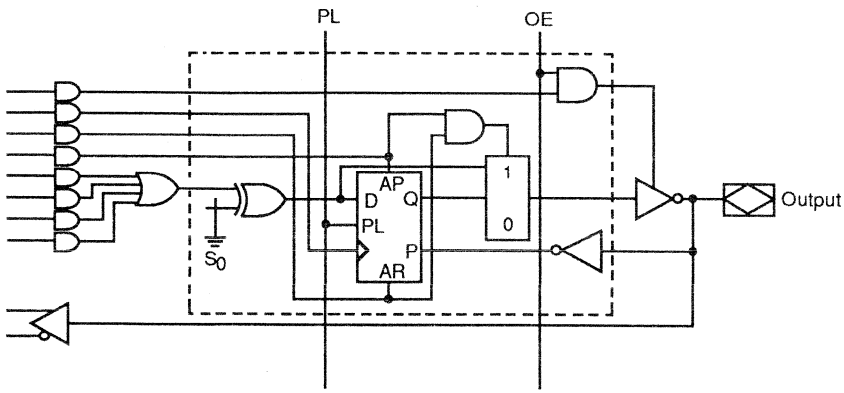
Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.



10232–004A

Figure 1. PAL20RA10 Macrocell

FUNCTIONAL DESCRIPTION

The PAL20RA10 has ten dedicated input lines and ten programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 13 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PAL20RA10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

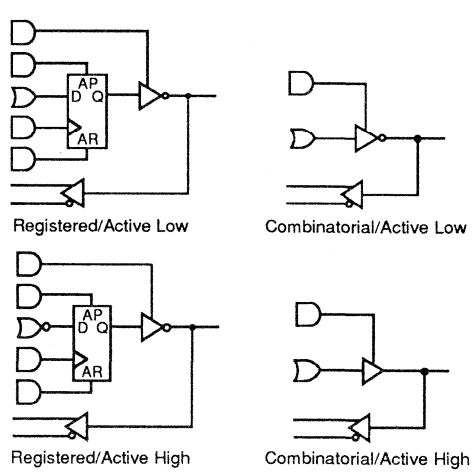
In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes a logic 1. If the reset product line is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed and the output becomes combinatorial. Otherwise, the output is from the register. Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flop-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.



10232–005A

Figure 2. Macrocell Configurations

Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Fuse

A security fuse is also provided to prevent unauthorized copying of PAL device patterns. Once the fuse is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every fuse is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer.

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PAL20RA10 logic diagram. When the output polarity fuse is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity fuse is intact, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming

The PAL20RA10 can be programmed on standard logic programmers. Programmers approved by Advanced Micro Devices are listed in the Programmer Reference Guide.

Register Preload

The register on the PAL20RA10/20 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transistions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function.

Pinouts

All PAL20RA10 devices have the same SKINNYDIP pinouts independent of performance and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. The PAL20RA10-20 and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The older, standard PAL20RA10 devices retain their original pinouts with no-connects on pins 5, 8, 11, and 19.

PAL20RA10 devices with the MMI marking indicate the PLCC pinout by the package designator: FN indicates JEDEC, and NL indicates non-JEDEC.

A different LCC pinout is offered for the military PAL20RA10. Older devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25.

Series	Com'l PLCC No-connects	Mil LCC No-connects
-20	1, 8, 15, 22 (JEDEC)	N/A
std.	5, 8, 11, 19	4, 11, 18, 25

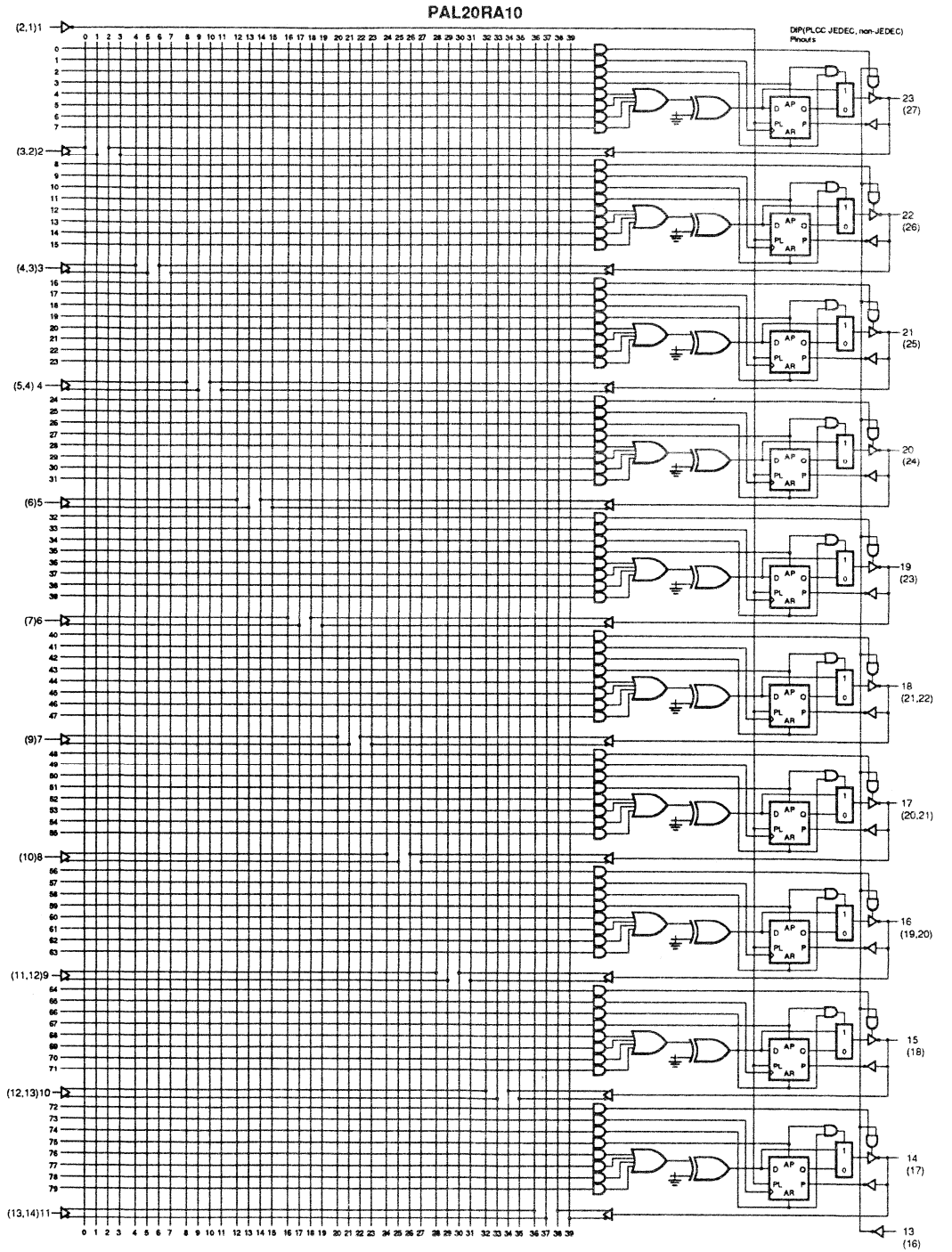
Quality and Testability

The PAL20RA10-20 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PAL20RA10-20 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses. The standard PAL20RA10 is fabricated with AMD's junction-isolated process, utilizing TiW fuses.

LOGIC DIAGRAM
DIP (PLCC JEDEC, non-JEDEC) Pinouts, see Connection Diagrams for LCC Pinout



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
DC Current into Outputs (-20 only)	16 mA
Static Discharge Voltage (-20 only)	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1) (-20 only)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Inputs	V_{IN} = 2.0 V	V_{CC} = 5.0 V	5	pF
		CLK, $\overline{OE}$		T_A = +25°C	9	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min. (Note 3)	-20 Max.	Std Min. (Note 3)	Std Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output	Active Low			20		30	ns
		Active High			20		35	ns
t_S	Setup Time from Input or Feedback to Clock			13		20		ns
t_H	Hold Time	Active Low		5		10		ns
		Active High		5		0		ns
t_{CO}	Clock to Output or Feedback			5	20	10	30	ns
t_{AP}	Asynchronous Preset to Registered Output				20		35	ns
t_{APW}	Asynchronous Preset Width			20		20		ns
t_{AR}	Asynchronous Reset to Registered Output				25		40	ns
t_{ARW}	Asynchronous Reset Width			20		20		ns
t_{WL}	Clock Width	LOW		14		20		ns
t_{WH}		HIGH		14		20		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	30		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	36		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				20		30	ns
t_{ER}	Input to Output Disable Using Product Term Control				20		30	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C , +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

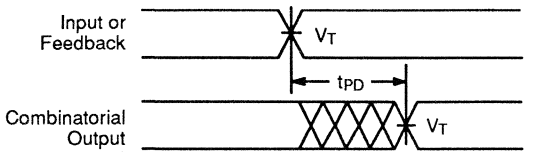
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description			Standard Min.	Standard Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output	Active Low			35	ns
		Active High			40	ns
t_S	Setup Time from Input or Feedback to Clock			25		ns
t_H	Hold Time	Active Low		10		ns
		Active High		0		ns
t_{CO}	Clock to Output or Feedback				35	ns
t_{AP}	Asynchronous Preset to Registered Output				40	ns
t_{APW}	Asynchronous Preset Width			25		ns
t_{AR}	Asynchronous Reset to Registered Output				55	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{WL}	Clock Width	LOW		25		ns
t_{WH}		HIGH		25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	16.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				35	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				35	ns

Notes:

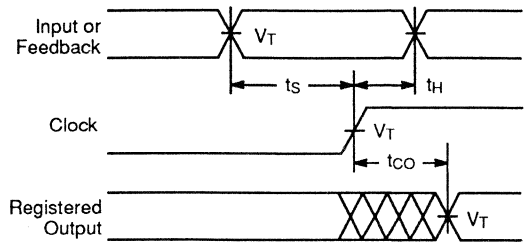
1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

SWITCHING WAVEFORMS



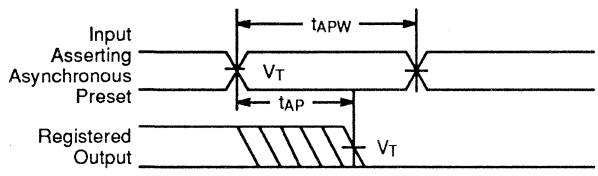
12015-010A

Combinatorial Output



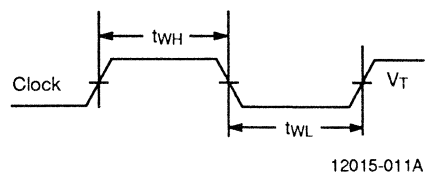
12015-012A

Registered Output



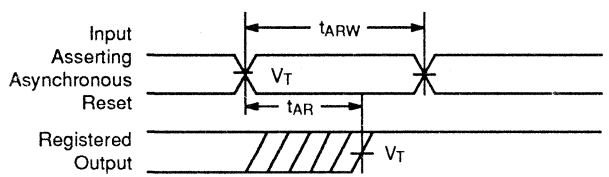
10232-007A

Asynchronous Preset



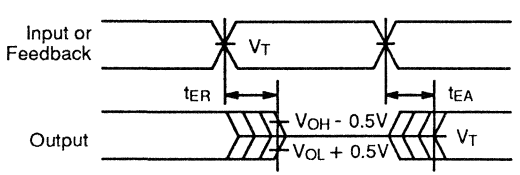
12015-011A

Clock Width



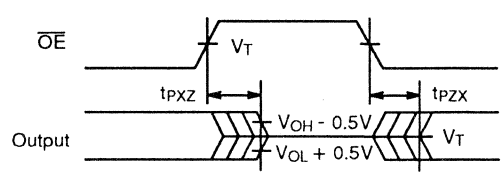
10232-009A

Asynchronous Reset



10232-008A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

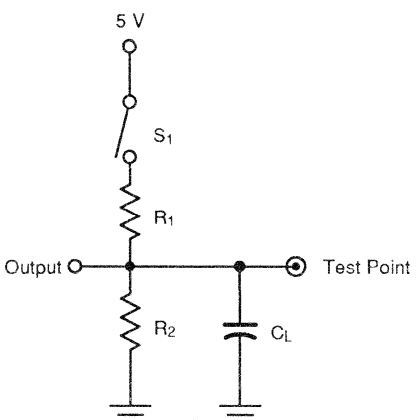
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

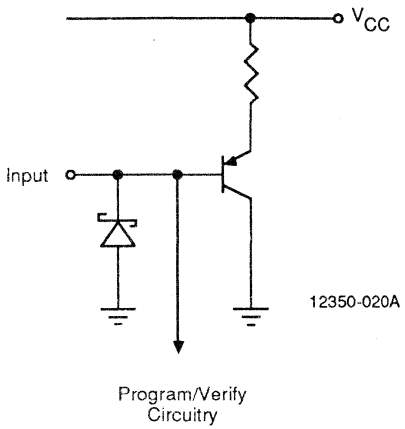


12350-019A

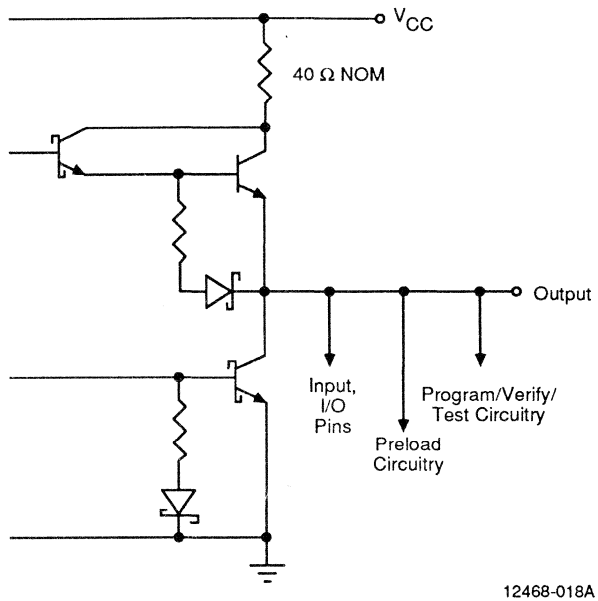
Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	560 Ω	1.1K Ω	560 Ω	1.1K Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output

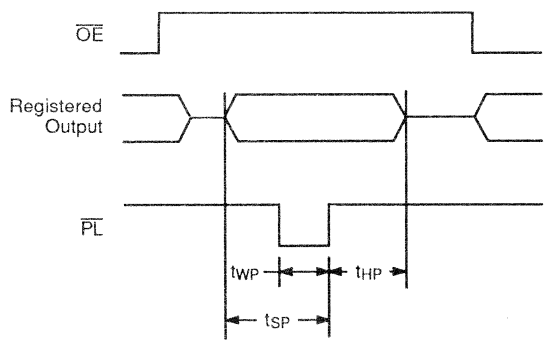


OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable output registers.
2. Apply either V_{IHP} or V_{ILP} to all registered outputs. Leave combinatorial outputs floating.
3. Pulse $\overline{PL}$ from V_{IHP} to V_{ILP} to V_{IHP}.
4. Remove V_{ILP}/V_{IHP} from all registered output pins.
5. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
6. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description		Min.	Rec.	Max.	Unit
V_{ILP}	Low-level input voltage		0	0	0.5	V
V_{IHP}	High-level input voltage		2.4	5.0	5.5	V
t_{SP}	Preload setup time	-20 COM'L	15			ns
		std COM'L	25			
		std MIL	30			
t_{WP}	Preload pulse width	-20 COM'L	20			ns
		std COM'L	35			
		std MIL	45			
t_{HP}	Preload hold time	-20 COM'L	15			ns
		std COM'L	25			
		std MIL	30			



10232-010A

Output Register Preload Waveform


IMPORTANT
NOTES

PALCE20V8

EE CMOS 24-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin, function and fuse-map compatible with all GAL® 20V8/As**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High speed CMOS technology**
  - –15 ns propagation delay for "–15" version
  - –25 ns propagation delay for "–25" version
- **Direct plug-in replacement for a wide range of 24-pin PAL devices**
- **Outputs individually programmable as registered or combinatorial**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 24-pin plastic SKINNYDIP® and 28-pin PLCC packages**
- **Programmable on standard PAL® device programmers**
- **Supported by PALASM® software**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

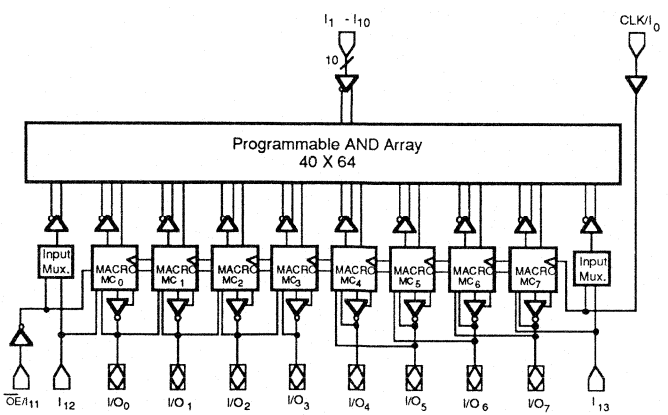
The PALCE20V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM

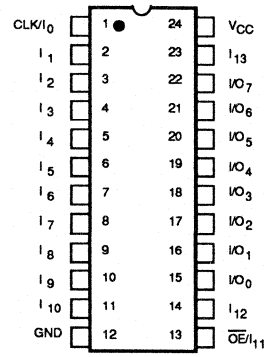


12197-001B

Publication # 12197 Rev. C Amendment /0
Issue Date: January 1990

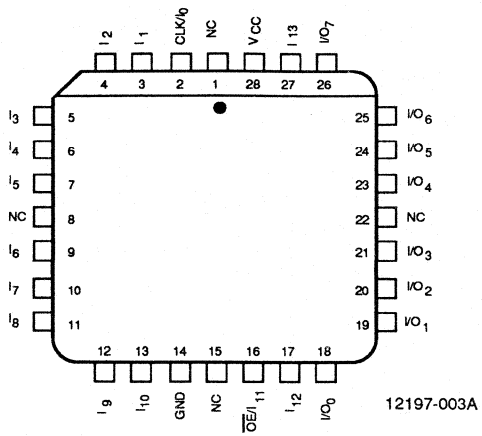
CONNECTION DIAGRAMS
Top View

SKINNYDIP



12197-002B

PLCC/LCC



12197-003A

Pin Designations:

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
$\overline{OE}$	=	Output Enable
V_{CC}	=	Supply Voltage

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Flip-Flops
f. Power
g. Speed
h. Package Type
i. Operating Conditions
j. Programming Designator

PAL CE 20 V 8 H -15 P C

a. FAMILY TYPE
PAL = Programmable Array Logic

b. TECHNOLOGY
CE = CMOS Electrically Erasable

c. NUMBER OF ARRAY INPUTS

d. OUTPUT TYPE
V = Versatile

e. NUMBER OF FLIP-FLOPS

f. POWER
H = Half Power (90 mA I_{CC})

g. SPEED
-15 = 15 ns t_{PD}
-25 = 25 ns t_{PD}

j. PROGRAMMING DESIGNATOR
Blank = Initial Release
/4 = First Revision
(May require different programmer revisions)

i. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

h. PACKAGE TYPE
P = 24-Pin 300-mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

Valid Combinations		
PALCE20V8H-15	PC, JC	Blank, /4
PALCE20V8H-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

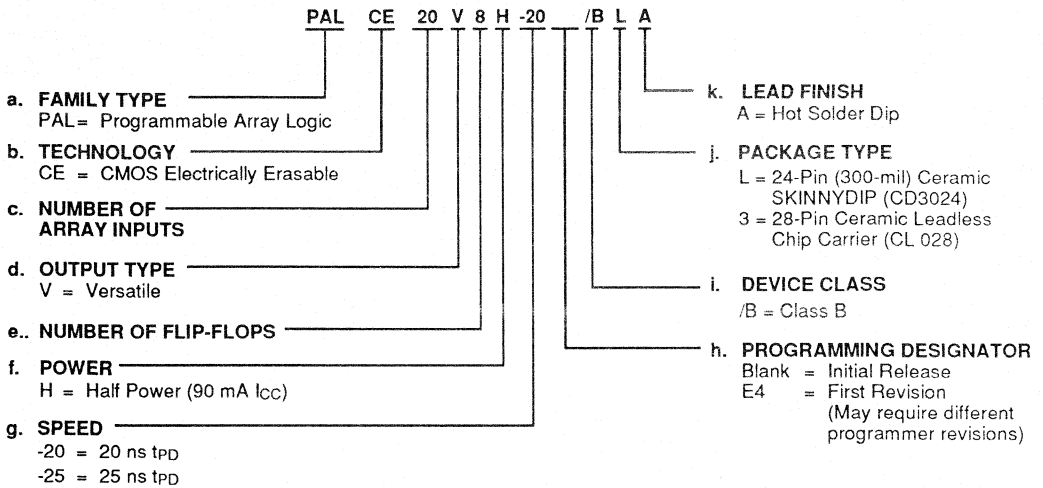
Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Flip-Flops
f. Power
g. Speed
h. Programming Designator
i. Device Class
j. Package Type
k. Lead Finish



Valid Combinations		
PALCE20V8H-20	Blank, E4	/BLA, /B3A
PALCE20V8H-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 7, 8, 9, 10 and 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

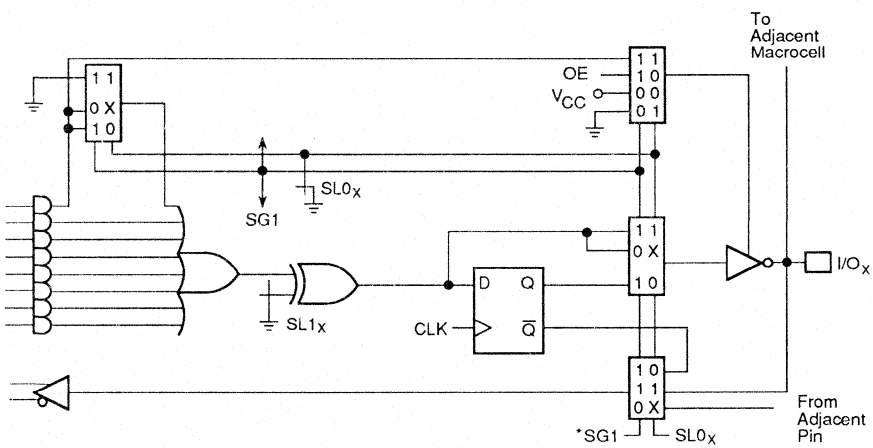
FUNCTIONAL DESCRIPTION

The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0..MC_7). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most 24-pin combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



* In Macrocell MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

12197-004A

PALCE20V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. A macrocell configured as a dedicated input derives the input signal from an adjacent I/O.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE20V8 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins are available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Because the macrocell is a dedicated output, the feedback is not used.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is an adjacent I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0, SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
			Device has registers	
0	1	0	Registered Output	PAL20R8, 20R6, 20R4
0	1	1	Combinatorial I/O	PAL20R6, 20R4
			Device has no registers	
1	0	0	Combinatorial Output	PAL20L2, 18L4,16L6,14L8
1	0	1	Dedicated Input	PAL20L2,18L4, 16L6
1	1	1	Combinatorial I/O	PAL20L8

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.

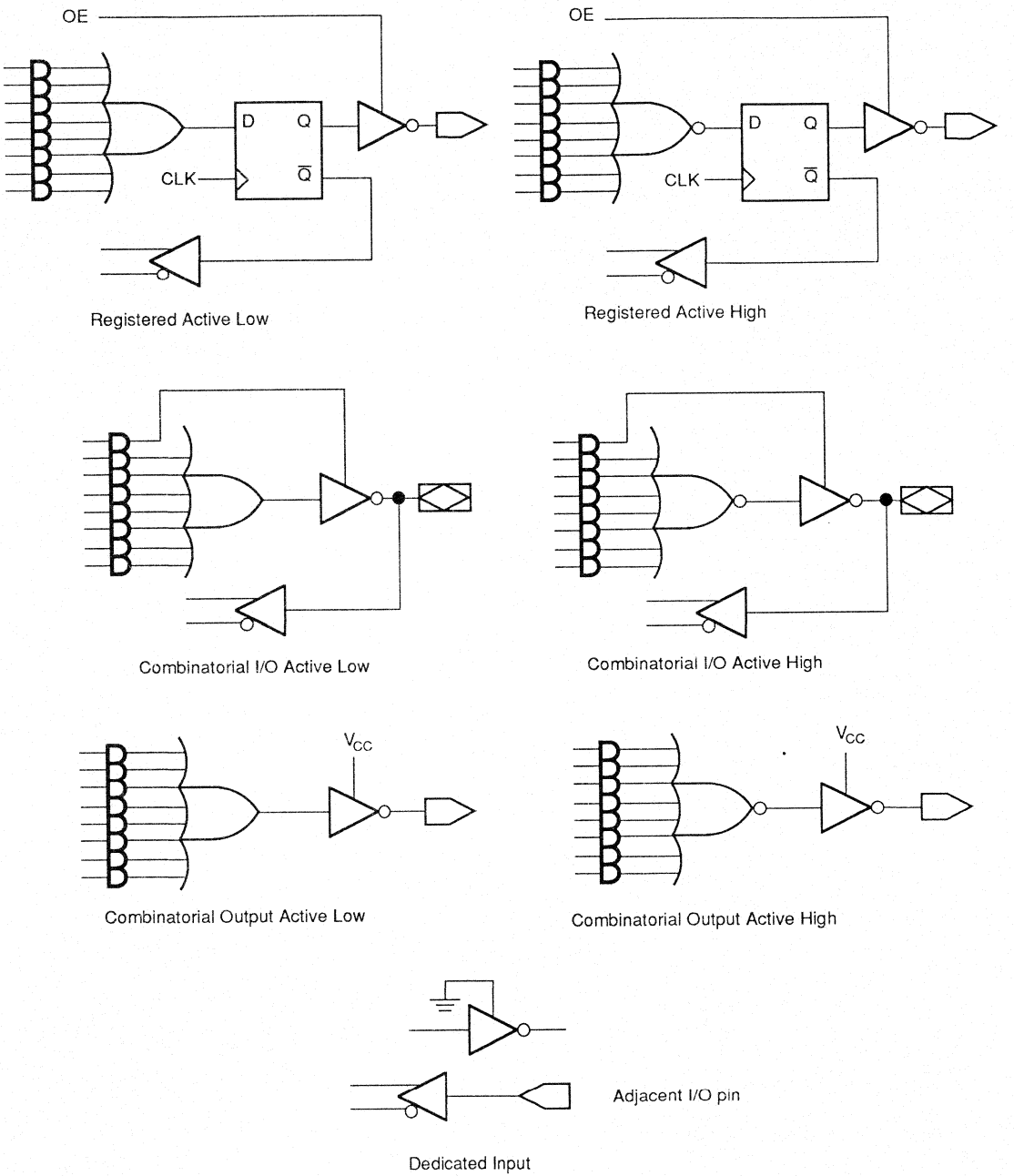


Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE20V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

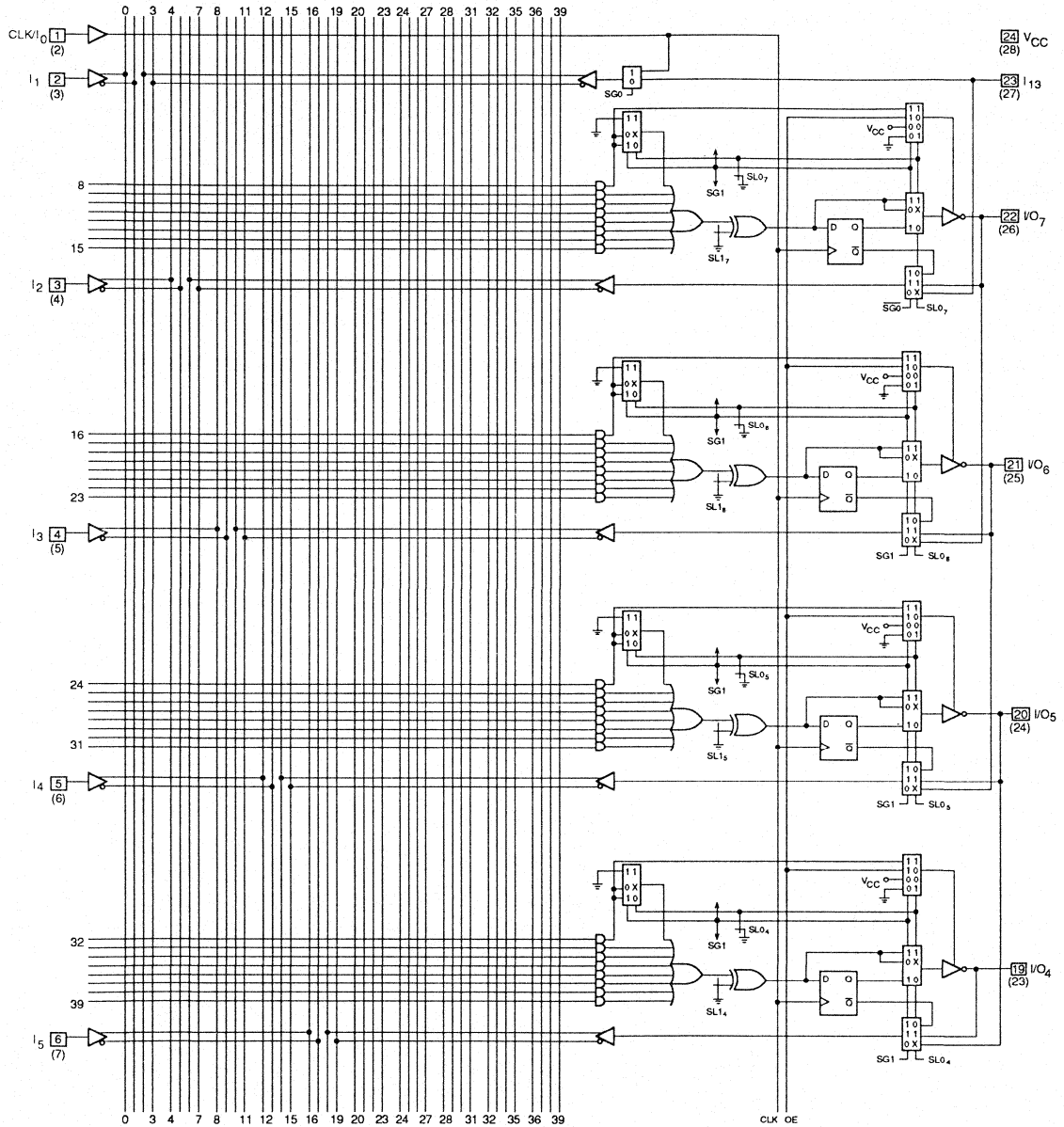
An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

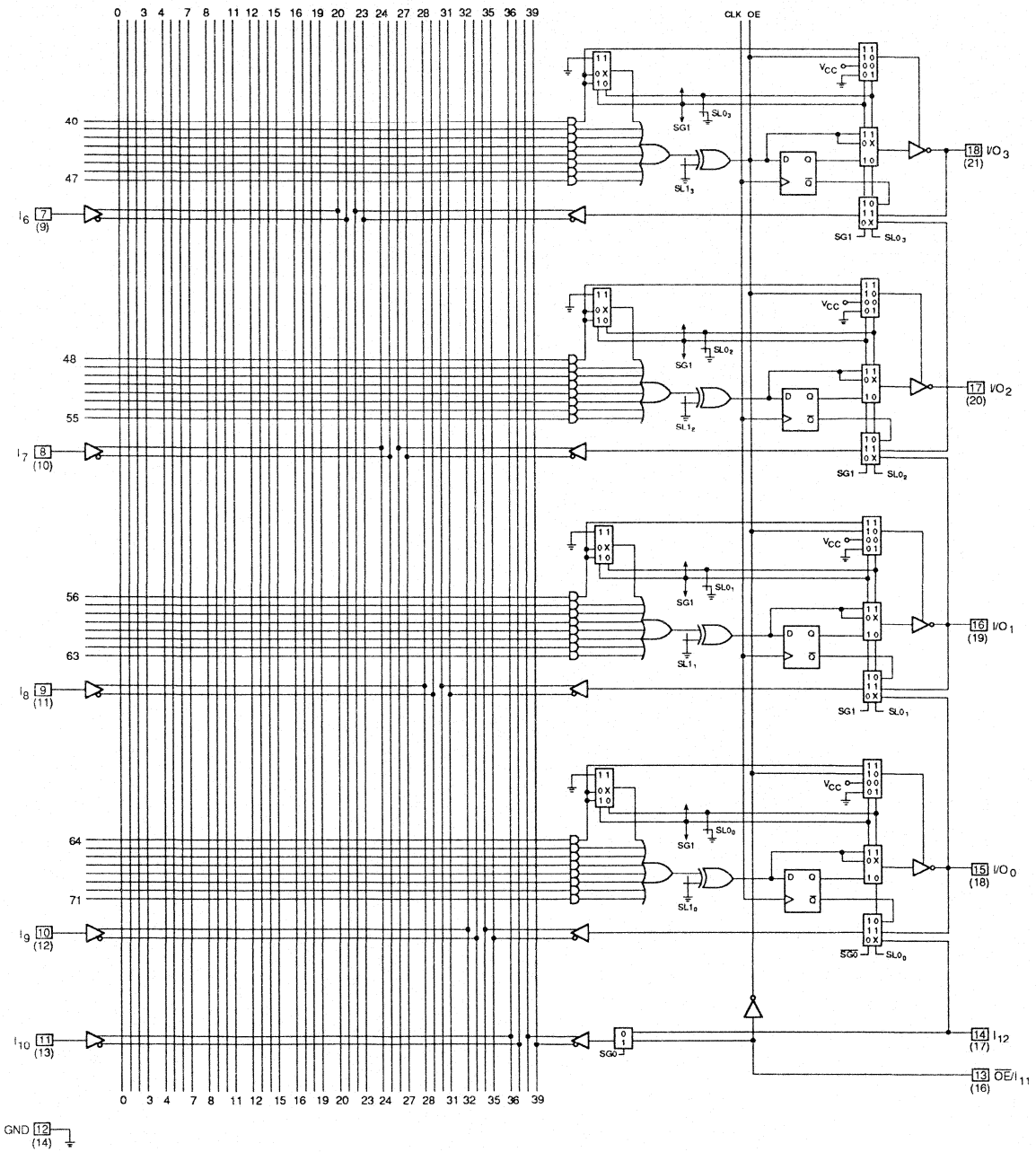
The PALCE20V8 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

LOGIC DIAGRAM
SKINNYDIP (PLCC and LCC) Pinouts



12197-005A

LOGIC DIAGRAM (Continued)
SKINNYDIP (PLCC and LCC) Pinouts



12197-005A
concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{CF}	Clock to Feedback (Note 3)				8		10	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback	$1/(t_S+t_{CF})$	50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		90	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{II} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	15	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

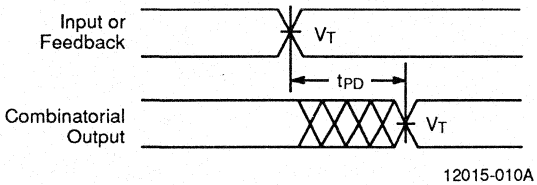
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input or Feedback to Clock			15		15		ns
t_H	Hold Time (Note 5)			0		0		ns
t_{CO}	Clock to Output				15		20	ns
t_{CF}	Clock to Feedback (Note 3)				13		18	ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	33.3		28.6		MHz
		Internal Feedback	$1/(t_S+t_{CF})$	35.7		30.3		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	41.7		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				20		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				20		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				20		25	ns

Notes:

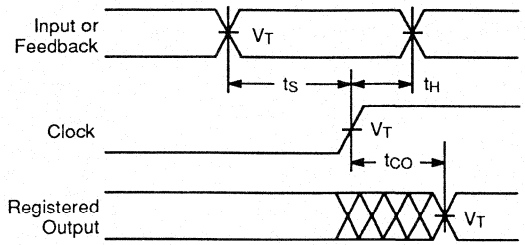
2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

SWITCHING WAVEFORMS



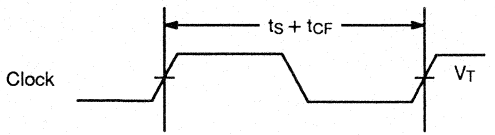
12015-010A

Combinatorial Output



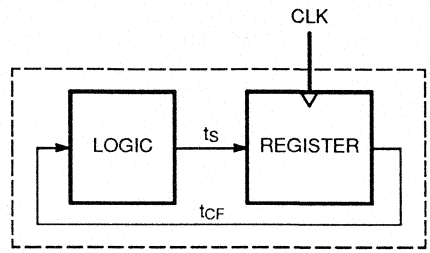
12015-012A

Registered Output

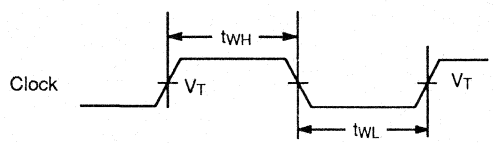


12149-025A

Clock to Feedback (f_{MAX} Internal)
See Path at Right

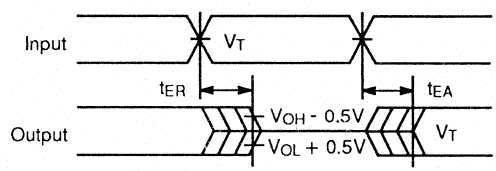


12015-021A



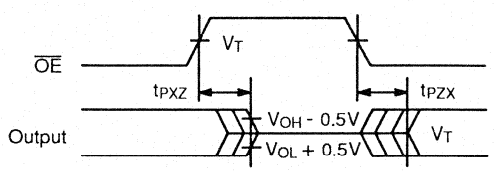
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

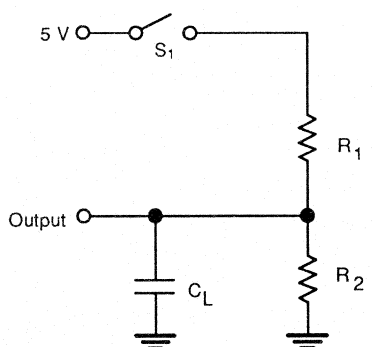
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12197-007A

Switching Test Circuit

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	50 pF	200 Ω	390 Ω	200 Ω	390 Ω	1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	200 Ω	390 Ω	200 Ω	390 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

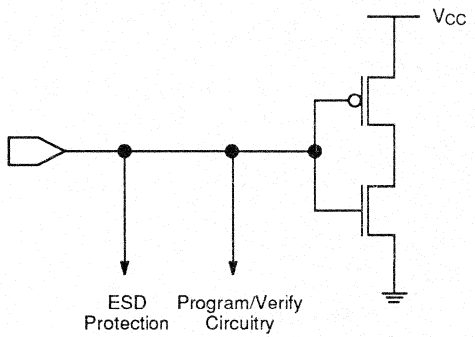
ENDURANCE CHARACTERISTICS

The PALCE20V8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

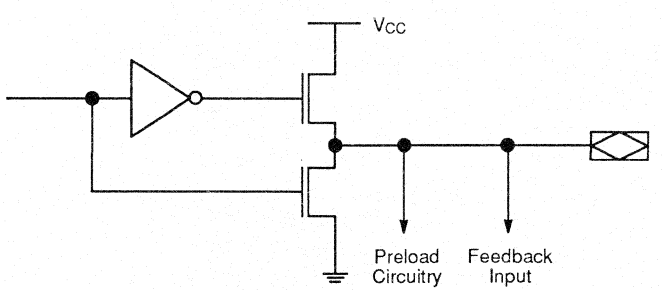
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

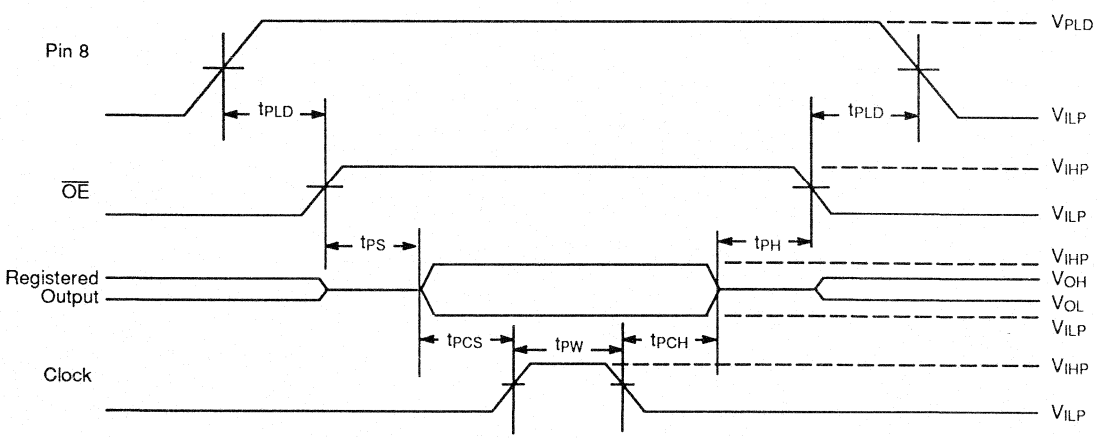
12197-013A

OUTPUT REGISTER PRELOAD

The Preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pin 8 to V_{PLD}.
3. Set $\overline{OE}$ HIGH.
4. Apply the desired value (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial output pins floating.
5. Clock pin 1 from V_{IL} to V_{IH}.
6. Remove V_{IL}/V_{IH} from all registered outputs.
7. Enable the output registers by lowering $\overline{OE}$.
8. Lower pin 8 to V_{IL}/V_{IH}.
9. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will be the inverse of the preload data.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_{PLD}	Setup and Hold Time from Preload (pin 8) to $\overline{OE}$	50	50		µs
t_{PS}	Setup Time from $\overline{OE}$ to Data	1	1		µs
t_{PH}	Hold Time from Data to $\overline{OE}$	1	1		µs
t_{PCS}	Setup Time from Data to Clock	1	1		µs
t_{PCH}	Hold Time from Clock to Data	1	1		µs
dV_r/dt	V_{PLD} Rising Slew Rate (pin 8)	10		100	V/µs
dV_f/dt	V_{PLD} Falling Slew Rate (pin 8)		2	3	V/µs
V_{PLD}	Super-Level Input Voltage	13.0	13.5	14.0	V
V_{IHP}	High-Level Input Voltage	2.4	5.0	5.5	V
V_{ILP}	Low-Level Input Voltage	0	0	0.5	V



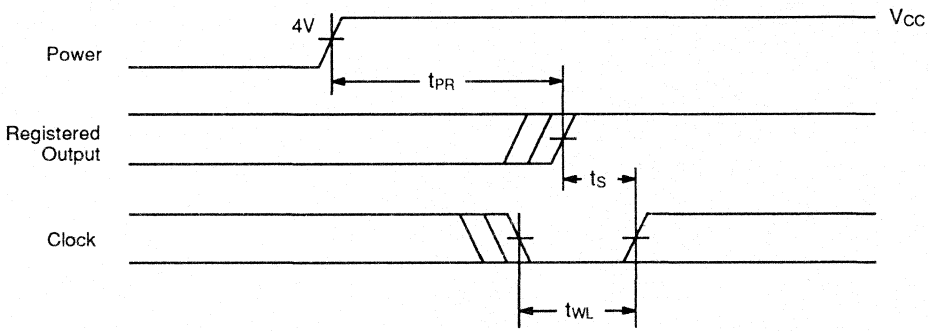
Output Register Preload Waveform

POWER-UP RESET

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

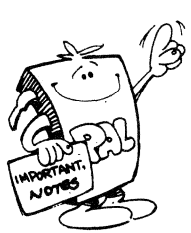
Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12197-009A

Power-Up Reset Waveforms

2



PAL20X10A Series
AmPAL20L10B/-20/AL

XOR Registered 24-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- XOR gates on registered outputs
- Efficient implementation of counters
- Popular 24-pin architectures: 20L10, 20X10, 20X8, 20X4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20X10A Series offers Exclusive-OR gates preceding each flip-flop. The XOR gate combines two sum terms, each composed of two product terms. This extra level of logic is very efficient for counter applications.

The combinatorial member of the family, the PAL20L10, offers three product terms per output with no XOR gate. A fourth product term provides the enable term. While the registered devices are offered in only one performance option, the 20L10 is offered in four performance grades. Note that three of these options follow the "old" AMD part numbering system while the fourth follows the "old" MMI part numbering system, as do the registered devices.

The family utilizes Advanced Micro Devices' advanced bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

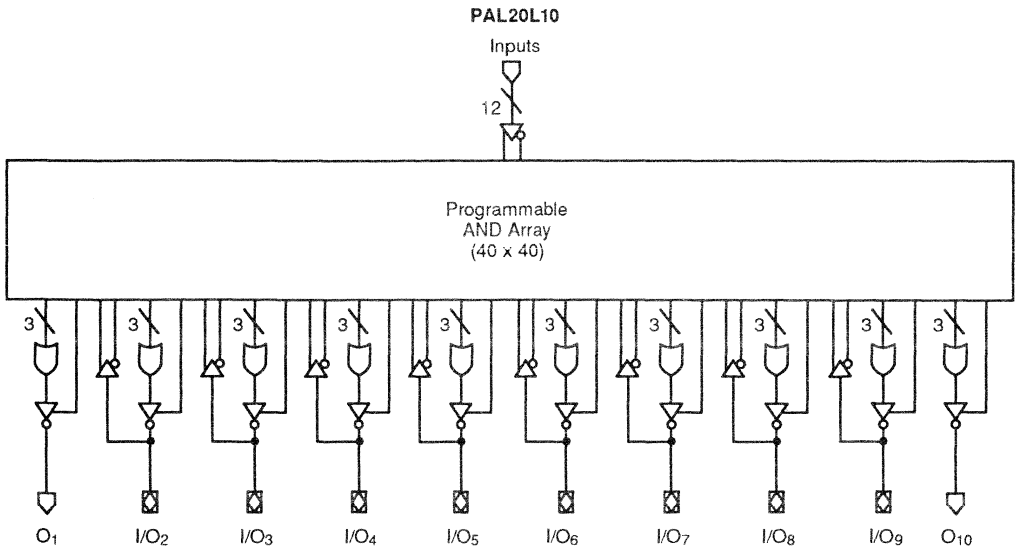
The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

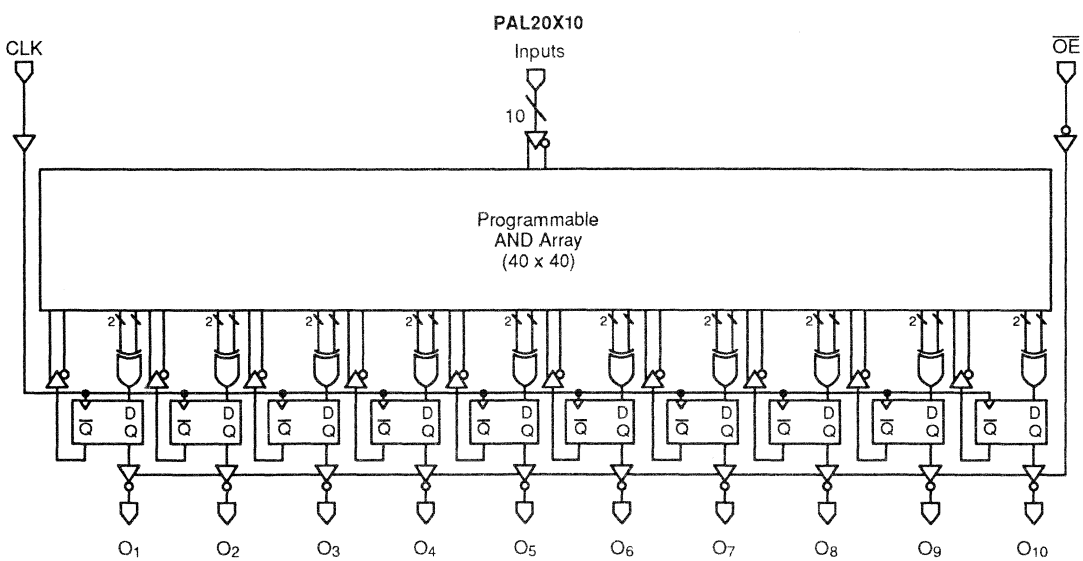
DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE	t_{PD} (ns)	I_{CC} (mA)
AmPAL20L10B	12	8 comb.	3	I/O	prog.	15	210
AmPAL20L10-20						20	165
AmPAL20L10AL		2 comb.	3	–	prog.	25	105
PAL20L10A						30	165
PAL20X10A	10	10 reg.	4, XOR	reg.	pin	30 (ts)	180
PAL20X8A	10	8 reg.	4, XOR	reg.	pin	30	180
		2 comb.	3	I/O	prog.		
PAL20X4A	10	4 reg.	4, XOR	reg.	pin	30	180
		6 comb.	3	I/O	prog.		

Publication # 10303 Rev. B Amendment/0
Issue Date: January 1990

BLOCK DIAGRAMS

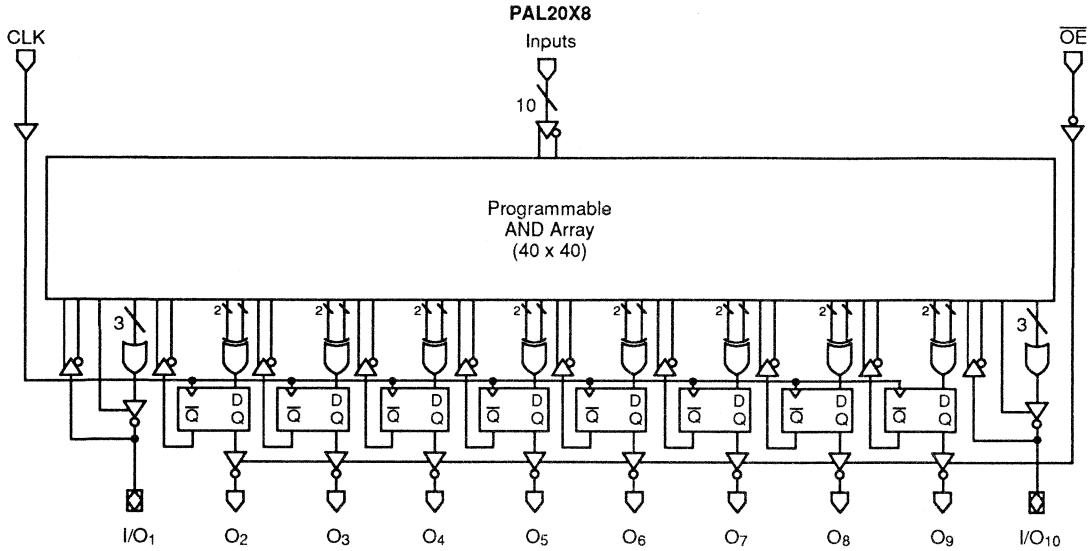


10303-001A



10303-002A

BLOCK DIAGRAMS



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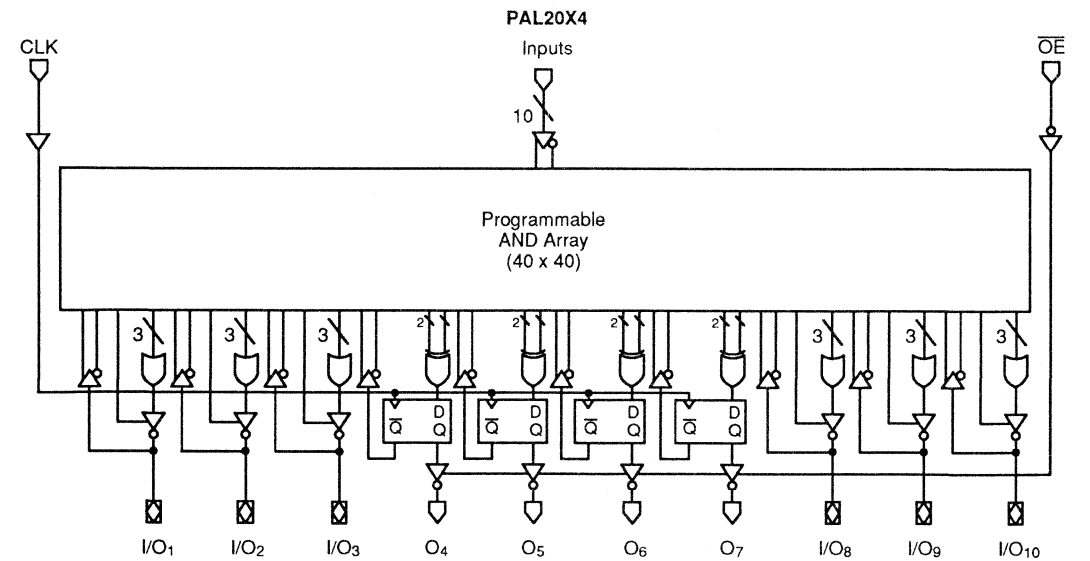
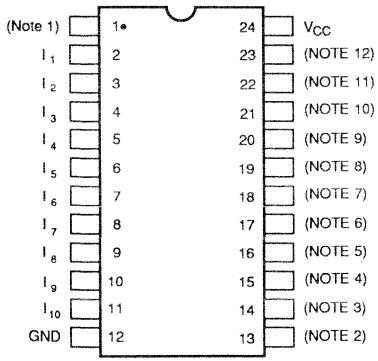


10303-004A

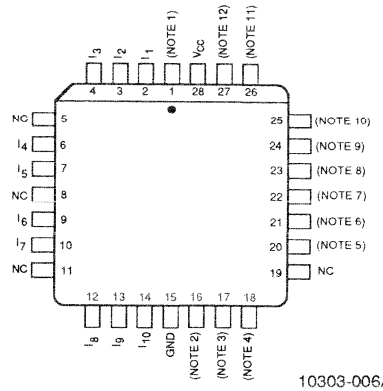
CONNECTION DIAGRAMS
Top View

SKINNYDIP/FLATPACK



10303-005A

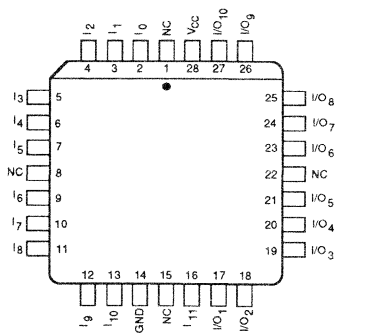
PLCC (except AmPAL20L10)



10303-006A

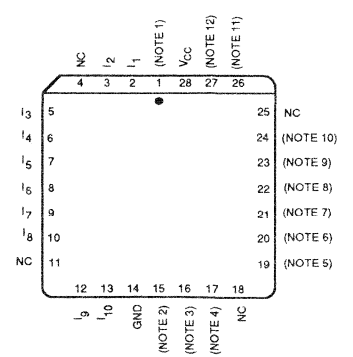
Note	20L10	20X10	20X8	20X4
1	I_0	CLK	CLK	CLK
2	I_{11}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	I/O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	O_7
10	I/O_8	O_8	O_8	I/O_8
11	I/O_9	O_9	O_9	I/O_9
12	O_{10}	O_{10}	I/O_{10}	I/O_{10}

PLCC
AmPAL20L10 only



10303-007A

LCC



10303-008A

Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

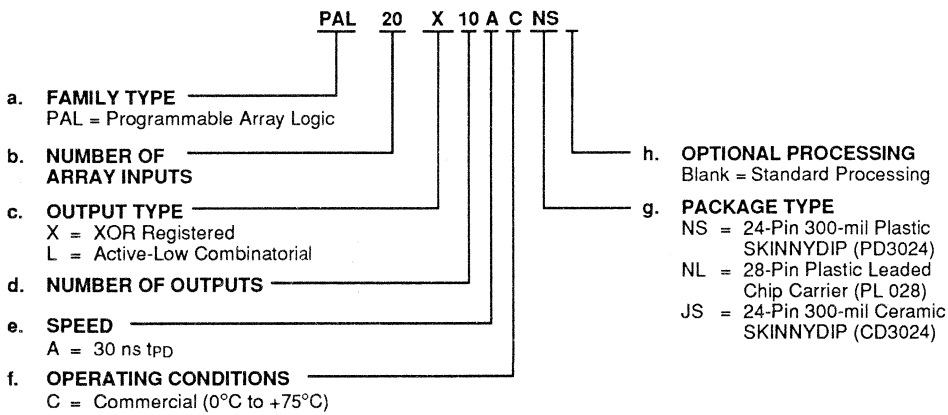
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products (MMI Marking Only)

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Operating Conditions
g. Package Type
h. Optional Processing



Valid Combinations	
PAL20L10A	CNS, CNL, CJS
PAL20X10A	
PAL20X8A	
PAL20X4A	

Valid Combinations

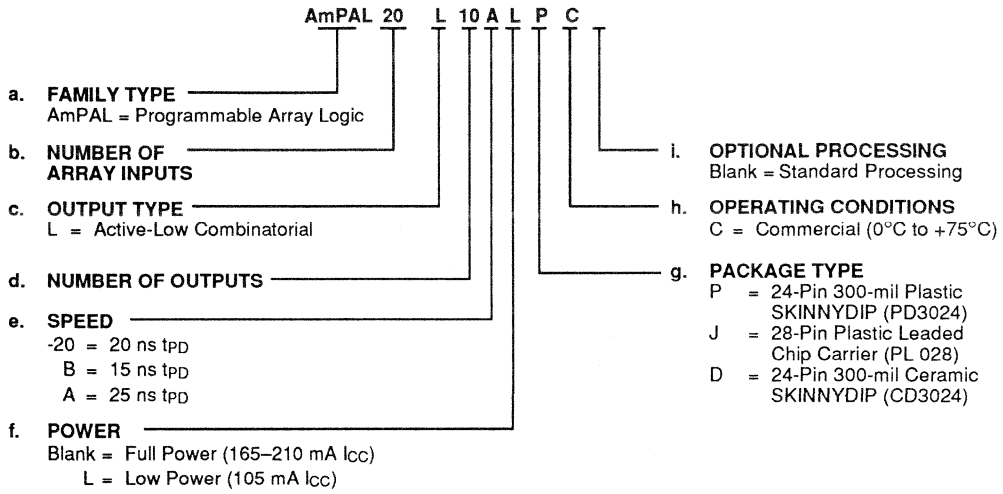
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

ORDERING INFORMATION
Commercial Products (AMD Marking Only)

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Power
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations		
AmPAL20L10	B, -20, AL	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

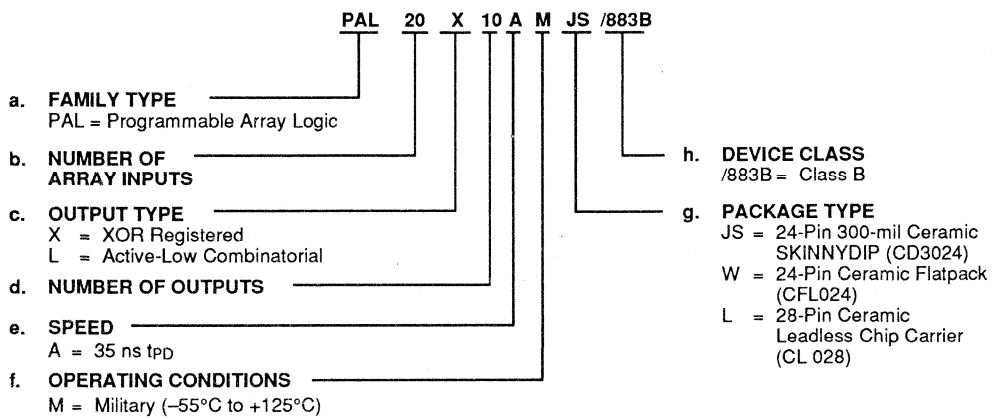
Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Operating Conditions
g. Package Type
h. Device Class



Valid Combinations	
PAL20L10A	MJS/883B, MW/883B, ML/883B
PAL20X10A	
PAL20X8A	
PAL20X4A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Four different devices are available in the 20X10 Series, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have ten dedicated input lines, and each combinatorial output is an I/O pin. The 20L10 has twelve dedicated input lines, and only eight of the ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20X10A Series will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL20X10A Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20X10 Series design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact. For the AmPAL20L10, the array will read as if every fuse is programmed.

Pinouts

All members of the PAL20X10 Family have the same SKINNYDIP pinouts independent of technology, performance, and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. The AmPAL20L10 and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The older PAL20X10A Series devices retain their original pinouts, with no-connects on pins 5, 8, 11, and 19.

A different LCC pinout is offered for military products.The older PAL20X10A Series devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25.

Series	Com'l PLCC No-connects	Mil LCC No-connects
AmPAL20L10 B/-20/AL	1, 8, 15, 22 (JEDEC)	N/A
PAL20X10A Series (inc. PAL20L10A)	5, 8, 11, 19	4, 11, 18, 25

Quality and Testability

The PAL20X10 Series offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

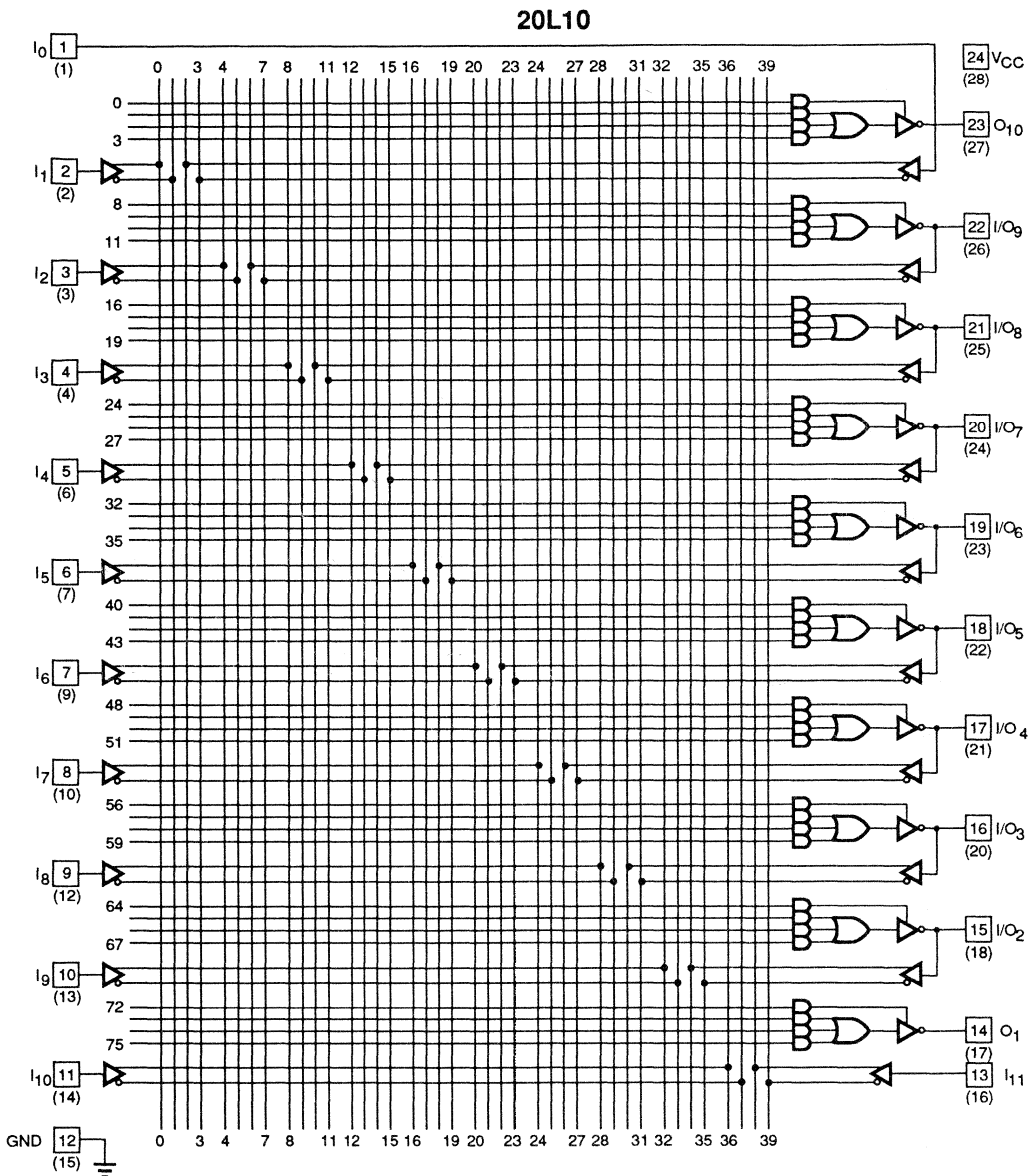
The PAL20X10A Series is fabricated with AMD's advanced junction-isolated bipolar process. The array connections are formed with proven TiW fuses for reliable operation.

The AmPAL20L10 is fabricated with the IMOX™ oxide-isolated bipolar process using proven PtSi fuses.

LOGIC DIAGRAM

SKINNYDIP (PLCC, PAL20L10A only) Pinouts

See Connection Diagrams for LCC and AmPAL20L10 PLCC Pinouts

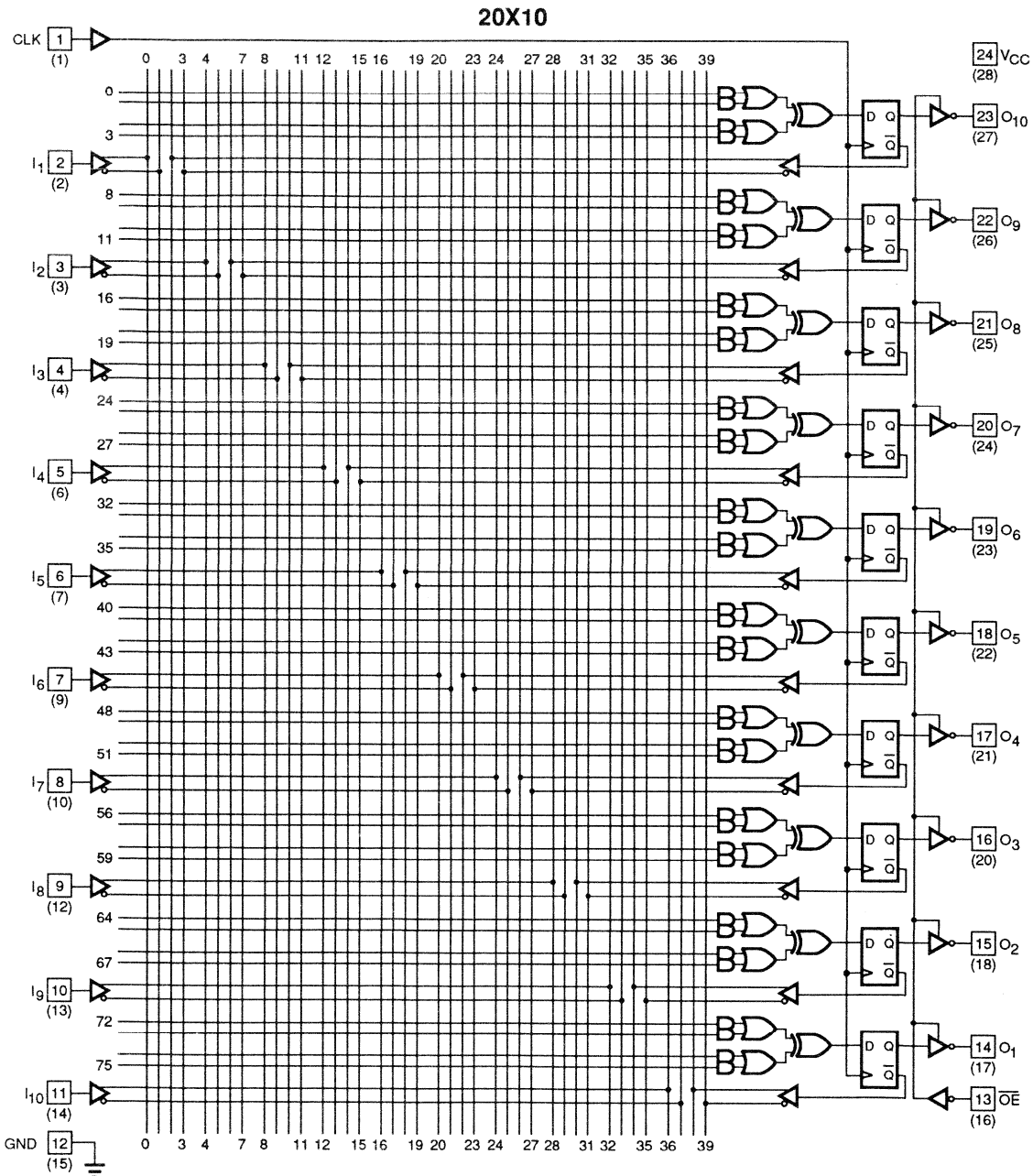


10303-009A

LOGIC DIAGRAM

SKINNYDIP (PLCC) Pinouts

See Connection Diagrams for LCC Pinout

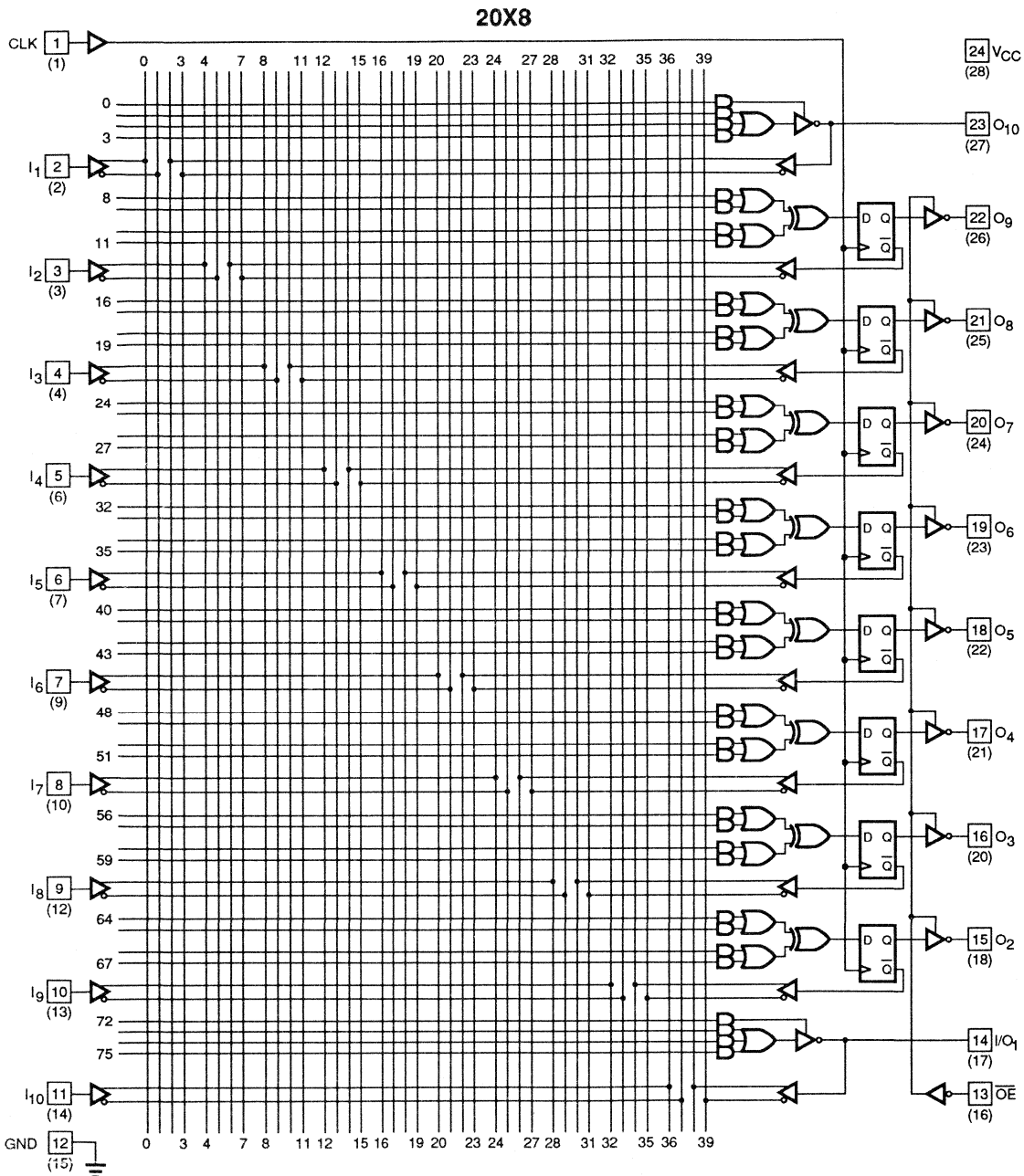


10303-010A

LOGIC DIAGRAM

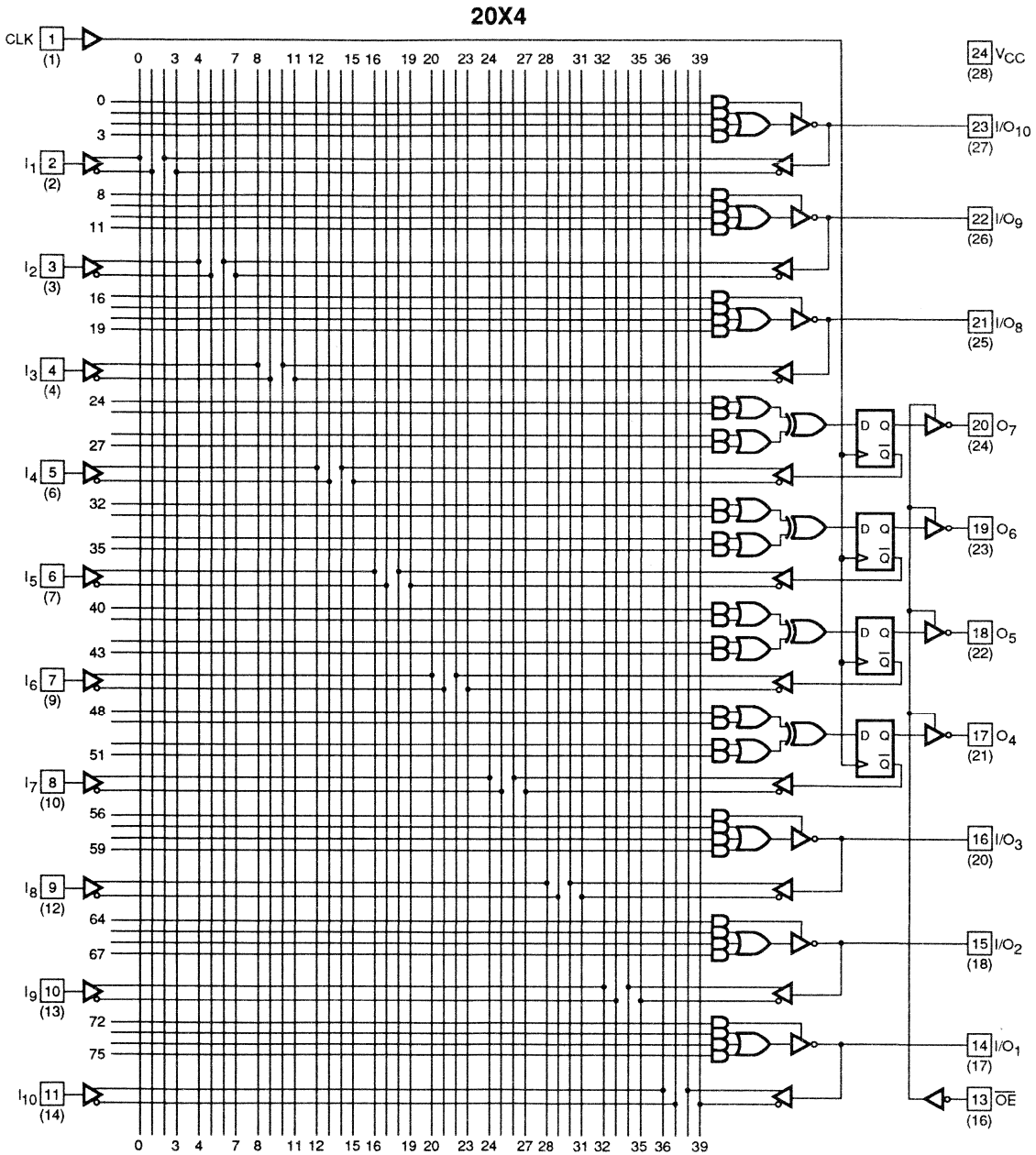
SKINNYDIP (PLCC) Pinouts

See Connection Diagrams for LCC Pinout



10303-011A

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts
See Connection Diagrams for LCC Pinout



10303-012A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	20X10A, 20X8A, 20X4A		180	mA
			20L10A		165	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L10A, 20X8A, 20X4A		30	ns
t_S	Setup Time from Input or Feedback to Clock			20X10A, 20X8A, 20X4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		22.2		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L10A, 20X8A, 20X4A		30	ns
t_{ER}	Input to Output Disable Using Product Term Control					30	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to 5.5 V
DC Output or I/O Pin Voltage	–0.5 V to 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA $V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)			–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	20X10A, 20X8A, 20X4A		180	mA
			20L10A		165	

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L10A, 20X8A, 20X4A		35	ns
t_S	Setup Time from Input or Feedback to Clock			20X10A, 20X8A, 20X4A	40		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			35		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		15.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		18.2		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L10A, 20X8A, 20X4A		35	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					35	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	20L10B		210	mA
			20L10-20		165	
			20L10AL		105	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

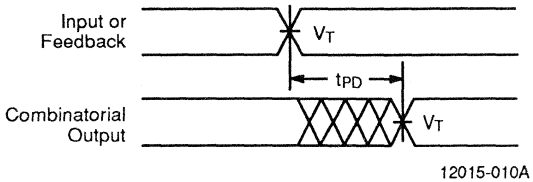
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	20L10B		20L10-20		20L10AL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		20		25	ns
t_{EA}	Input to Output Enable Using Product Term Control		18		20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		20		25	ns

Notes:

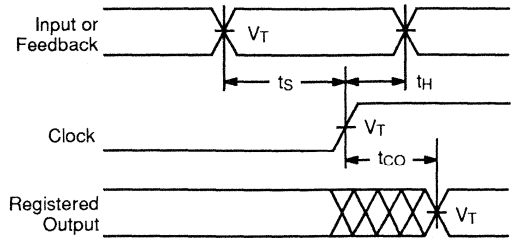
2. See Switching Test Circuit for test conditions.

SWITCHING WAVEFORMS



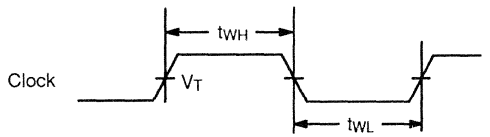
12015-010A

Combinatorial Output



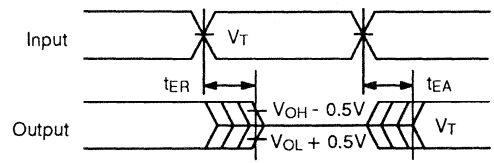
12015-012A

Registered Output



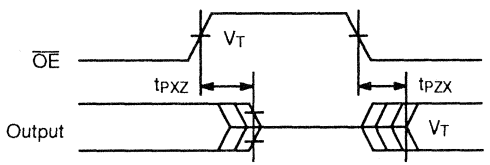
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

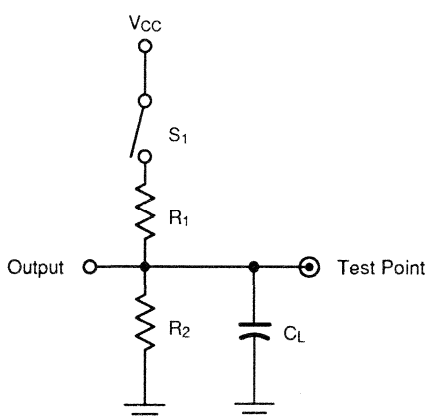
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

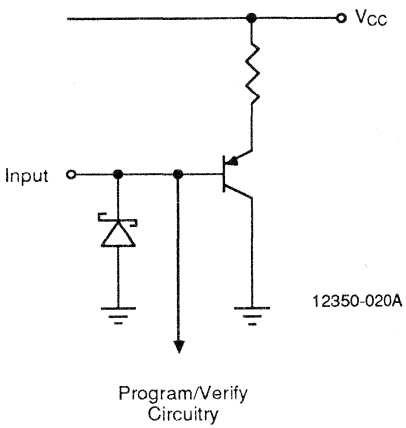


10303-013A

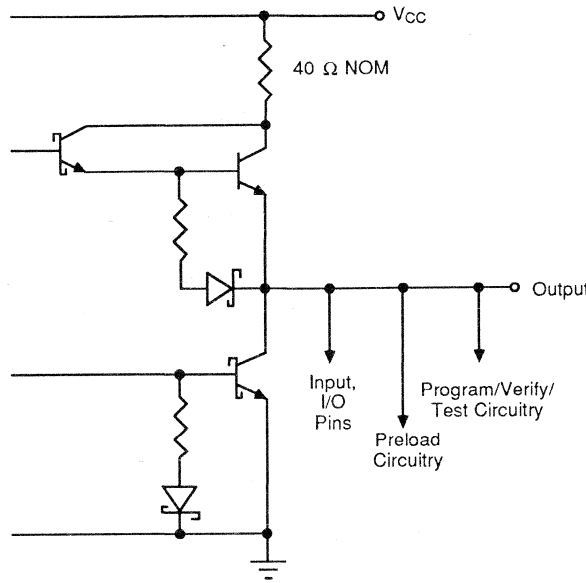
Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output

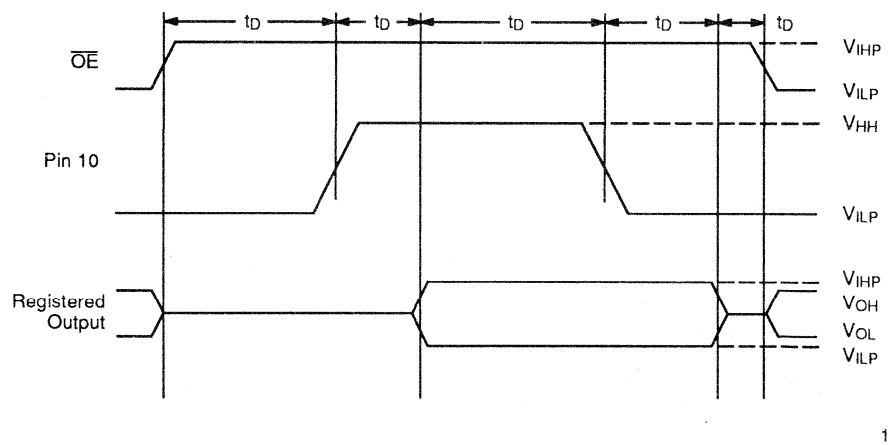


OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Raise pin 10 to V_{HH} to enter preload mode.
4. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
5. Lower pin 10 to V_{ILP}.
6. Remove V_{ILP}/V_{IHP} from all registered output pins.
7. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19	20	21	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload		4.5		V
t_D	Delay time	100	200	1000	ns



10303-015A

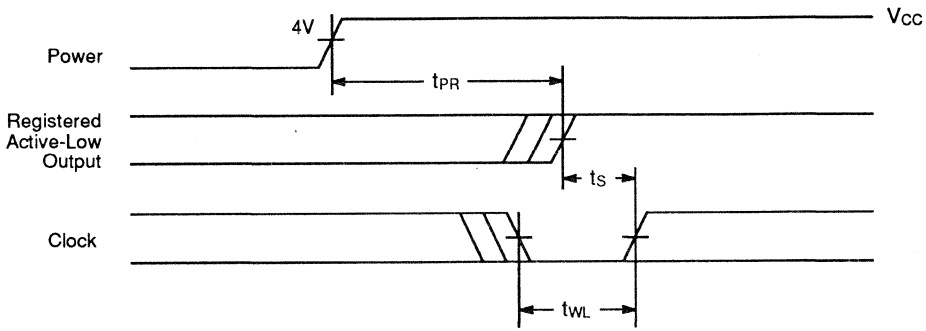
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform

2

Final | Com'l

PAL22IP6-25

Interface Protocol Asynchronous Cell (IPAC) PAL® Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

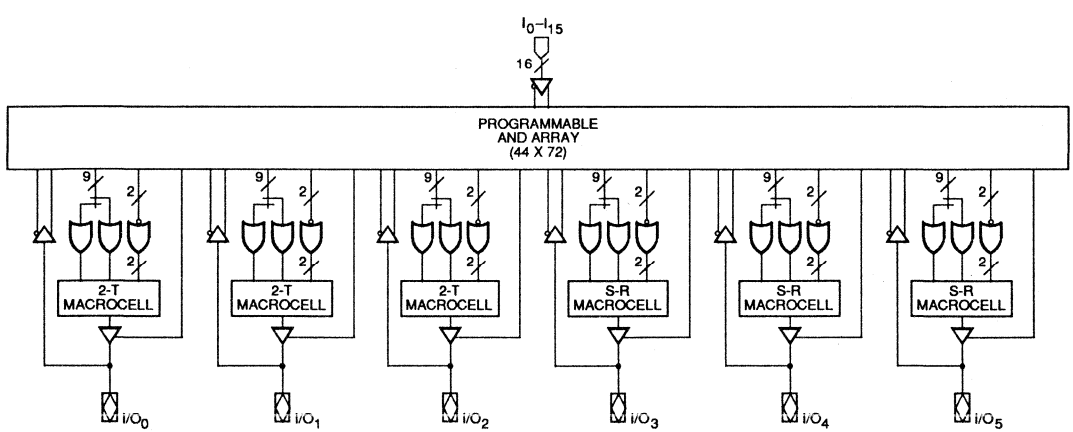
- PAL device optimized for asynchronous interface protocol applications
- High current driving capability—48 mA/64 mA
- Six unique edge-activated flip-flops
  - Three edge-activated Set-Reset flip-flops (S-R)
  - Three edge-activated Dual-Toggle flip-flops (2-T)
- Two Edge-Activated-Inputs per flip-flop offer powerful system benefits:
  - S-R: input rejects signals once triggered
  - 2-T: simultaneous edge-activated-inputs allowed
- Product term steering feature enhances flexibility
- Individual level-sensitive Preset and Clear for each flip-flop
- Programmable polarity for Edge-Activated Inputs (S, R, T_1 and T_2)
- Individually programmable Asynchronous Preset/Clear:
  - Both override all Edge-Activated-Inputs to a cell
  - Preset has higher priority than Clear
- Flip-flops can be bypassed individually
- Center V_{CC} and Ground pins to reduce ground bounce
- Special security fuse for design secrecy
- Easy design with PALASM® software
- Programmable on standard PAL device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL22IP6 Interface Protocol Asynchronous Cell (IPAC) PAL device contains two basic types of Edge-Activated-Input flip-flops. The first type of flip-flop is a new bistable structure known as the Dual-Toggle flip-flop (2-T). This bistable structure simply reverses output state whenever an active edge occurs on either of the two input lines. The two inputs (T_1 and T_2) are totally independent of each other. The second type of flip-flop is an edge-activated Set-Reset flip-flop (S-R). With the S-R flip-flop, an active edge on the Set input causes the flip-flop to go HIGH, and an active edge on the Reset input causes the flip-flop to go LOW. The PAL22IP6 has three sets of the S-R and 2-T macrocells, along with the PAL array for implementing logic functions.

These flip-flops do not have a "data path", which means they have no setup or hold time constraints. In addition, all of the Edge-Activated-Input polarities are programmable, which provides the user a choice of either rising or falling edge for each input.

BLOCK DIAGRAM



968 01

Publication # 10997 Rev.C Amendment /0
Issue Date: January 1990

GENERAL DESCRIPTION (Cont'd.)

All of the flip-flops feature level-sensitive Asynchronous Preset (AP) and Asynchronous Clear (AC) inputs, which can override the Edge-Activated-Inputs. A HIGH logic level on the AP input of the flip-flop will cause the flip-flop to change to a logic 1 state asynchronously. Likewise, a HIGH logic level on the AC input of the flip-flop will cause the flip-flop to change to a logic 0 state asynchronously. The AP signal has priority over the AC signal; if both are HIGH simultaneously, the flip-flop will be preset to a logic 1 state. The AP and AC functions are discussed in more detail later. The IPAC flip-flops feature the capability of receiving both Preset and Clear signals in any order, even simultaneously, with predictable results. The output registers can be bypassed individually to provide more design flexibility. The output registers also include I/O feedback to enhance state machine designs.

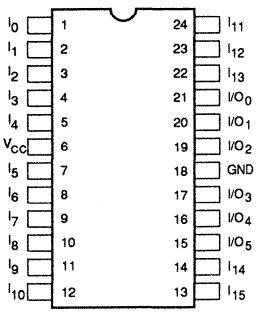
The IPAC PAL device is fabricated using Advanced Micro Devices' advanced MONOX III process, which is a fully ion-implanted oxide-isolated stepper-aligned process. It provides high reliability, and high programming and functional yields. Special on-chip test circuits allow full AC, DC, and functional testing before programming.

The PAL22IP6 can be programmed on standard PAL device programmers with appropriate programming modules and software configurations. Design development is supported by Advanced Micro Devices' PALASM® software as well as by other programmable logic design tools available from third-party vendors.

CONNECTION DIAGRAMS

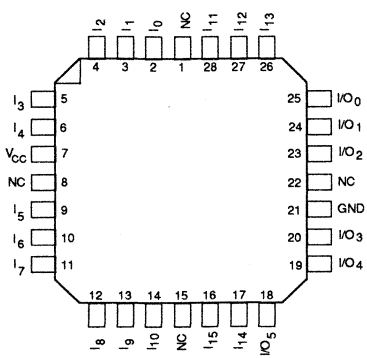
Top View

SKINNYDIP



968 03

PLCC



968 03A

PIN DESIGNATIONS

I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
GND = Ground
NC = No Connect

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages.
The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option
c. Package Type
d. Operating Conditions
e. Optional Processing

PAL 22 IP 6 –25 P C

a. PROGRAMMABLE ARRAY LOGIC
NUMBER OF ARRAY INPUTS
OUTPUT TYPE
IP = Interface Protocol
NUMBER OF FLIP-FLOPS
b. SPEED
– 25 = 25 ns t_{PD}

e. PROCESSING
blank = Standard
XXXX = Other

d. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

c. PACKAGE TYPE
P = Plastic SKINNYDIP (PD 3024)
D = Ceramic SKINNYDIP (CD 3024)
J = Plastic Leaded Chip Carrier (PL 028)

Valid Combinations

Valid Combinations	
PAL22IP6-25	PC, DC, JC

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.
Note: marked with AMD logo.

FUNCTIONAL DESCRIPTION

The PAL22IP6 has sixteen dedicated input lines and six programmable output macrocells with I/O pin feedback. Each macrocell has two Edge-Activated-Inputs and Asynchronous Preset and Clear inputs. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array.

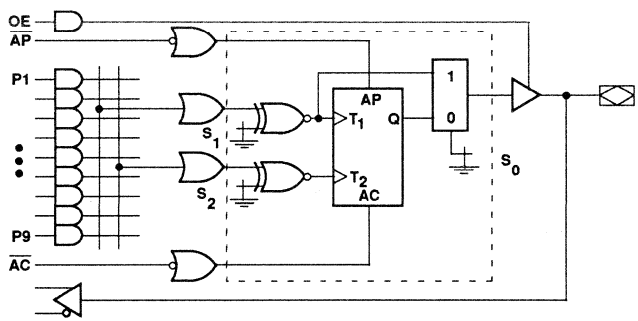
The programmable functions in the PAL22IP6 are automatically configured from the user's design specification. The design specification is processed by development software to verify the design and create a programming file. The file, once downloaded to a programmer, configures the device according to the desired function.

Powerful 2-T and S-R Flip-Flops

The PAL22IP6 has three positive edge-activated 2-T flip-flops and three positive edge-activated S-R flip-flops. Each flip-flop has two Edge-Activated-Inputs with programmable polarity. These inputs are driven by an OR gate with up to nine product term inputs with product term steering. Each product term can have up to 22 inputs. The descriptions, macrocells, and function tables for both 2-T and S-R flip-flops are shown below.

2-T Flip-Flop Description

The 2-T flip-flop output will be toggled whenever a rising edge is applied to either of the two Edge-Activated-Inputs. Two rising edges between two inputs of the 2-T flip-flop can be totally asynchronous. Simultaneous rising-edge inputs will not cause metastability, and the flip-flop output will remain the same.



968 02

Figure 1a. IPAC 2-T Macrocell

Input to Flip-flop				Output	Function
T_1	T_2	AP	AC	Q_{n+1}	
†	†	0	0	Q_n	Hold
↑	†	0	0	$\overline{Q_n}$	Toggle on T_1
†	↑	0	0	$\overline{Q_n}$	Toggle on T_2
↑	↑	0	0	Q_n	Dual Toggle; No Change*
X	X	1	X	1	Force Priority 1
X	X	0	1	0	Force Priority 0

Nomenclature

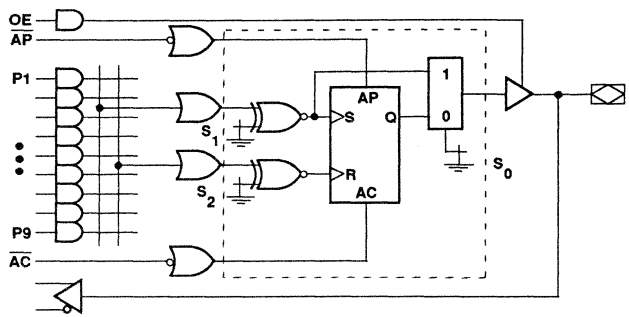
↑ = rising-edge transition
X = don't care
0 = logic zero
1 = logic one
† = states other than a rising-edge transition (either 0, 1, or falling-edge transition)

* Simultaneous edge triggering of T_1/T_2 is ALLOWED, and will result in the output not changing, or will produce a narrow pulse, depending on the timing lapse of the edges

Table 1a. Edge-Activated 2-T Function Table

S-R Flip-Flop Description

The S-R flip-flop will go HIGH after the first Set rising edge and will disregard the subsequent Set edges until a Reset signal is received. It will go LOW after the first Reset rising edge and will then disregard the subsequent Reset edges until the Set signal is received. The time lapse between the Set and Reset active triggering edges on the device input should be greater than $t_{S\text{-}R,\,max}$ in order to trigger on both inputs. If it is less than $t_{S\text{-}R,\,min}$ the second Edge-Activated-Input will not trigger the flip-flop. If it is between the $t_{S\text{-}R,\,max}$ and $t_{S\text{-}R,\,min}$, the output will be unpredictable.



968 04

Figure 1b. IPAC S-R Macrocell

Input to Flip-Flop				Output	Function
S	R	AP	AC	Q_{n+1}	
†	†	0	0	Q_n	Hold
†	↑	0	0	0	Reset to 0 on edge
↑	†	0	0	1	Set to 1 on edge
X	X	1	X	1	Force Priority 1
X	X	0	1	0	Force Priority 0

Nomenclature

↑ = rising-edge transition
X = don't care
0 = logic zero
1 = logic one
† = states other than a rising-edge transition (either 0, 1, or falling-edge transition)

Note: Set and Reset edge-activated inputs must be separated by $t_{S\text{-}R,\,max}$ for output to change (refer to Special IPAC Timing Parameters).

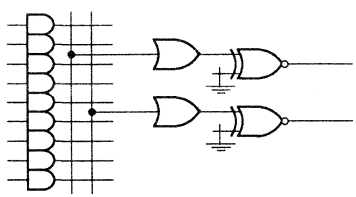
Table 1b. Edge-Triggered S-R Function Table

Programmable Edge-Activated-Input Polarity

The Edge-Activated-Inputs of each macrocell are asynchronous with respect to each other, and the polarity of each triggering edge is independently programmable depending on the fuse on the input of the Exclusive-NOR gate. Since these inputs to each macrocell come from the programmable array, the flip-flops can be triggered independently.

Product Term Steering

Product term steering allows each pair of Edge-Activated-Inputs to allocate terms to one input or the other (not both). Each macrocell has a total of nine data product terms; thus, one Edge-Activated-Input can use zero to nine while the other has nine to zero (e.g., three and six). Product terms can not be shared between flip-flop inputs. If both Edge-Activated-Inputs need the same term, it must be created twice, once for each input.



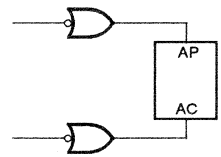
968 08

Figure 2. IPAC PAL Device Product Term Steering

Programmable Level-Sensitive Asynchronous Preset and Clear

Each macrocell flip-flop has separate sum terms for Asynchronous Preset (AP) and Asynchronous Clear (AC). The Preset and Clear signals for all flip-flops are asynchronous and independently programmable. Both inputs are level-sensitive and override the Edge-Activated-Inputs. Preset forces the output to go HIGH, while Clear forces the output to go LOW. When both signals are asserted simultaneously, Preset will override Clear. The IPAC flip-flops provide the capability to operate both Preset and Clear in any sequence, including simultaneously with predictable results.

Note that for the IPAC PAL device, Asynchronous Preset and Asynchronous Clear are sum terms rather than product terms. Both Preset and Clear are controlled by independent OR gates with inverted inputs (Figure 3a). Since both the true and complement of every array input are available, the Preset and Clear equations can be written as a simple sum of device inputs and feedback. This allows more than one condition to force Preset and Clear, adding greater flexibility for the designer. Through DeMorganization, NAND gate control is also possible, as shown in Figure 3b.



968 09

Figure 3.
IPAC PAL Device Asynchronous Preset and Clear

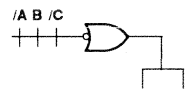
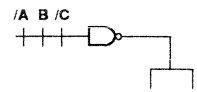


Figure 3a.
IO.SETF = A+/B+C
OR Function



968 09 A & B

Figure 3b.
IO.SETF = /(/A*B*/C)
DeMorganized Equivalent

Registered or Combinatorial Outputs

Each output of the PAL22IP6 includes an edge-activated flip-flop for data storage and synchronization. Any output can be configured to be combinatorial by selecting the multiplexer path that bypasses the output flip-flop. Bypass is automatically selected if requested in the design specification. The unprogrammed configuration is a registered I/O.

Output Enable and High Current Bus Driver

The flip-flop outputs can be enabled to present logic HIGH or logic LOW states, or can be disabled to provide a high-impedance state. Each output enable is independently programmable by a dedicated product term. I/O pins I/O_0, I/O_1, I/O_4 and I/O_5 can drive up to 48 mA; I/O pins I/O_2 and I/O_3 can drive up to 64 mA. The high current output driving capability of the IPAC PAL device is designed to improve the performance and density of three-state memory address/data drivers, clock drivers and bus-oriented drivers for most buses in the market.

Security Fuse

After programming and verification, a PAL22IP6 can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors.

Quality and Testability

The PAL22IP6 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields.

IPAC DESIGN RESTRICTION

Overview

The high-speed IPAC PAL device has one design restriction. On the S-R flip-flop, direct active-HIGH feedback from the output to the non-inverting R input will violate the timing requirements and the output will be unpredictable. The solution is to DeMorganize the R-input equation.

Timing Requirement

For the S-R flip-flop, active edges on S and R must be separated by at least $t_{S\text{-}R,\ max}$ to guarantee that the flip-flop will respond. If *direct feedback* is used (Q is part of the S or R-input equation) then one input may follow the other by t_{EIO}, the delay from input to registered feedback. Therefore, t_{EIO} must be greater than $t_{S\text{-}R,\ max}$ (Figure 7). We will refer to this as the *feedback criterion*. For the high-speed IPAC PAL device, we can guarantee this in all but one case.

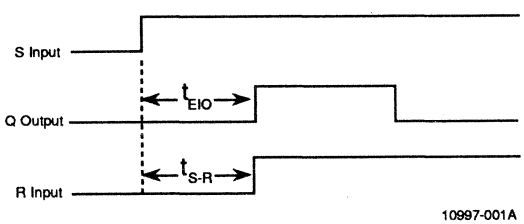
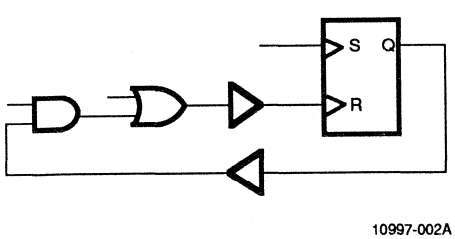


Figure 7. If Q = R, t_{EIO} must be greater than $t_{S\text{-}R}$

Design Restriction

This one case not allowed is direct active-HIGH feedback from Q to the non-inverting rising-edge triggered R input (Figure 8). This also includes feedback from a different flip-flop if both S inputs contain a common source input (Figure 9). We will refer to this as *direct feedback equivalent*. All other configurations are allowed.



Q.R := Q ; not allowed

Figure 8. Direct active-HIGH feedback to R; not allowed

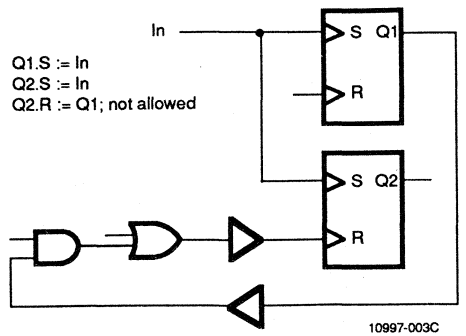
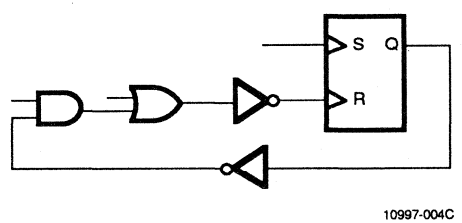


Figure 9. Equivalent to direct feedback; not allowed

Solution

The solution is to DeMorganize the equation so that two inversions are added to the feedback path, slowing it down. This translates to using /Q instead of Q in the R equation, and defining the R input as being falling-edge triggered (Figure 10). DeMorganization will affect the number of product terms required, but the nine available terms will generally be sufficient.

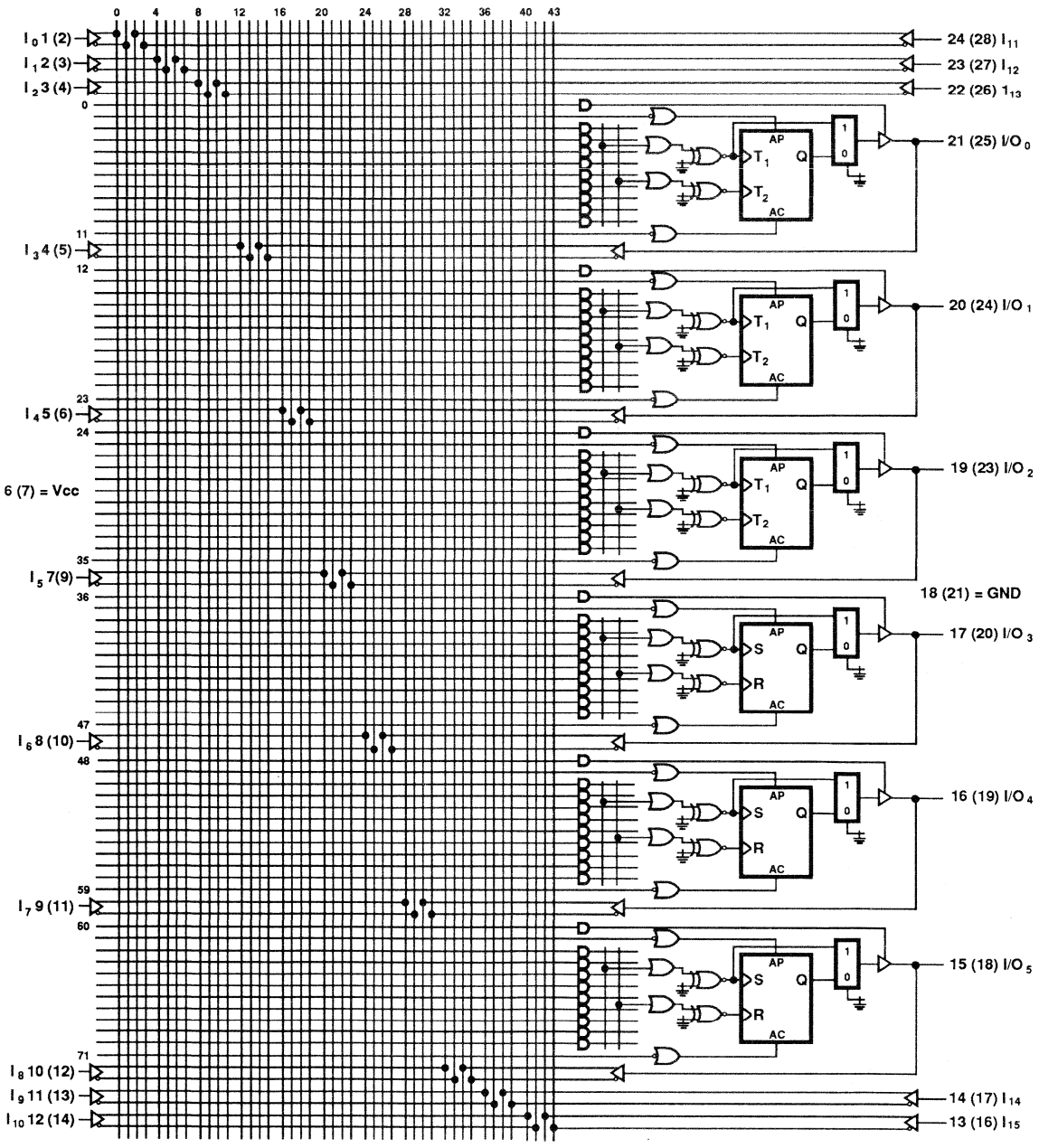


/Q.R := /Q ; allowed

Figure 10. DeMorganized equivalent of Figure 8; allowed

Logic Diagram

DIP (PLCC) Pinouts



968 21

2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... –0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... –0.5 V to +V_{CC} Max.
DC Input Voltage ..... –0.5 V to + 5.5 V
DC Input Current ..... –30mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) Operating Free Air ..... 0°C to +75°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.5	V
			I_{OL} = 48 mA (I/O_0, I/O_1, I/O_4, I/O_5)			
			I_{OL} = 64 mA (I/O_2, I/O_3)		0.6	
V_{IH}	Input HIGH Level (Note 1)	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		V
V_{IL}	Input LOW Level (Note 1)	Guaranteed Input Logical LOW Voltage for all Inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Max., I_{IN} = –18 mA			–1.2	V
I_{IH}	Input HIGH Current (Note 3)	V_{CC} = Max., V_{IN} = 2.4 V			25	µA
I_{IL}	Input LOW Current (Note 3)	V_{CC} = Max., V_{IN} = 0.4 V			–250	µA
I_I	Maximum Input Current	V_{CC} = Max., V_{IN} = 5.5 V			100	µA
I_{OZH}	Output Leakage Current (Note 3)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}	V_O = 2.7 V		100	µA
I_{OZL}			V_O = 0.4 V		–350	
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 2)		–50	–225	mA
I_{CC}	Power Supply Current	V_{CC} = Max.			210	mA

Notes: 1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZH} and I_{IH} (or I_{OZL} and I_{IL}).

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 1)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
t_{PD}	Input or Feedback to Non-Registered Output (Note 2)	Active LOW		25	ns
		Active HIGH			
$^*t_{EIO}$	Edge-Activated-Input to Output or Feedback (Notes 4, 5)			25	ns
$^*t_{S-R}$	Differential Time Between E-A-I Edges of S-R Cell (Notes 4, 5)		6	15	ns
$^*t_{2-T}$	Differential Time Between E-A-I Edges of 2-T Cell (Note 4)		10		ns
$^*t_{PW}$	Edge-Activated-Input Pulse Width (Note 4)		17		ns
t_{AP}	Asynchronous Preset to Registered Output			30	ns
t_{APW}	Asynchronous Preset Pulse Width		17		ns
t_{APR}	Asynchronous Preset Recovery Time		10		ns
t_{AC}	Asynchronous Clear to Registered Output			30	
t_{ACW}	Asynchronous Clear Pulse Width		17		
t_{ACR}	Asynchronous Clear Recovery Time		10		ns
t_{EA}	Input to Output Enable (Note 3)			20	ns
t_{ER}	Input to Output Disable (Note 3)			20	ns

Notes:
1. Commercial Test Conditions: R_1 = 100 Ω, R_2 = 390 Ω (see Switching Test Circuit).
2. t_{PD} is tested with switch S_1 closed and C_L = 50 pF (including jig capacitance). V_{IH} = 3 V, V_{IL} = 0 V, $V_{OH} = V_{OL}$ = 1.5 V.
3. For three-state outputs, output enable times are tested with C_L = 50 pF to the 1.5 V; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high-impedance tests are made to an output voltage of V_{OH} – 0.5 V with S_1 open; LOW to high-impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.
4. The definition of these parameters is in the Special IPAC Timing Parameters section.
5. On the S-R flip-flop, direct active-HIGH feedback from the output to the non-inverting R input is not allowed.

*SPECIAL IPAC TIMING PARAMETERS

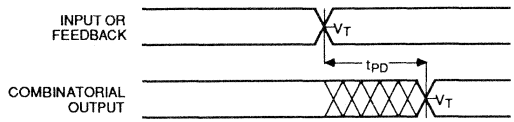
t_{EIO} Edge-Activated-Input to Output Time
The Edge-Activated-Input to Output parameter is defined as the minimum time it takes to obtain a valid data level on the flip-flop output after an Edge-Activated-Input is applied.

t_{S-R} Differential Time between Edge-Activated-Input Edges of S-R Cell
This unique timing parameter, t_{S-R}, is defined as the minimum allowed time between active edges of the two inputs of the S-R flip-flop. If the time between adjacent active edges of these two inputs is greater than or equal to the maximum t_{S-R}, the second Edge-Activated-Input will trigger the flip-flop. If the time between active edges is less than or equal to the minimum t_{S-R}, the second Edge-Activated-Input will not trigger the flip-flop. However, if the time between active edges lies between the minimum and maximum t_{S-R}, the output will be unpredictable.

t_{2-T} Differential Time between Edge-Activated-Input Edges of 2-T Cell
The minimum allowed time between active edges of the two inputs of the 2-T flip flop. If the time between active edges of the two inputs is greater than the minimum t_{2-T}, the output pulse will be measurable. If the time between active edges of the two inputs is smaller than the minimum t_{2-T}, the output pulse will be just a glitch. Since simultaneous inputs will not cause metastability, the purpose of this parameter is to determine the differential time for inputs in order to get a measurable output pulse width.

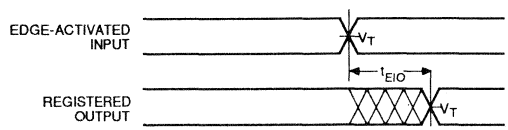
t_{PW} Edge-Activated-Input Pulse Width
The minimum Edge-Activated-Input pulse width required to activate the 2-T or S-R cell.

SWITCHING WAVEFORMS



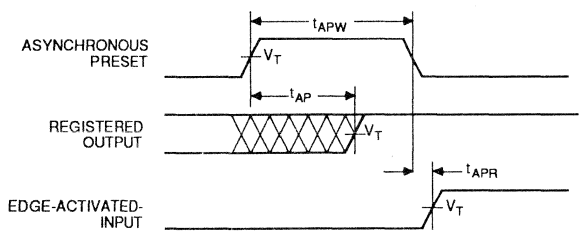
968 10A

Combinatorial Output



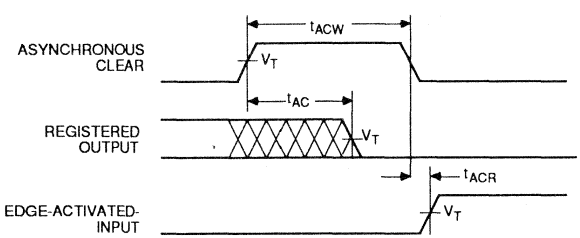
968 10B

Registered Output



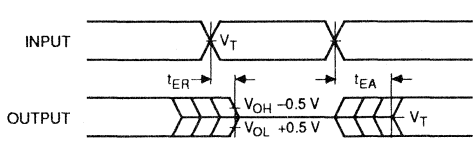
968 10C

Asynchronous Preset



968 10D

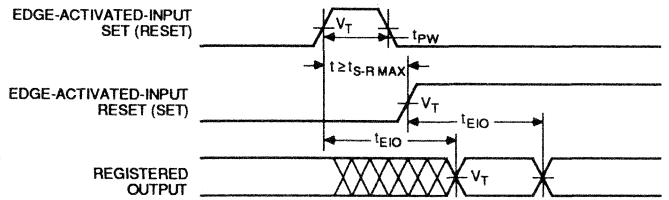
Asynchronous Clear



968 10E

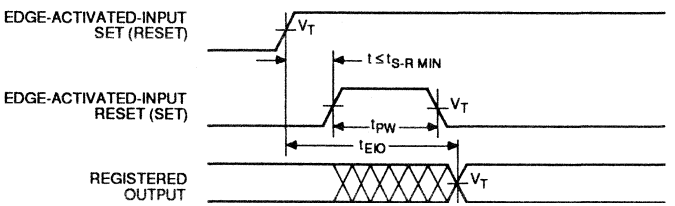
Input to Output Disable/Enable

SWITCHING WAVEFORMS (Cont'd)



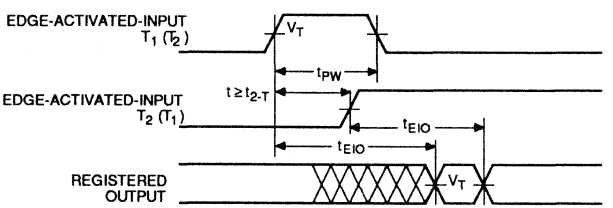
1647C 11

Differential Inputs for S-R Cell (Case 1)



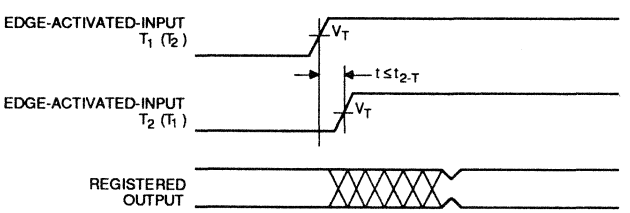
968 12

Differential Inputs for S-R Cell (Case 2)



1647C 13

2-T Cell Timing (Case 1)

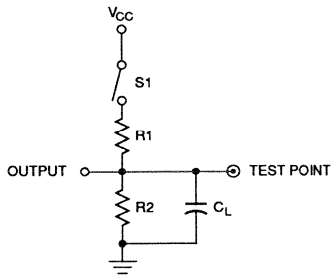


1647C 14

2-T Cell Timing (Case 2)

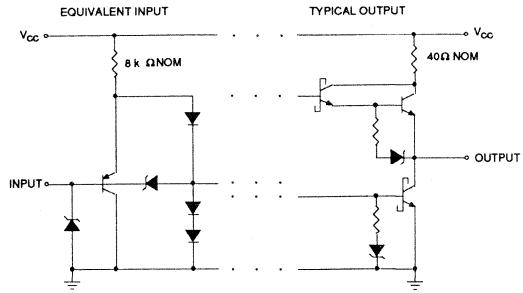
Notes:
1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

SWITCHING TEST CIRCUIT



968 15

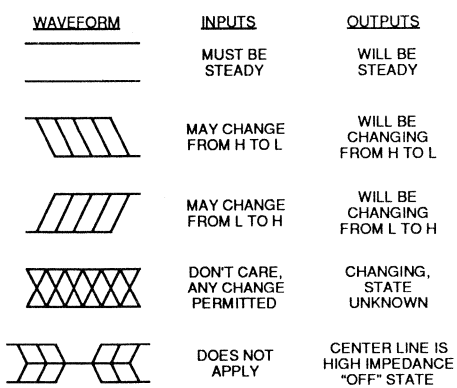
INPUT/OUTPUT DIAGRAM



1647C 16

Specification	Switch S1	C_L	R_1	R_2	Measured Output Value
t_{PD}; t_{EIO}	Closed	50 pF	100 Ω	390 Ω	1.5 V
t_{EA}	Z→H: open Z→L: closed	50 pF	100 Ω	390 Ω	1.5 V
t_{ER}	H→Z: open L→Z: closed	5 pF	100 Ω	390 Ω	H→Z : V_{OH} – 0.5 V L→Z : V_{OL} + 0.5 V

Key to Switching Waveforms



968 07

APPLICATION DESCRIPTION

The IPAC PAL device is ideal for interfacing two system components with different asynchronous protocol signals. In other words, handshake protocol signals of two peripherals, a processor and a peripheral, two processors, etc., which are not synchronized to a common clock, are ideal candidates for IPAC designs.

The two types of IPAC registers, the edge-activated S-R register and the edge-activated Dual-T type register, not only can simplify asynchronous designs but also offer increased system performance over conventional solutions. They also eliminate the need for synchronizing the asynchronous signals, thereby eliminating instances where metastability can occur and improving system reliability. The next section describes this in detail.

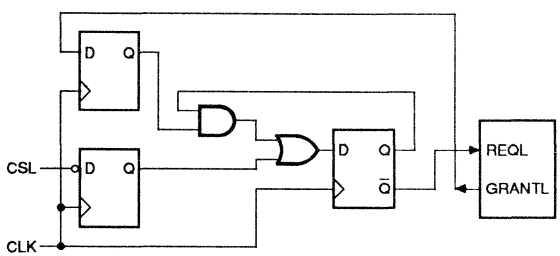
Interface Design Example

The advantage of the IPAC flip-flops is to enhance the system performance. The IPAC flip-flops eliminate the need for a clock, and consequently the need to synchronize asynchronous signals. In conventional designs such synchronization requires two extra clock cycles to mitigate the effects of metastability. The following example of a simple request/grant-type interface protocol illustrates the two major advantages of the IPAC PAL device.

The example interfaces a microprocessor to a peripheral using a request/grant handshake protocol. The microprocessor generates a chip-select (CSL) signal which is transformed to a peripheral-request (REQL) signal. The peripheral responds by generating a grant (GRANTL) signal, at which time the microprocessor removes its REQL signal.

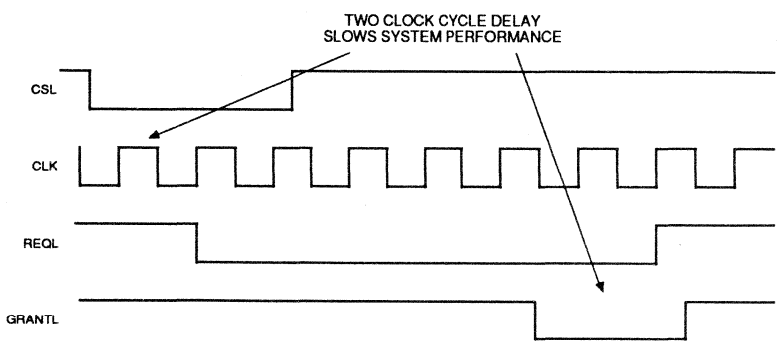
The conventional approach is to register the microprocessor CSL signal to generate a much longer REQL signal. It requires three registers and a clock to implement the design. The GRANTL signal is used to remove the REQL signal. This also requires two clock cycles.

2



968 18

Figure 12. Conventional Solution



968 19

Figure 13. Timing Diagram of a Simplified REQ/GRANT Protocol

The IPAC PAL device uses the falling edge of the CSL signal to generate the request (Figure 14) without the danger of metastability. It also removes its REQL signal on the falling edge of the GRANTL signal, again without any risk of metastability. In both instances the output signal responds to the input without the two-clock cycle delay, thereby improving system performance. Table 2 describes the advantages of using the IPAC device versus standard TTL Logic (74FXXX) and the PAL20R8B.

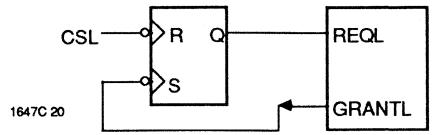


Figure 14. The IPAC Solution

	74FXXX	PAL20R8B	IPAC
Chip Count Comparison	1	1/3	1/3
Handshake Speed*	50 ns	54 ns	25 ns
Design Complexity	Complex	Complex	Simple
Metastability Possible	Yes	Yes	No

Table 2. Benchmark Comparison for Various Interface Designs
* These numbers apply to both directions of handshake

AmPAL22P10B/AL/A

24-pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 15 ns maximum propagation delay
- Universal combinatorial architecture
- Programmable output polarity
- Programmable replacement for high-speed TTL logic
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The AmPAL22P10 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL22P10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

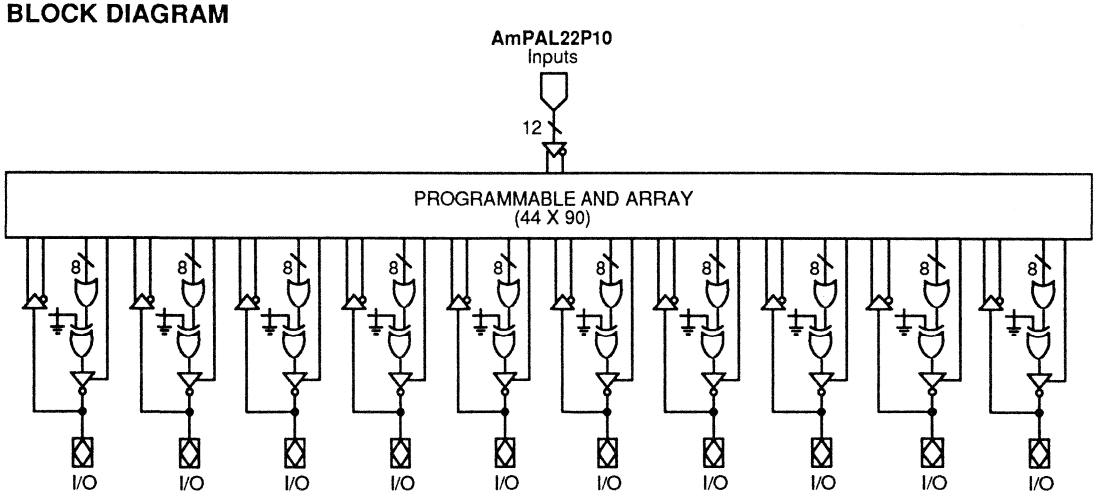
- Variable input/output pin ratio
- Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

2

BLOCK DIAGRAM



12984–002A

Publication # 12984 Rev. D Amendment /0
Issue Date: January 1990

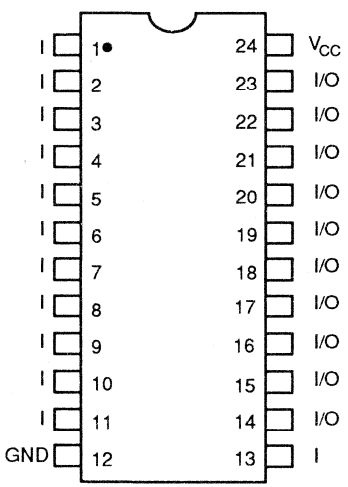
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max.)	I_{CC} mA (Max.)	I_{OL} mA (Min.)
Very High Speed ("B") Versions	15	210	24
High Speed ("A") Versions	25	210	24
High Speed, Half Power ("AL") Versions	25	105	24

CONNECTION DIAGRAMS

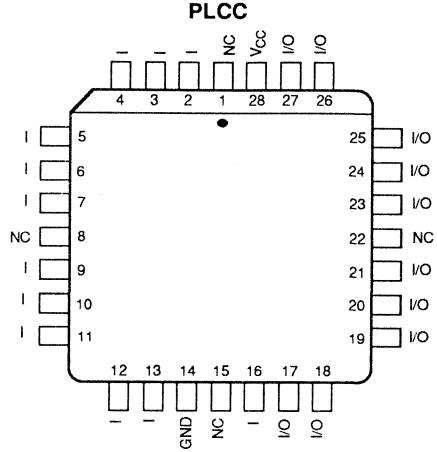
Top View

SKINNYDIP



12984–003A

PLCC



Note:
Pin 1 is marked for orientation

12984–004A

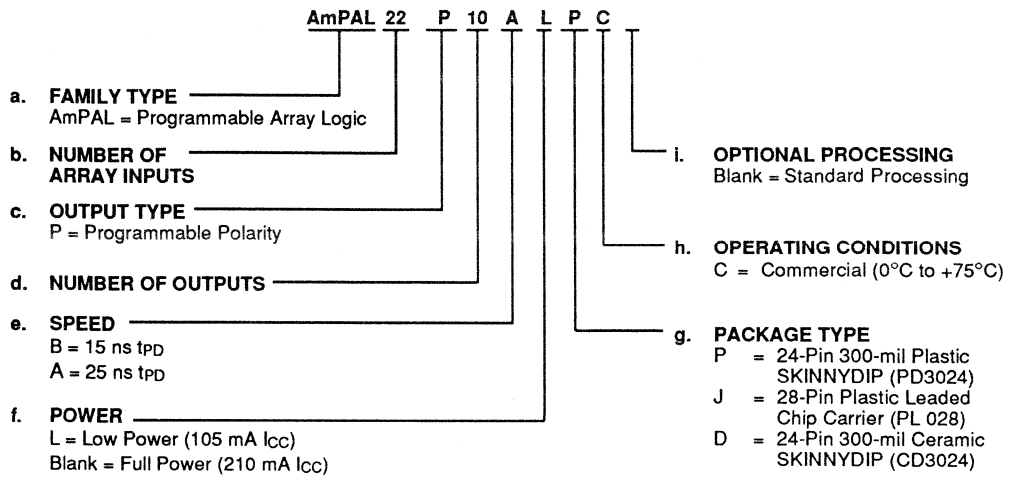
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Power
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations		
AmPAL22P10	B, AL, A	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL22P10 has twelve dedicated input lines, and all ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts. Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL22P10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

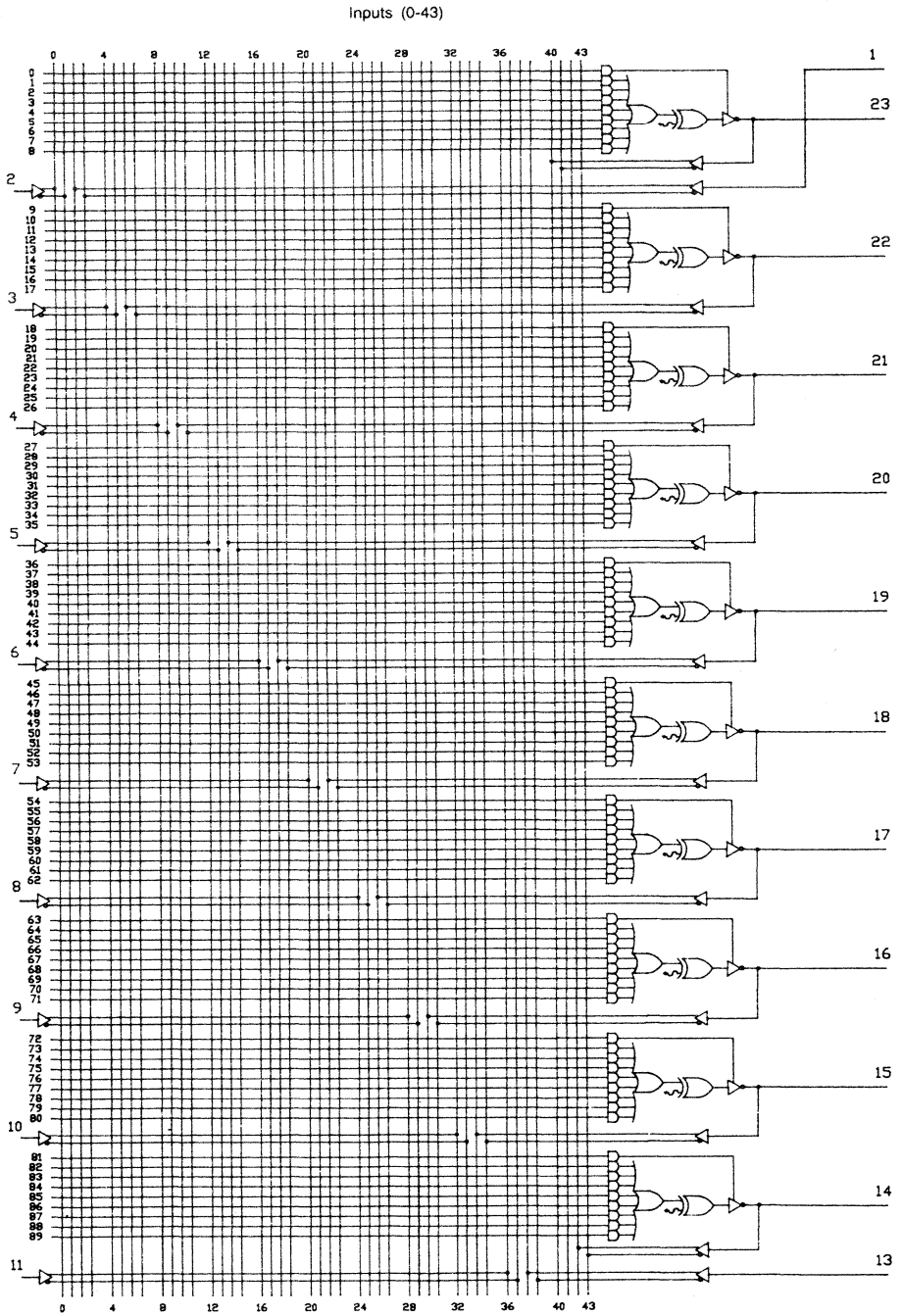
The AmPAL22P10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL22P10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM

AmPAL22P10



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature With Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Input Current	–30 mA to +5 mA
DC I/O Pin Voltage	–0.5 V to V_{CC} Max.
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	B, A		210	mA
			AL		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

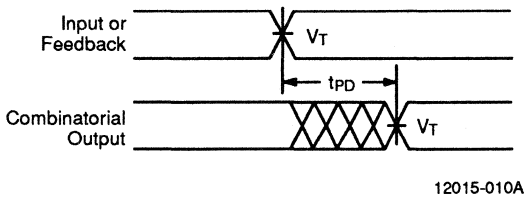
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		25	ns
t_{EA}	Input to Output Enable Using Product Term Control		18		25	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25	ns

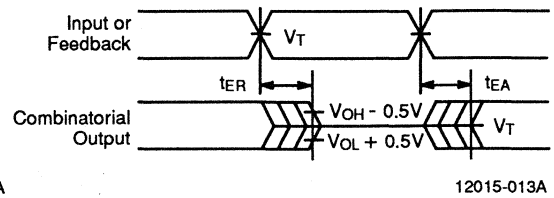
Note:

2. See Switching Test Circuit for test conditions.

SWITCHING WAVEFORMS



Combinatorial Output



Input to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

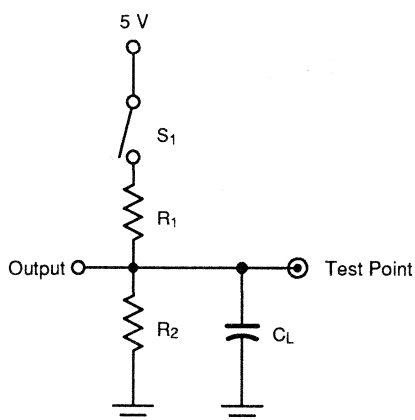
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

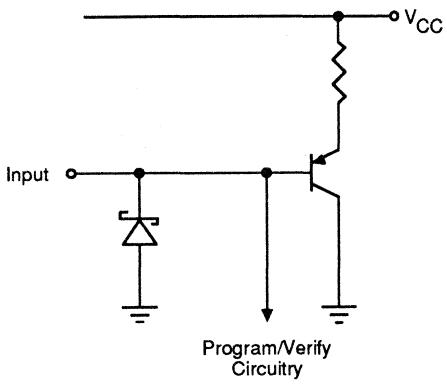


12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

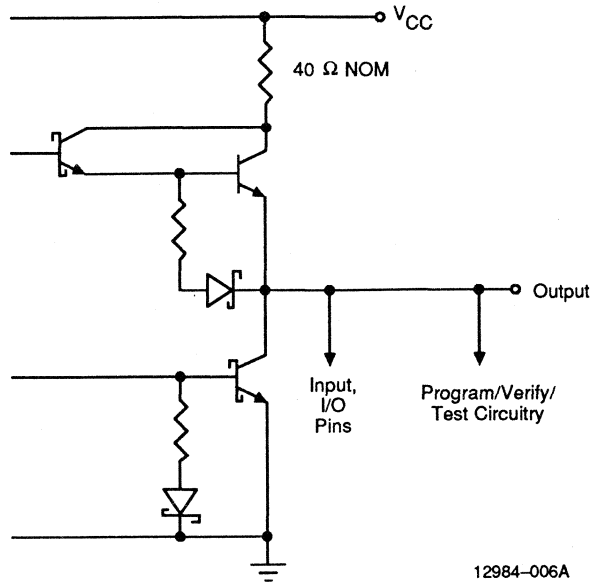
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



12350-020B

Typical Output



12984-006A

PAL22V10-10/15
AmPAL22V10/A
PALCE22V10H-15/25/Q-25

24-pin TTL/CMOS Versatile PAL® Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 10 ns propagation delay and 71 MHz f_{MAX}
- Low-power EE CMOS versions
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

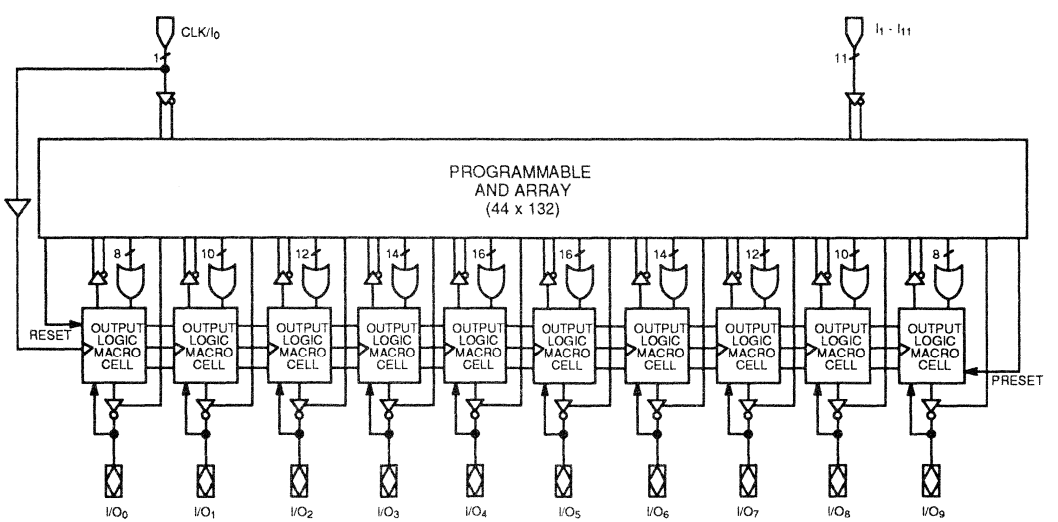
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two fuses controlling two multiplexers in each macrocell.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers.

2

BLOCK DIAGRAM



13003-001A

Publication # 14004 Rev. A Amendment /0
Issue Date: February 1990

PERFORMANCE OPTIONS
Commercial

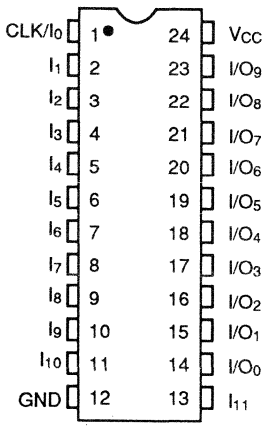
Speed (t_{PD}, ns)	Power (I_{CC}, mA)		
	55	90	180
35			Std
25	CMOS Q-25	CMOS H-25	A
15		CMOS H-15	-15
10			-10

OPERATING RANGES

Commercial	Military
-10	-15
-15	-20
A (25 ns)	A (30 ns)
Std (35 ns)	Std (40 ns)
H-15	H-25
H-25	H-30
Q-25	

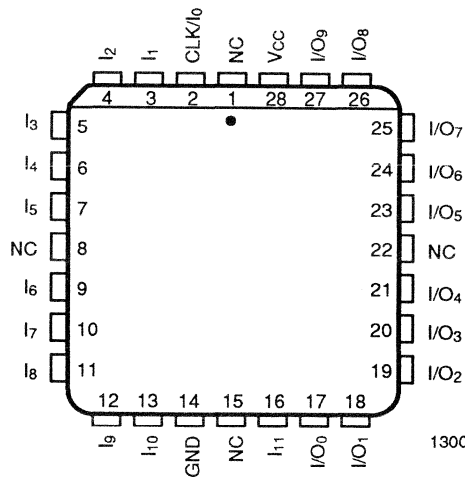
CONNECTION DIAGRAMS
Top View

SKINNYDIP/FLATPACK



13003-002A

PLCC/LCC



13003-003A

Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

2

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Power
g. Speed
h. Package Type
i. Operating Conditions
j. Programming Designator

PAL CE 22 V 10 H -15 P C

a. FAMILY TYPE
PAL or AmPAL = Programmable Array Logic

b. TECHNOLOGY
CE = CMOS Electrically Erasable
Blank = Bipolar

c. NUMBER OF ARRAY INPUTS

d. OUTPUT TYPE
V = Versatile

e. NUMBER OF OUTPUTS

f. POWER
Q = Quarter Power (55 mA I_{CC})
H = Half Power (90 mA I_{CC})
Blank = Full Power (180 mA I_{CC})

g. SPEED
-10 = 10 ns t_{PD}
-15 = 15 ns t_{PD}
-25 = 25 ns t_{PD}
A = 25 ns t_{PD}
Blank = 35 ns t_{PD}

h. PACKAGE TYPE
P = 24-Pin 300-mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
D = 24-Pin 300-mil Ceramic SKINNYDIP (CD3024)

i. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

j. PROGRAMMING DESIGNATOR
Blank = Initial Release
/4 = First Revision
(May require different programmer revisions)

Valid Combinations		
PAL22V10-10	PC, JC, DC	
PAL22V10-15		
AmPAL22V10A		
AmPAL22V10		
PALCE22V10H-15		blank, /4
PALCE22V10H-25		
PALCE22V10Q-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Technology**
c. **Number of Array Inputs**
d. **Output Type**
e. **Number of Outputs**
f. **Power**
g. **Speed**
h. **Programming Designator**
i. **Device Class**
j. **Package Type**
k. **Lead Finish**

PAL CE 22 V 10 H -25 /B L A

a. **FAMILY TYPE**
PAL or AmPAL = Programmable Array Logic

b. **TECHNOLOGY**
CE = CMOS Electrically Erasable
Blank = Bipolar

c. **NUMBER OF ARRAY INPUTS**

d. **OUTPUT TYPE**
V = Versatile

e. **NUMBER OF OUTPUTS**

f. **POWER**
H = Half Power (100 mA I_{CC})
Blank = Full Power (180–200 mA I_{CC})

k. **LEAD FINISH**
A = Hot Solder Dip

j. **PACKAGE TYPE**
L = 24-Pin 300-mil Ceramic SKINNYDIP (CD3024)
K = 24-Pin Ceramic Flatpack (CFL024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL028)

i. **DEVICE CLASS**
/B = Class B

h. **PROGRAMMING DESIGNATOR**
Blank = Initial Release
E4 = First Revision
(May require different programmer revisions)

g. **SPEED**
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}
-25 = 25 ns t_{PD}
-30 = 30 ns t_{PD}
A = 30 ns t_{PD}
Blank = 40 ns t_{PD}

Valid Combinations	
PAL22V10-15	/BLA, /BKA, /B3A
PAL22V10-20	
AmPAL22V10A	
AmPAL22V10	
PALCE22V10H-25	blank, E4
PALCE22V10H-30	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests
Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In
Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PAL22V10 allows the systems engineer to implement the design on-chip, by opening fuse links (or programming EE cells) to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

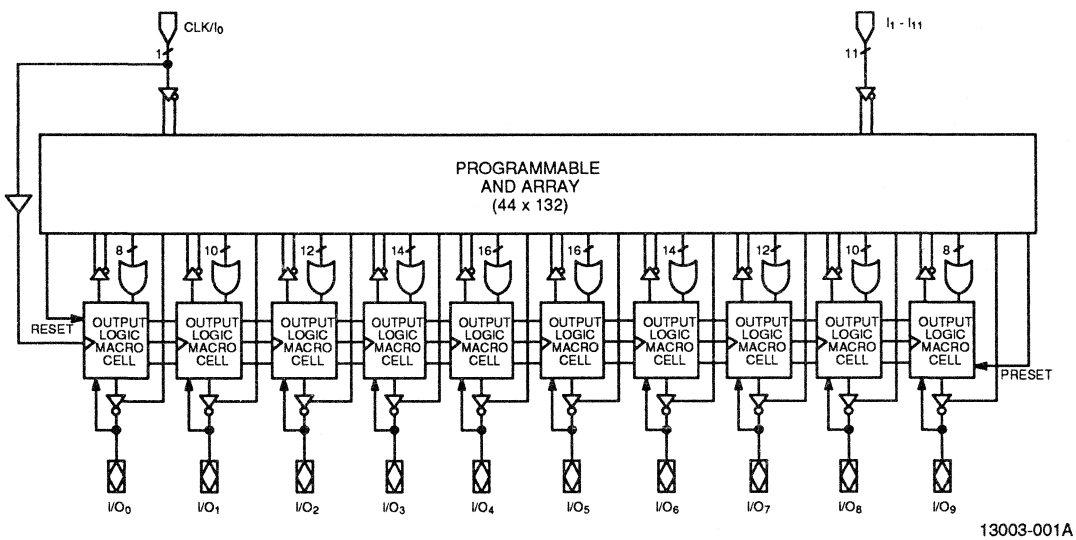
Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PAL22V10 has 12 inputs and 10 I/O macrocells (Figure 1). The macrocell allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Programming the fuse or erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a fuse or EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



13003-001A

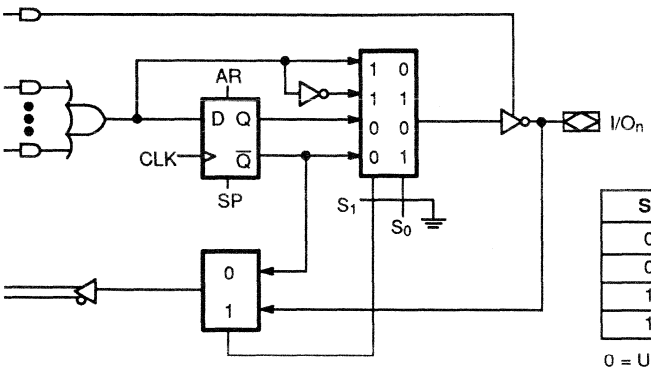
Figure 1. Block Diagram

Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Unprogrammed fuse or programmed EE bit
1 = Programmed fuse or erased (charged) EE bit

13003-004A

Figure 2. Output Logic Macrocell Diagram

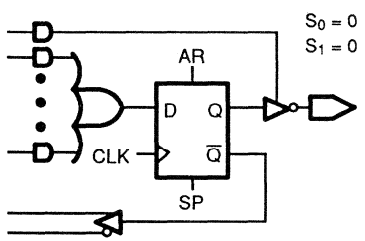


Figure 3a. Registered/Active Low

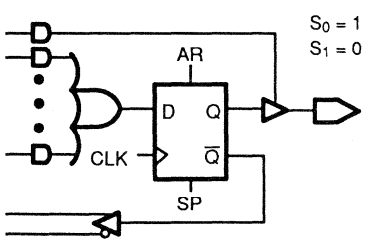


Figure 3b. Registered/Active High

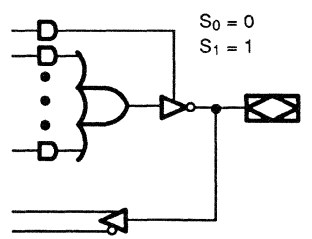


Figure 3c. Combinatorial/Active Low

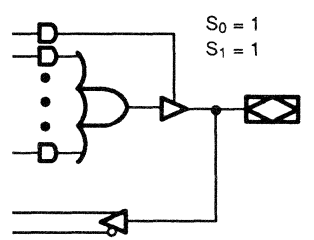


Figure 3d. Combinatorial/Active High

13003-009A

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PAL22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10 µs maximum.

Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse or EE bit. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

For the CMOS PALCE22V10, a floating gate is used as the security bit. The bit can only be erased in conjunction with erasure of the entire pattern.

Quality and Testability

The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

The erasability of the CMOS PALCE22V10 allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The bipolar PAL22V10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation. The PAL22V10-10 uses TiW fuses.

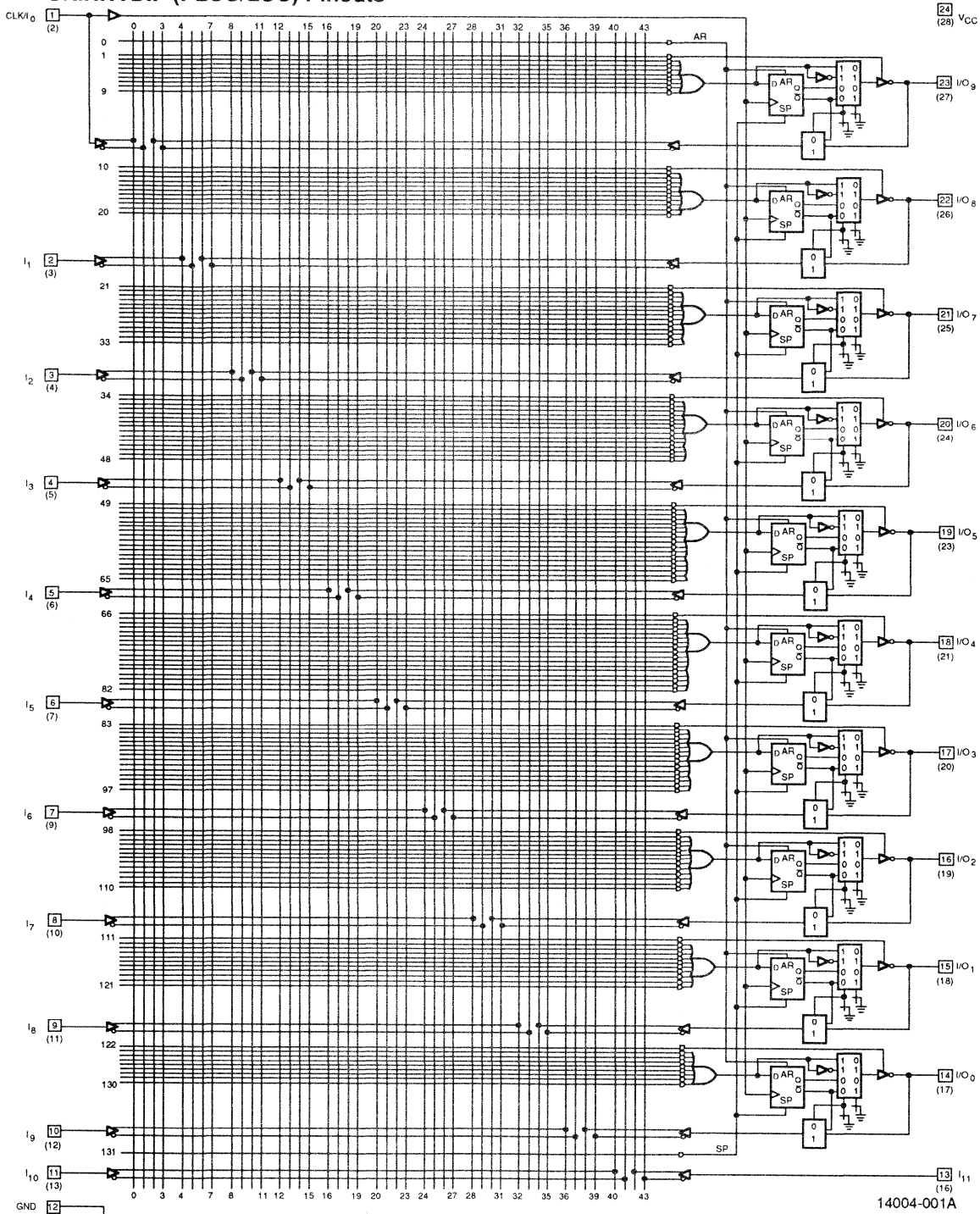
The CMOS PALCE22V10 is fabricated with AMD's advanced EE CMOS process. The array connections are formed by electrically-erasable floating gates similar to those found in EEPROMs.

Programming and Erasing

The PAL22V10 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The CMOS PALCE22V10 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

LOGIC DIAGRAM
SKINNYDIP (PLCC/LCC) Pinouts



14004-001A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage (-10)	–1.2 V to V_{CC} + 0.5 V
DC Input Voltage (-15)	–0.5 V to V_{CC} + 0.5 V
DC Input Current (-15)	–30 mA to + 5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		–10 Typ.	–15 Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	6	9	pF
		Others		T_A = 25°C		6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description			-10 Min. (Note 3)	-10 Max.	-15 Min.	-15 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10		15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			8		10		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output			3	6		10	ns
t_{CF}	Clock to Feedback (Note 4)				2.5		2.5	ns
t_{AR}	Asynchronous Reset to Registered Output				15		20	ns
t_{ARW}	Asynchronous Reset Width			10		15		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		10		ns
t_{SPR}	Synchronous Preset Recovery Time			8		10		ns
t_{WL}	Clock Width	LOW		5		6		ns
t_{WH}		HIGH		5		6		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$	71		50		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	95		80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	100		83		MHz
t_{EA}	Input to Output Enable Using Product Term Control			3	10		15	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10		15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage (-15)	–1.2 V to +7.0 V
DC Input Voltage (-20)	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to +7.0 V
DC Input Current (-20)	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		-15 Typ.	-20 Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	6	9	pF
		Others		T_A = 25°C		6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		20	ns
t_S	Setup Time from Input, or Feedback to Clock			10		17		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{CF}	Clock to Feedback (Note 3 and 4)				2.5		13	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 5)			15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 5)			10		20		ns
t_{SPR}	Synchronous Preset Recovery Time (Note 4)			10		20		ns
t_{WL}	Clock Width	LOW		6		15		ns
t_{WH}		HIGH		6		15		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$	50		31.2		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	80		33.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				15		20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
5. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = 25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			A		Std		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				25		35	ns
– t_S	Setup Time from Input, Feedback or SP to Clock			20		30		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output or Feedback				15		25	ns
t_{AR}	Asynchronous Reset to Registered Output				30		40	ns
t_{ARW}	Asynchronous Reset Width			25		35		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		35		ns
t_{SPR}	Synchronous Preset Recovery Time			20		30		ns
t_{WL}	Clock Width	LOW		15		25		ns
t_{WH}		HIGH		15		25		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	28.5		18		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25		35	ns
t_{ER}	Input to Output Disable Using Product Term Control				25		35	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA
Output Sink Current	100 mA (Note 6)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
6. Not more than one output should sink 100 mA at a time. Duration should not exceed one second.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = 25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			A		Std		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				30		40	ns
t_S	Setup Time from Input, or Feedback to Clock			25		35		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output or Feedback				20		25	ns
t_{AR}	Asynchronous Reset to Registered Output				35		45	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			30		40		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			30		40		ns
t_{WL}	Clock Width	LOW		20		30		ns
t_{WH}		HIGH		20		30		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	22		16.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)				30		40	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				30		40	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage (Except Pin 5)	–0.5 V to V_{CC} + 0.5 V
DC Input Voltage (Pin 5)	–0.6 V to +11.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground (Except H-25)	+4.75 V to +5.25 V
Supply Voltage (V_{CC}) with Respect to Ground (H-25)	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	H		90	mA
			Q		55	

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{CF}	Clock to Feedback (Note 3)				7		13	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		33.3		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage (Except Pin 5)	–0.5 V to V_{CC} + 0.5 V
DC Input Voltage (Pin 5)	–0.6 V to +11.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 5)	–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.		100	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

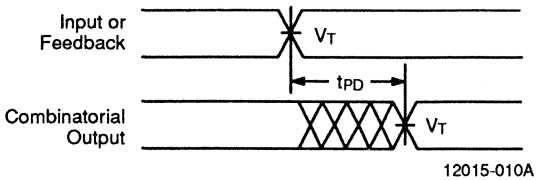
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-25 Min.	-25 Max.	-30 Min.	-30 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				25		30	ns
t_S	Setup Time from Input, Feedback or SP to Clock			20		20		ns
t_H	Hold Time (Note 4)			0		0		ns
t_{CO}	Clock to Output				20		20	ns
t_{CF}	Clock to Feedback (Note 3)				18		18	ns
t_{AR}	Asynchronous Reset to Registered Output				30		35	ns
t_{ARW}	Asynchronous Reset Width (Note 4)			25		30		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)			25		30		ns
t_{SPR}	Synchronous Preset Recovery Time			25		30		ns
t_{WL}	Clock Width	LOW		15		15		ns
t_{WH}		HIGH		15		15		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$	25		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	26		26		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				25		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				25		30	ns

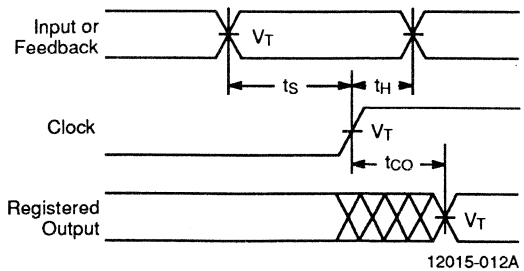
Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 7, 8, 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

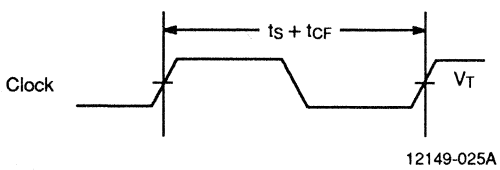
SWITCHING WAVEFORMS



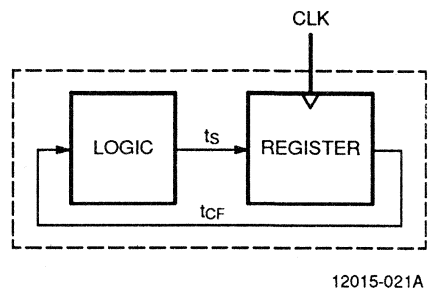
Combinatorial Output

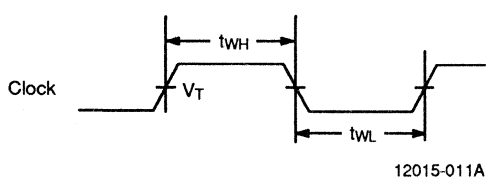


Registered Output

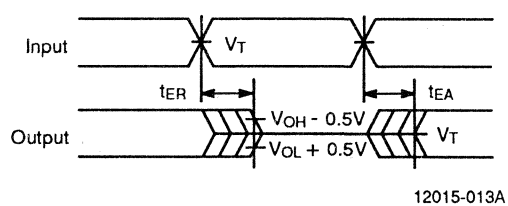


Clock to Feedback (f_{MAX} Internal)
See Path at Right

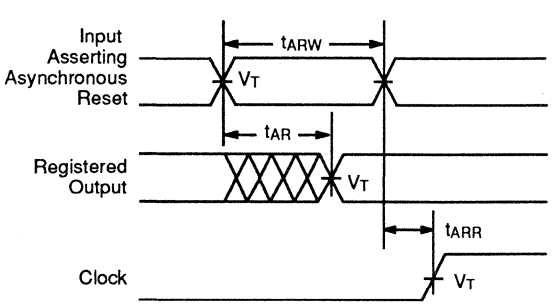




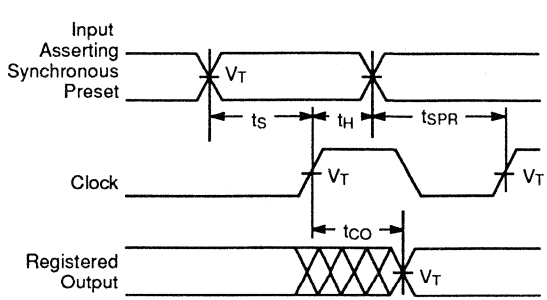
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical. (2–4 ns for 22V10-10)

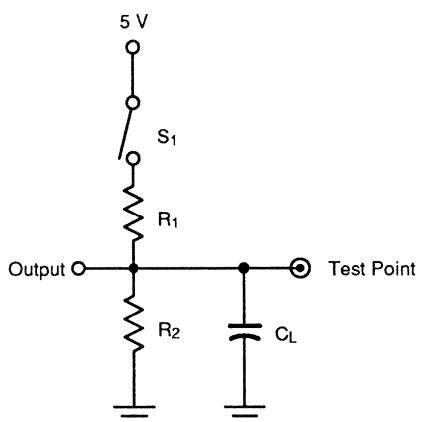
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	Must be Steady	Will be Steady
———		
⟋⟋⟋	May Change from H to L	Will be Changing from H to L
⟋⟋⟋	May Change from L to H	Will be Changing from L to H
⟋⟍⟋⟍	Don't Care; Any Change Permitted	Changing, State Unknown
⟩⟨	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

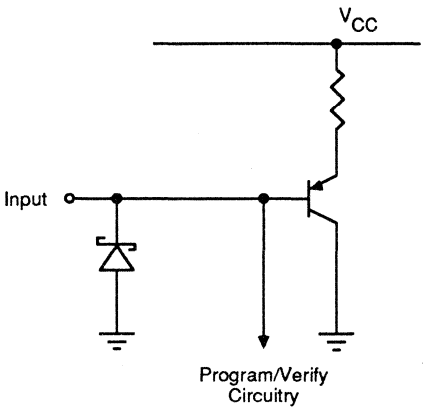


12350-019A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	390 Ω CMOS: 338 Ω	750 Ω CMOS: 248 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

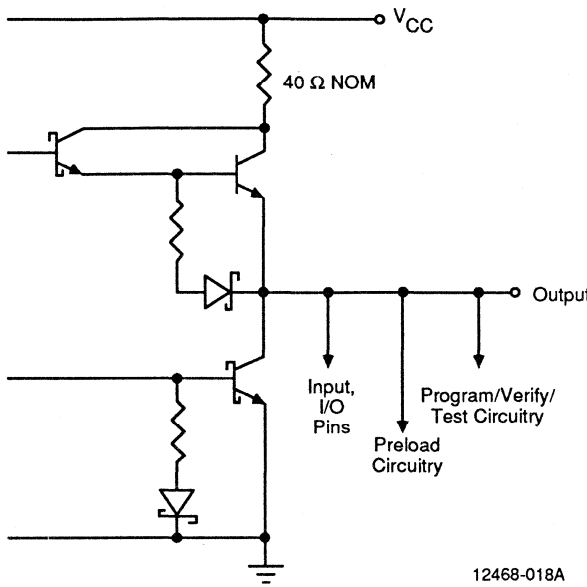
INPUT/OUTPUT EQUIVALENT SCHEMATICS
Bipolar Devices Only

Typical Input



12468-017A

Typical Output



12468-018A

ENDURANCE CHARACTERISTICS

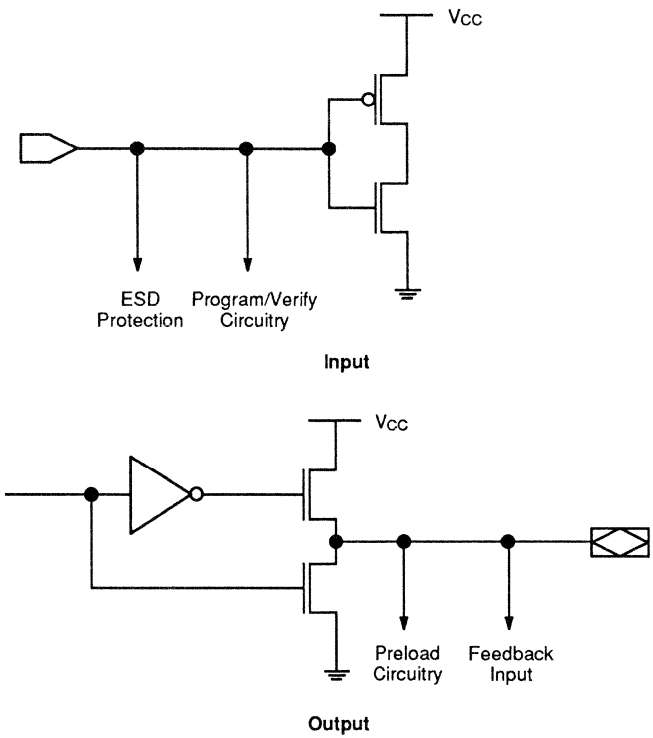
The PALCE22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS

CMOS Devices Only



12197-013A

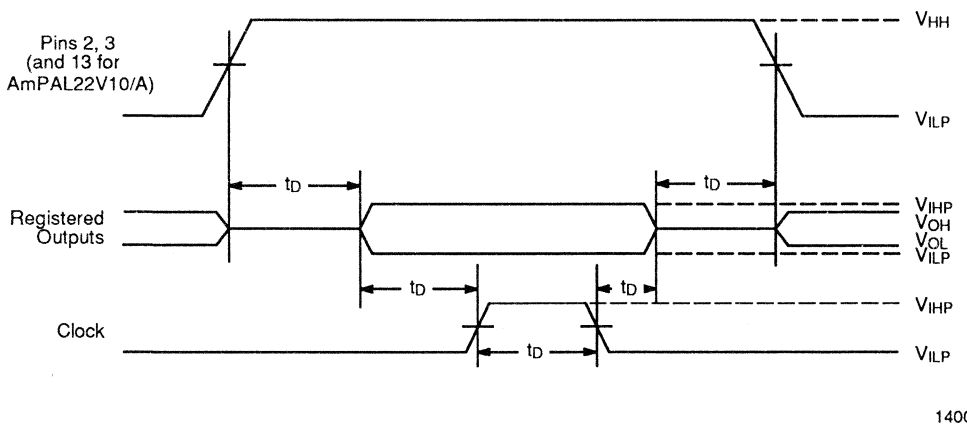
OUTPUT REGISTER PRELOAD

Bipolar Devices Only

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pins 2 and 3 (and 13 for AmPAL22V10/A) to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pins 2 and 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	10	11	12	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns



Output Register Preload Waveform

OUTPUT REGISTER PRELOAD

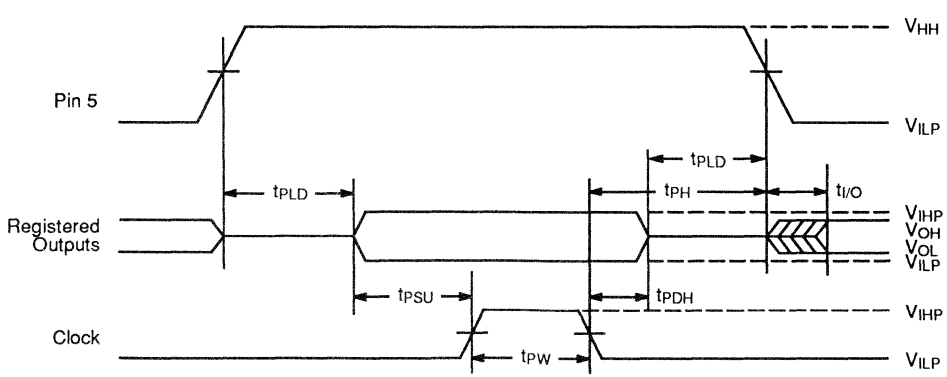
CMOS Devices Only

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pin 5 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 5 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	9.5	10	10.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	3.0	4.0	V_{CC}	V
t_{PLD}	Setup and Hold Data to Preload (Pin 5)	50	50		µs
t_{PSU}	Data Setup Prior to Applying Preload Latch Pulse	1.0	1.0*		µs
t_{PDH}	Data Hold After Latch Pulse	1.0	1.0*		µs
t_{PH}	Mode Hold After Latch Pulse	1.0	1.0*		µs
t_{PW}	Latch Pulse Width	1.0	1.0*		µs
$t_{I/O}$	I/O Valid After Pin 5 Drops from V_{HH} to TTL Levels			100	µs
$\frac{dVr}{dt}$	V_{HH} Rising Slew Rate (Pin 5)	10		100	V/µs
$\frac{dVf}{dt}$	V_{HH} Falling Slew Rate (Pin 5)		2.0	3.0	V/µs

* Recommended value is as close to 1.0 µs + tolerance as practical, but not less than 1.0 µs.



14004-003A

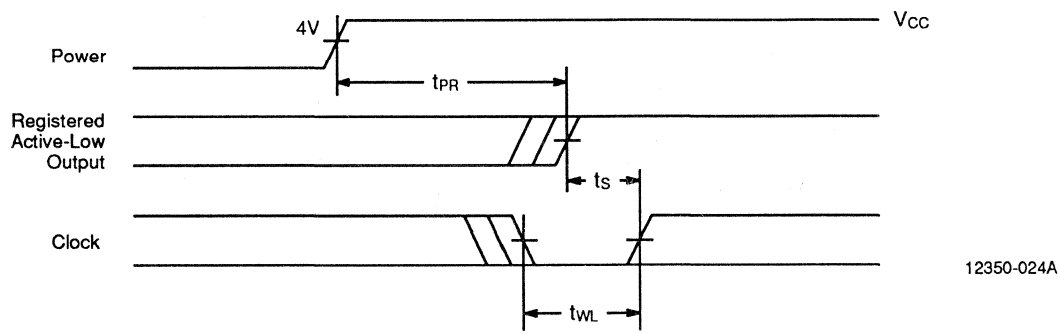
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description		Max.	Unit
t_{PR}	Power-up Reset Time	Bipolar	1	µs
		CMOS	10	
t_S	Input or Feedback Setup Time		See Switching Characteristics	
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

PALCE22V10Z-25

Zero Standby Power 24-pin EE CMOS Versatile PAL® Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero standby power allows battery operation**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Easy design with PALASM® software**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Programmable on standard PAL device programmers**
- **24-pin SKINNYDIP® and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALCE22V10Z is a zero standby power version of the popular PAL22V10 programmable logic device. Zero standby power (100 μA max) and low operating power allow the PALCE22V10Z to be used in battery-powered systems. The PALCE22V10Z is pin-compatible with the other PAL22V10 devices.

The PALCE22V10Z utilizes Advanced Micro Devices' advanced low-power, high-speed EE CMOS technology. The device provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

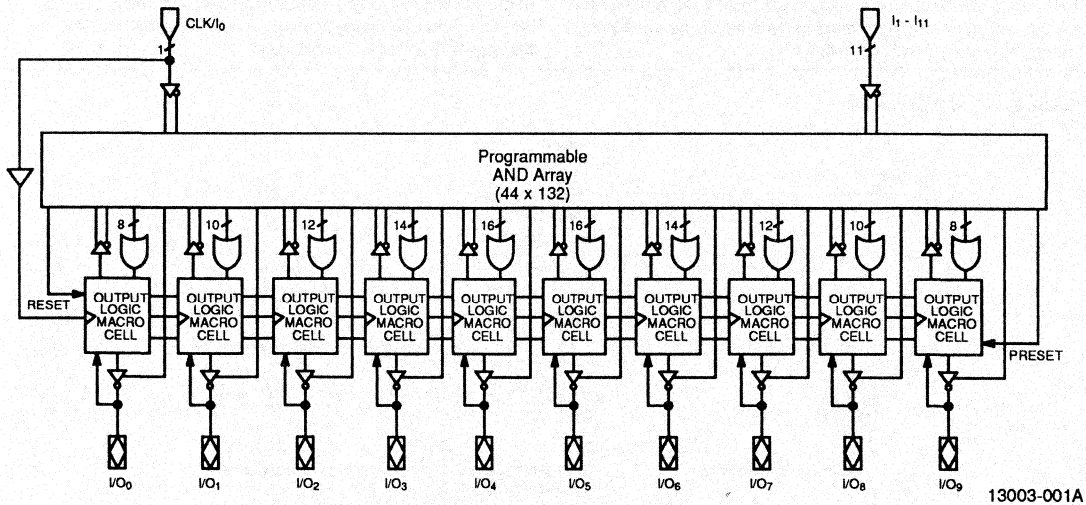
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules.

2

BLOCK DIAGRAM



13003-001A

Publication # 14001 Rev. A Amendment /0
Issue Date: January 1989

Final | COM'L

AmPAL23S8-20/25

20-Pin PAL® Device-Based Sequencer

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 14 Registers
  - 4 Output Logic Macrocells
  - 4 Output Registers
  - 6 Buried State Registers
- 23 possible array inputs and 8 outputs in a 20-pin package
- 33-MHz external/40-MHz internal cycle time
- Variable product term (PT) distribution for increased design flexibility
- Asynchronous and synchronous outputs supported for both Mealy- and Moore-type state-machine implementations
- Individually user-programmable Output Enable (OE) PTs with polarity control
- PTs for observing the buried registers on 6 of the output pins
- Separate PTs for common Synchronous PRESET and common Asynchronous RESET of all registers
- PRELOAD available on all registers for added test capability
- 99.9% post programming functional yield (PPFY)
- Platinum-Silicide fuse technology produces the most reliable bipolar programmable devices available today

GENERAL DESCRIPTION

The AmPAL23S8 is the first programmable array logic (PAL)-based sequencer device. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to customize logic functions by programming the device for specific applications. The AmPAL23S8 combines the ease of use of the familiar 20-pin PAL devices with the advanced "macrocell" concept introduced in the AmPAL22V10, as well as six Buried State Registers (BSRs).

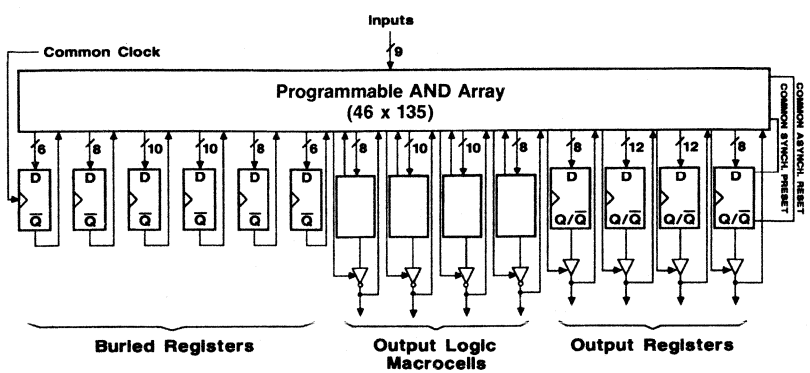
The AmPAL23S8 provides up to twenty-three array inputs and eight outputs. Four of the outputs are Output Logic Macrocells (OLMs) capable of being individually programmed as "combinatorial" or "registered," with active-HIGH or active-LOW polarity on each output. The other four are "registered" outputs, also capable of being programmed for active- HIGH or LOW polarity. All the flexibility on the outputs result in the simplification of logic design. The need to perform "DeMorgan's Law" on equations to have them fit into a PAL device is now a thing of the past. Each of the eight output registers can also be used dynamically as an input or output for greater design flexibility.

The AmPAL23S8 also offers designers increased flexibility and control over Output Enable (OE) functions. Each output is logically controlled by an OE product term (PT), with programmable OE polarity control. This allows the designer to use more complex control than previously available.

The six BSRs provide designers with enhanced logic power for sequencer applications. These registers are not only available to the system designer for use in sequencer applications (without the expense of a valuable I/O pin), but they may also be observed on the output pins during test. The observability of these registers on a programmable-logic sequencer adds to the list of features which make this device unique, simple to design with, and simple to debug.

System operation has been enhanced by the addition of Synchronous PRESET and Asynchronous RESET PTs. The AmPAL23S8 also incorporates the unique capability of PRELOADing the eight output registers and the BSRs to any desired state during testing. This is essential to permit full logical verification during test.

BLOCK DIAGRAM

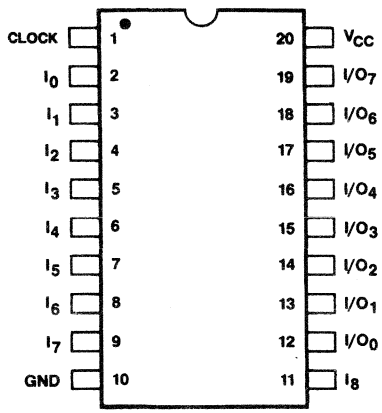


BD006800

Publication # 08207 Rev. E Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAM
Top View

DIP



CD009870

Note: Pin 1 is marked for orientation.

Pin Description

V_{CC} = Supply Voltage

GND = Ground

CLOCK = Clock Pin

$I_0 - I_8$ = Dedicated Input Pins (9)

$I/O_0 - I/O_7$ = Bidirectional I/O Pins (8)

2

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed
C. Package Type
D. Operating Conditions
E. Optional Processing

AMPAL23S8 –20 P C –

E. OPTIONAL PROCESSING
Blank = Standard processing

D. OPERATING CONDITIONS
C = Commercial (0 to + 75°C)

C. PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
D = 20-Pin Ceramic DIP (CD 020)

B. SPEED
–20 = 20 ns
–25 = 25 ns

A. DEVICE NUMBER/DESCRIPTION
AmPAL23S8
20-Pin IMOX PAL-Based Sequencer

Valid Combinations	
AMPAL23S8-20	PC, DC
AMPAL23S8-25	PC, DC

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The AmPAL23S8 is an advanced bipolar programmable array logic (PAL)-based sequencer. It contains a programmable array organized in the familiar sum-of-products structure. The structure of this device makes it particularly ideal for state machine applications. Any design which employs the use of complex state functions is a prime candidate for the AmPAL23S8.

The block diagram on the first page shows the basic architecture of this device; a maximum of 23 array inputs and 8 outputs are available. The inputs are connected to a programmable AND array containing 135 product terms (PTs), of which 124 are logical PTs and 11 are control PTs. Before programming, the AND gates are connected to both the true and complement of every input. By selectively programming fuses, the AND gates may be connected to only the true input, the complement input, or to neither type of input, establishing a logical "don't care". When both the true and complement fuses are left intact, a logical FALSE results on the output of the AND gate. An AND gate with all fuses blown will assume the logical TRUE state. The outputs of the AND gates are connected to OR gates.

Variable Product Term (PT) Distribution

The number of AND gates assigned to each OR gate varies in a fixed manner for each output as shown in the logic diagram (Figure 5). The OR gate outputs feed dedicated registers and macrocells. Each OR gate averages approximately ten PTs for output registers and macrocells. This gives the capability of using from eight to twelve logical PTs on one output in a single clock cycle (no feedback necessary). Buried state registers (BSRs) have an average of eight PTs per OR gate, providing the capability of using from six to ten logical PTs in one BSR in a single clock cycle.

Variable Output Architecture: Output Logic Macrocells (OLMs)

An innovation in logic design is the implementation on the AmPAL23S8 of variable output architecture on four of the outputs. These Output Logic Macrocells (OLMs) are user programmable for a great deal of design flexibility. Each of the four OLMs can be independently programmed for eight distinct configurations. The outputs can be either "registered" or "combinatorial;" they can also be individually programmed for active-HIGH or active-LOW polarity. Finally, the feedback paths which feed through the multiplexer back to the AND array can be programmed so that they originate either from the register or from the I/O pin. From the feedback multiplexer both the true and complement of the output going back to the array are available. All possible configurations of the OLMs are illustrated in Figures 4-1 through 4-8. For maximum flexibility, selection of output polarity and feedback path are kept independent of each other.

Output Registers

In addition to the four OLMs on the AmPAL23S8, there are also four output registers. The data on the output registers may be fed back to the array. When the output is disabled, the pin may be used as an external input. Since each of the eight outputs can obtain feedback from the pins associated with them, all eight of them provide the advantage of being usable dynamically as either inputs or outputs, significantly increasing design flexibility and possibilities.

Buried State Registers (BSRs)

The six observable Buried State Registers are one of the key features of the AmPAL23S8. All BSR outputs are fed back to the AND array, but they do not use up an output pin. The state of each BSR is, however, observable on an associated output pin by activating the user-programmable Observability product term as well as the appropriate Output Enable product term.

The extensive user-programmable flexibility enhances the usefulness of this device for different types of state machine implementations. The possibility exists to create both the Mealy and Moore type of design in the same device.

Programmable Output Polarity

Each output has a user-programmable output polarity fuse which, when blown, indicates that the output will be active HIGH, and when intact, active LOW. The obvious benefit of this enhancement is the increased flexibility of design. With the choice of output polarity, there is no need to DeMorganize equations to fit the device, allowing for more efficient designs both in terms of the amount of time spent in design as well as effective utilization of the device.

For further enhancement of the increased logic power of the AmPAL23S8, each output has a PT to control Output Enable (OE) with programmable polarity.

PRESET/RESET

To improve functionality at the system level, the AmPAL23S8 has additional RESET and PRESET PTs. One PT controls Output Register and BSR PRESET, and one PT controls the RESET for these registers. When the Synchronous PRESET PT is asserted (HIGH), all registers are loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous RESET PT is asserted, all registers are immediately loaded with a LOW, independent of the clock. These functions are particularly useful for applications such as system power-up and RESET.

PRELOAD

In order to simplify testing, the AmPAL23S8 is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. PRELOAD allows any arbitrary "present state" values to be loaded into the OLMs, BSRs and Output Registers of this device. OLM Registers and BSRs are PRELOADed in separate cycles, allowing them to be PRELOADed with different values. Logic verification sequences can be significantly shortened, and all possible state sequences tested, reducing test time and development costs, and guaranteeing proper functionality in system.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way, any state transition can be checked.

It is obvious that to attempt the debugging of a design using BSRs without the benefit of PRELOAD capability would be quite difficult. The combination of this feature and the BSRs

being observable is virtually indispensible for efficient and trouble-free state machine design.

Observability

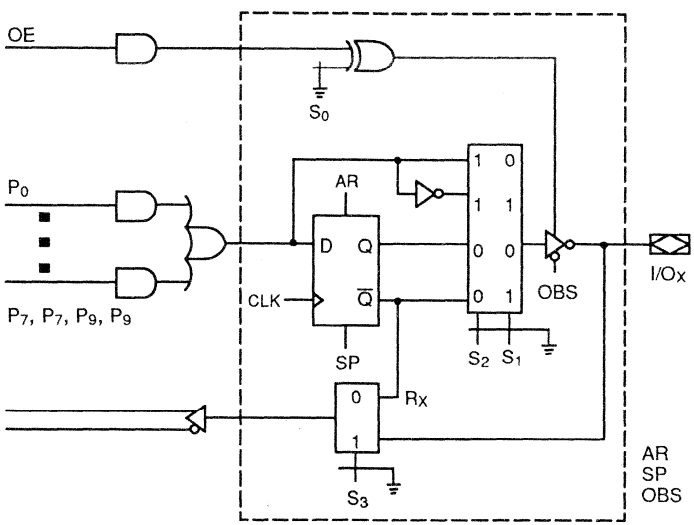
This extra ease of debugging the design comes from the use of the Observability (OBS) PT. The outputs must first be enabled according to the programmed pattern. When the OBS PT is selected, it disables all the Output Registers and Macrocell buffers, and enables the BSR buffers onto the output pins 13 through 18. When the OBS PT is not selected, the Output Registers and Macrocell buffers are enabled and the BSR buffers are disabled. When all the fuses for this PT are intact, (i.e., OBS is not selected), the data from the BSRs will not be visible on the output pins, and the Output Registers and OLMs will be enabled.

Processing and Fuse Technology

The AmPAL23S8 is manufactured using Advanced Micro Devices' IMOX oxide isolation process. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AmPAL23S8 is fabricated with AMD's fast programming, highly reliable Platinum-Silicide fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large, nonconductive gaps that ensure very stable, long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers high reliability for fusible link programmable logic.



AR Common Asynch Reset
SP Common Synch Preset
OBS Common Observability Term

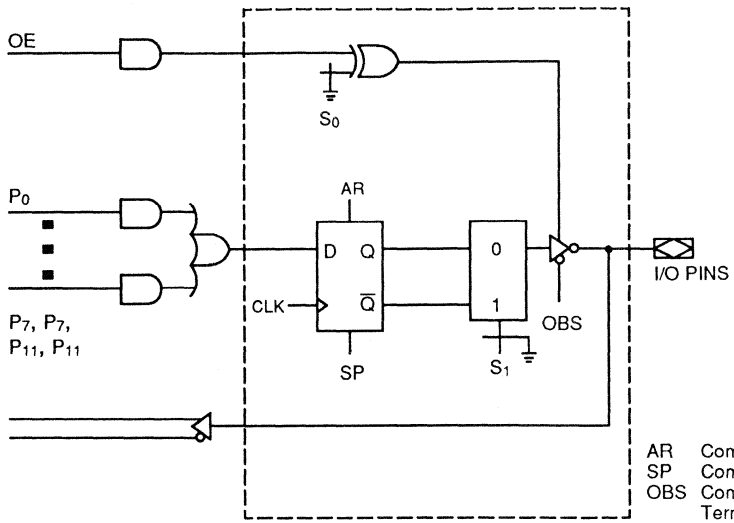
S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

08207-001A

S1	S2	S3	OUTPUT CONFIGURATION
0	0	0	ACTIVE LOW/REG/REG FEEDBACK
0	0	1	ACTIVE LOW/REG/IO FEEDBACK
0	1	0	ACTIVE LOW/COMB/REG FEEDBACK
0	1	1	ACTIVE LOW/COMB/IO FEEDBACK
1	0	0	ACTIVE HIGH/REG/REG FEEDBACK
1	0	1	ACTIVE HIGH/REG/IO FEEDBACK
1	1	0	ACTIVE HIGH/COMB/REG FEEDBACK
1	1	1	ACTIVE HIGH/COMB/IO FEEDBACK

0 = INTACT FUSE
1 = PROGRAMMED FUSE

Figure 1. Output Logic Macrocell (OLM)

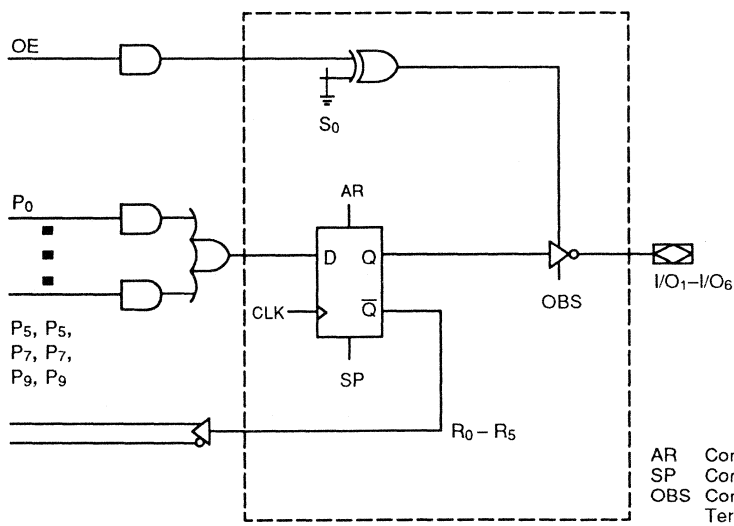


S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

S1	OUTPUT CONFIGURATION
0	ACTIVE LOW
1	ACTIVE HIGH

0 = INTACT FUSE
1 = PROGRAMMED FUSE

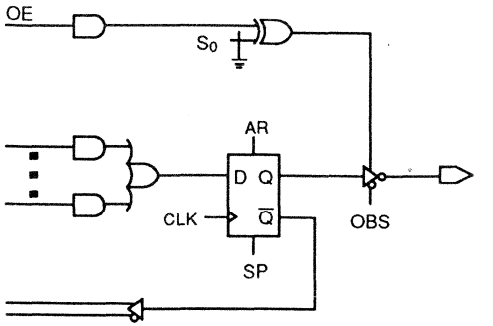
Figure 2. Output Register With Polarity



S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

0 = INTACT FUSE
1 = PROGRAMMED FUSE

Figure 3. Buried State Register (BSR)

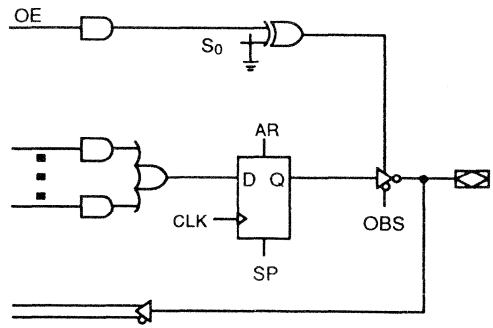


08207-004A

Output
Active Low $S_1 = 0$
Registered $S_2 = 0$

Feedback
Registered $S_3 = 0$

4-1

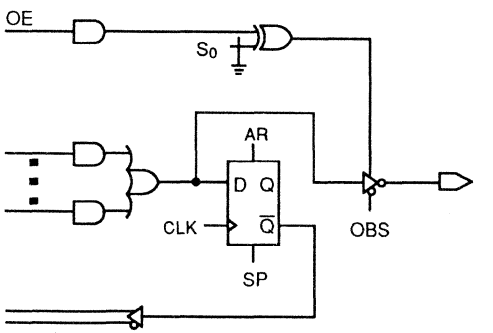


08207-005A

Output
Active Low $S_1 = 0$
Registered $S_2 = 0$

Feedback
I/O Pin $S_3 = 1$

4-2

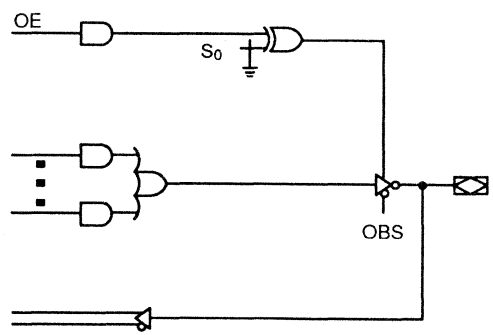


08207-006A

Output
Active Low $S_1 = 0$
Combinatorial $S_2 = 1$

Feedback
Registered $S_3 = 0$

4-3



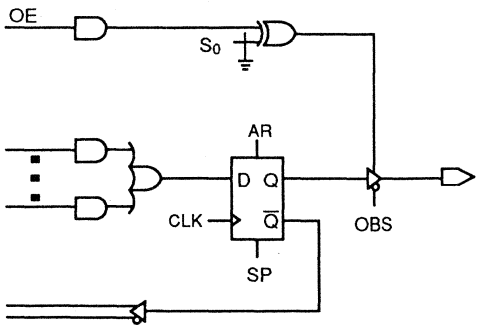
08207-007A

Output
Active Low $S_1 = 0$
Combinatorial $S_2 = 1$

Feedback
I/O Pin $S_3 = 1$

4-4

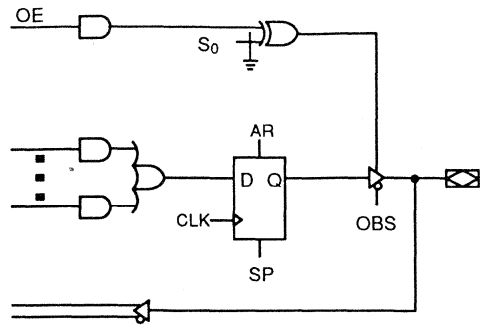
Figure 4. Possible Configurations of the Output Logic Macrocells (OLMs)



Output
Active High $S_1 = 1$
Registered $S_2 = 0$

Feedback
Registered $S_3 = 0$

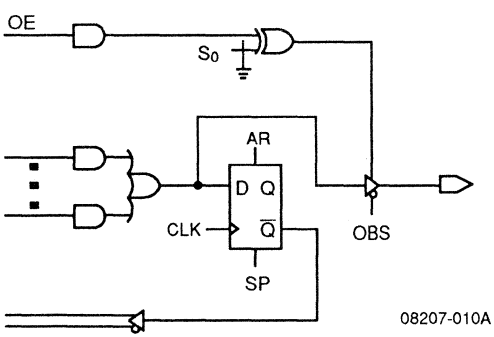
4-5



Output
Active High $S_1 = 1$
Registered $S_2 = 0$

Feedback
I/O Pin $S_3 = 1$

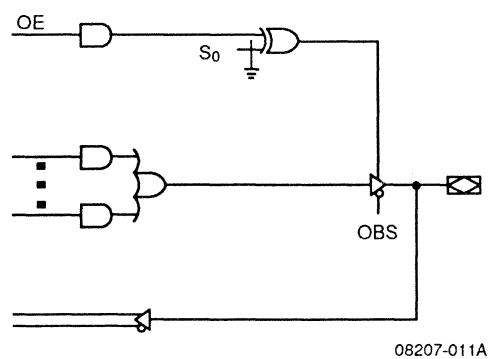
4-6



Output
Active High $S_1 = 1$
Combinatorial $S_2 = 1$

Feedback
Registered $S_3 = 0$

4-7



Output
Active High $S_1 = 1$
Combinatorial $S_2 = 1$

Feedback
I/O Pin $S_3 = 1$

4-8

Figure 4. Possible Configurations of the Output Logic Macrocells (OLMs) (Continued)

LOGIC DIAGRAM
AmPAL23S8

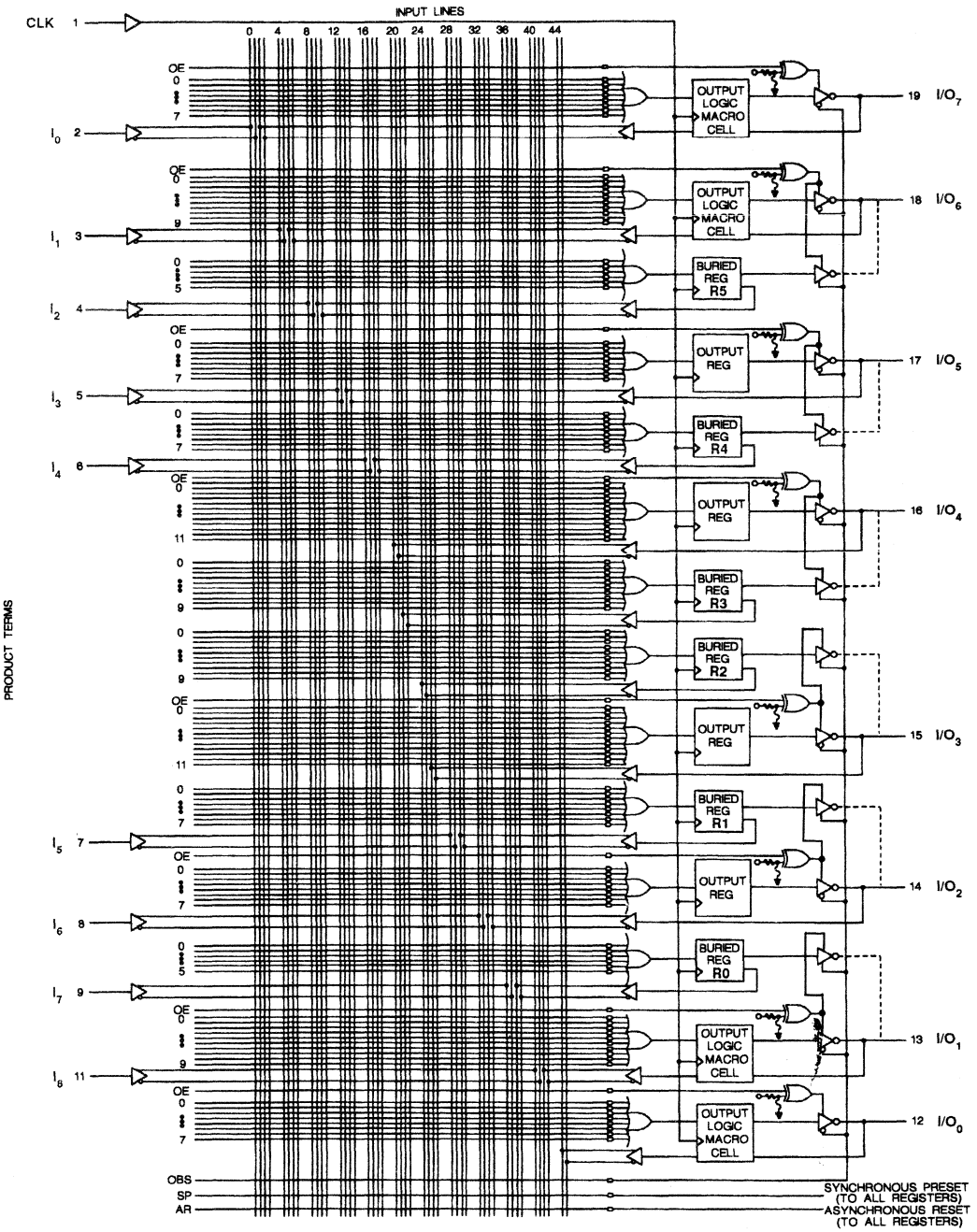


Figure 5.

LD000282

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} Max.
DC Input Current	−30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1,11	V_{IN} = 2.0 V	V_{CC} = 5.0 V	10	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

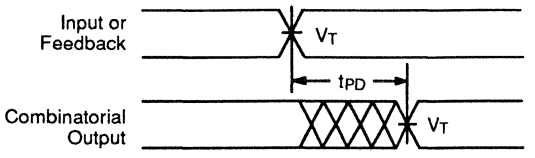
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			17		20		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				13		15	ns
t_{CF}	Clock to Feedback (Note 3)				8		10	ns
t_{AR}	Asynchronous Reset to Registered Output				25		30	ns
t_{ARW}	Asynchronous Reset Width			20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			20		25		ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	33		28.5		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	40		33		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25		28	ns
t_{ER}	Input to Output Disable Using Product Term Control				25		28	ns

Notes:

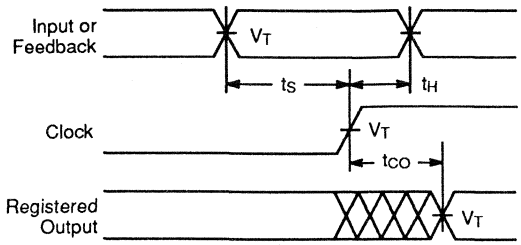
2. See Switching Test Circuit for test conditions.
3. Calculated from measured clock to combinatorial output.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



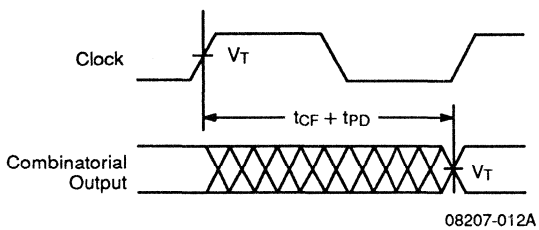
12015-010A

Combinatorial Output



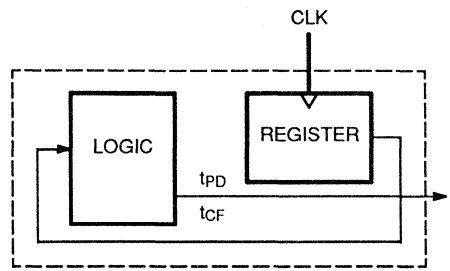
12015-012A

Registered Output

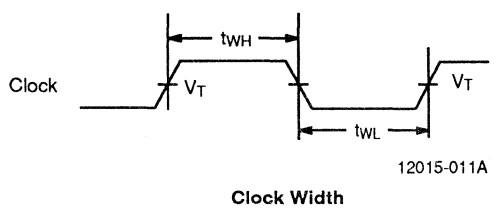


08207-012A

Clock to Feedback
See Path at Right

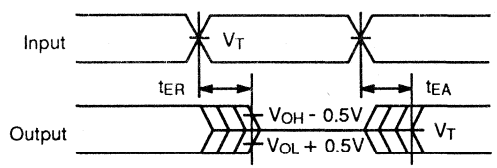


08207-013A



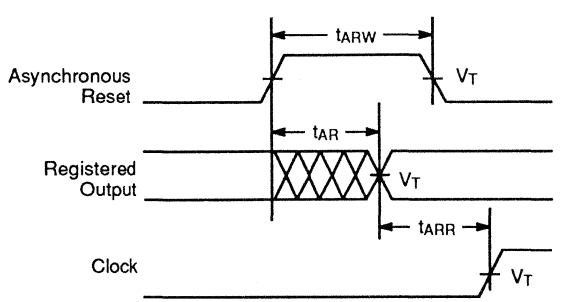
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



08207-014A

Asynchronous Reset

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

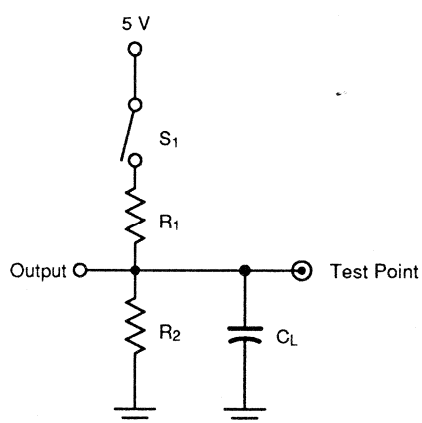
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedence "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

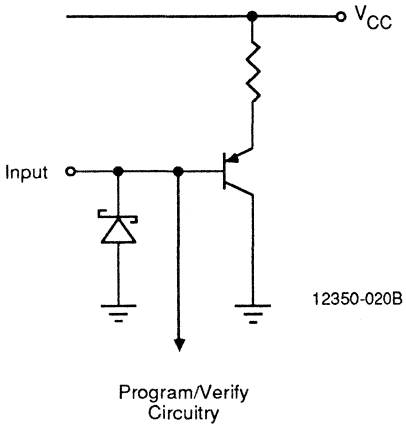


12350-019A

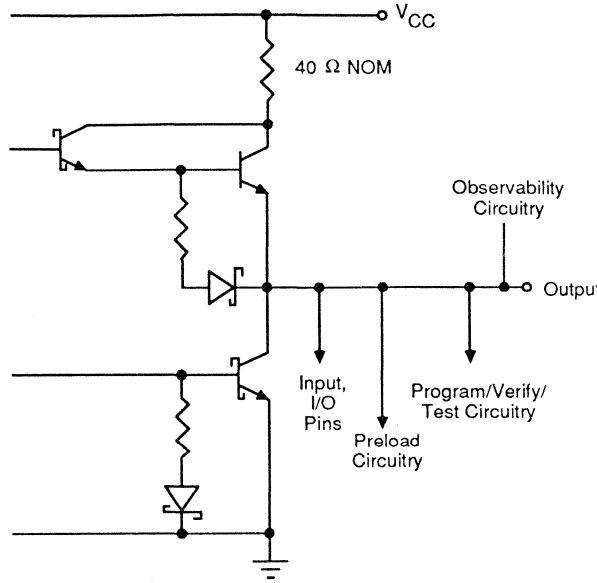
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input

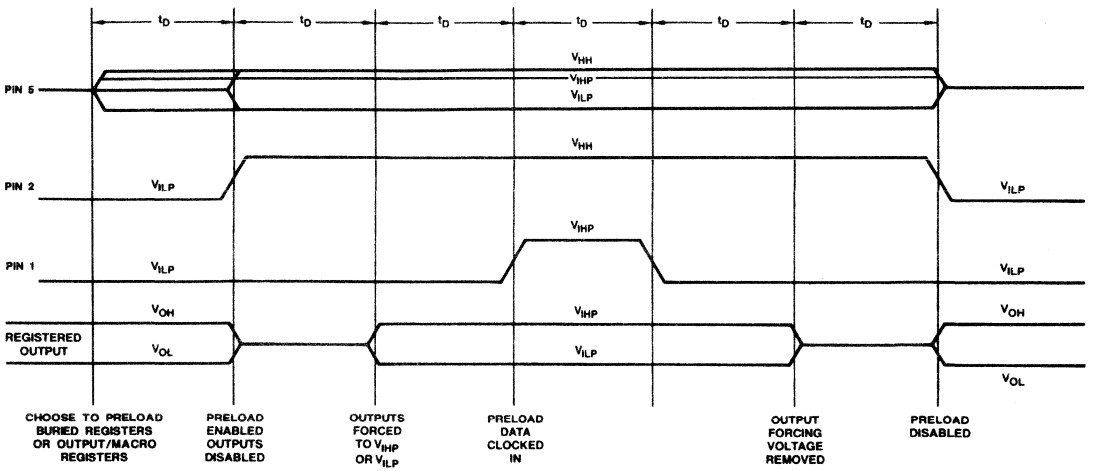


Typical Output



REGISTER PRELOAD

All AmPAL23S8 registers are provided with circuitry to allow loading each register synchronously with a HIGH or LOW. Output/macrocell registers and buried state registers are PRELOADed in separate cycles allowing output/macrocell registers and buried state registers to be PRELOADed with different values. PRELOAD will simplify testing since any state can be loaded into the registers to control testing sequences. The pin levels and timing necessary to perform the PRELOAD function are detailed below.



Par.	Min.	Max.
V_{HH}	10	12
V_{ILP}	0	0.5
V_{IHP}	2.4	5.5

Register Selection	Pin 5
Buried	V_{HH}
Output/Macro	$\leq V_{IHP}$

Level Forced on Register Output Pin During PRELOAD Cycle	Register State After Cycle
V_{IHP}	HIGH
V_{ILP}	LOW

WF022292

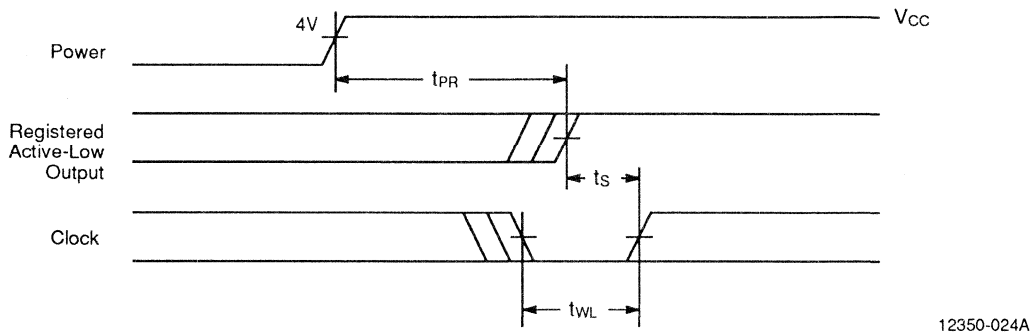
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

2

PAL24R10-10 Series

10 ns 28-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 10 ns maximum propagation delay
- f_{MAX} = 55.5 MHz
- 8 ns maximum from clock input to data output
- Center V_{CC} and GND pins provide clean signals
- 28-pin version of popular architectures: 24L10, 24R10, 24R8, 24R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 28-pin SKINNYDIP® and PLCC packages save space

GENERAL DESCRIPTION

The PAL24R10-10 Series (PAL24L10-10, PAL24R10-10, PAL24R8-10, PAL24R4-10) is a high-speed 28-pin version of the standard PAL16R8 and PAL20R8 Series. With a 10-ns maximum propagation delay time, the PAL24R10-10 Series provides high speed in a 28-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL24R10-10 Series adds two more inputs and two output or I/O pins to the standard 20R8 Series to take advantage of all the pins in the 28-pin PLCC package.

The family utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count. Power and ground have been placed on the center pins of the device, a configuration that minimizes ground bounce.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

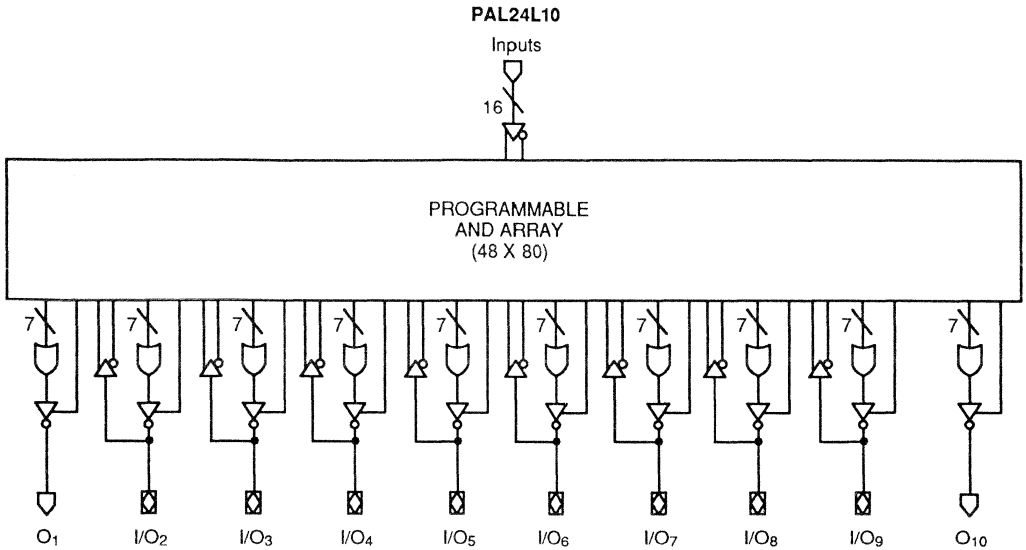
The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL24L10-10	16	8 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL24R10-10	14	10 reg.	8	reg.	pin
PAL24R8-10	14	8 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL24R4-10	14	4 reg. 6 comb.	8 7	reg. I/O	pin prog.

Publication # 12721 Rev. A Amendment /0
Issue Date: January 1990

BLOCK DIAGRAMS



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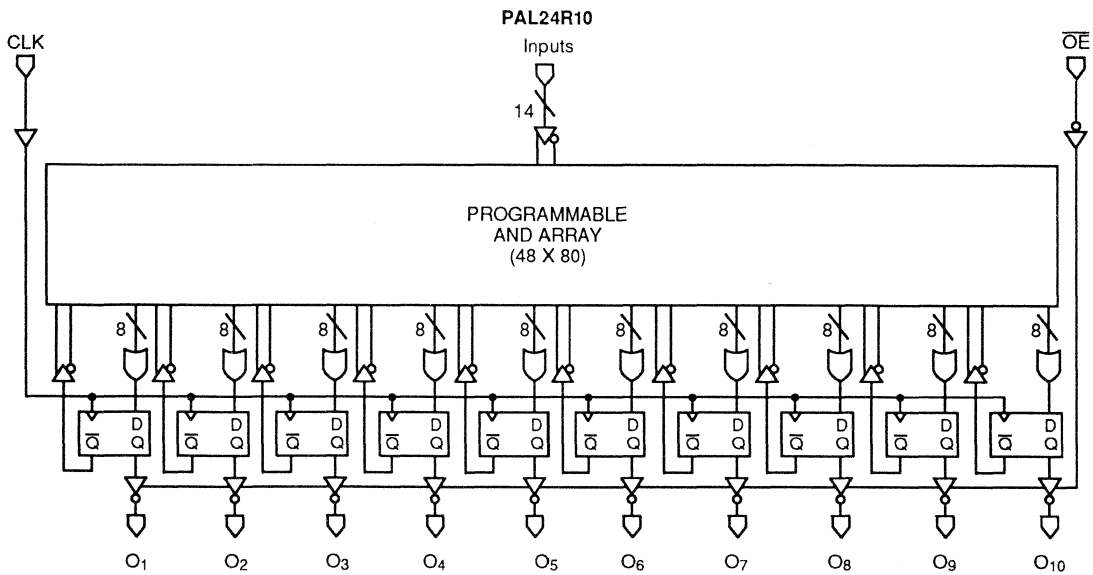
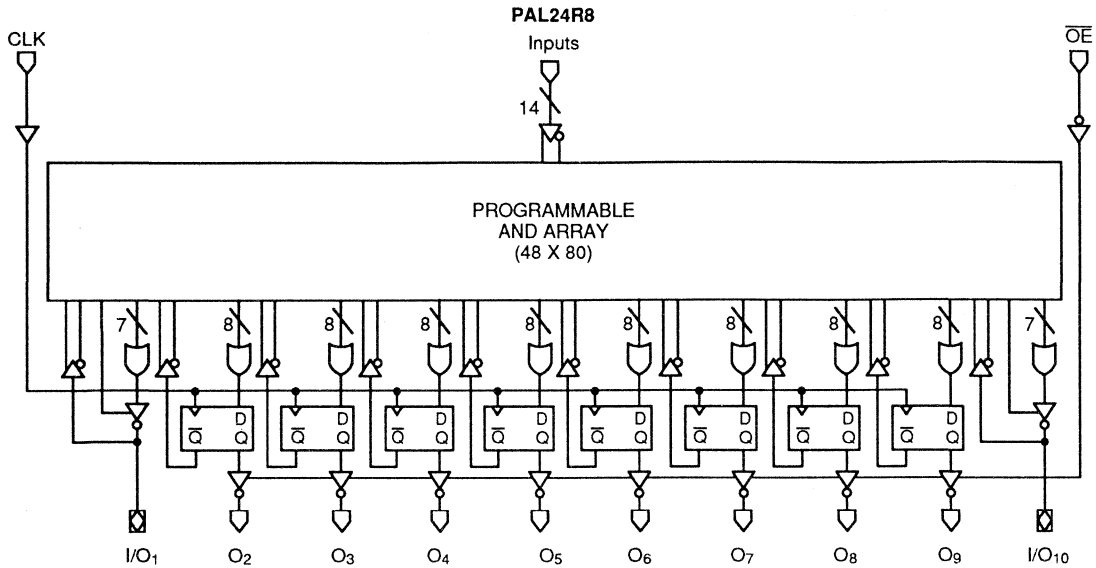
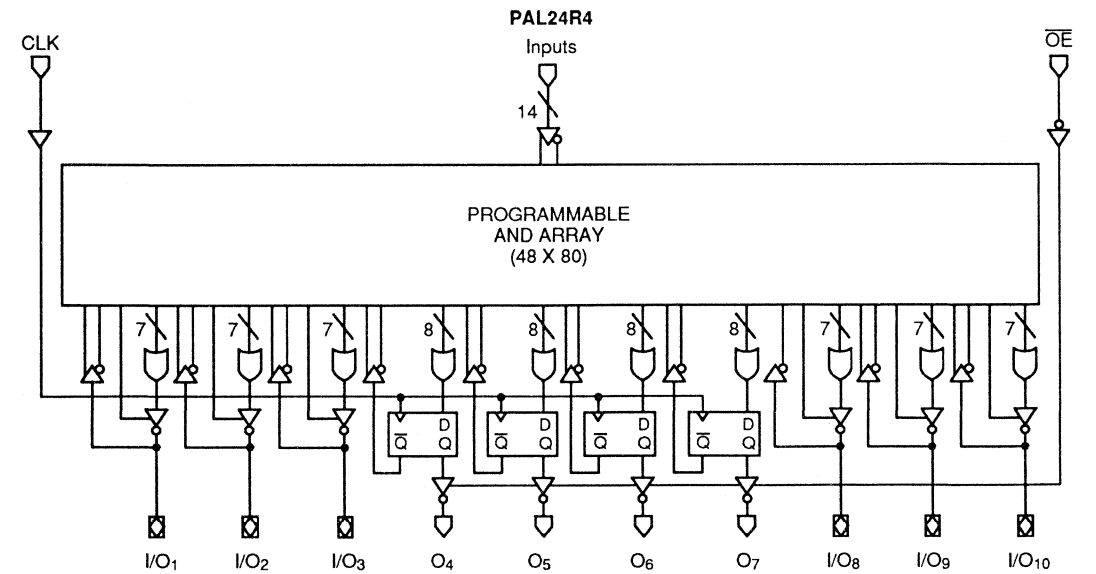


12721-001A

BLOCK DIAGRAMS



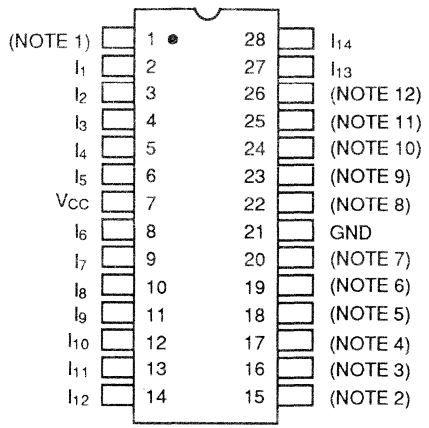
12721-002A



12721-003A

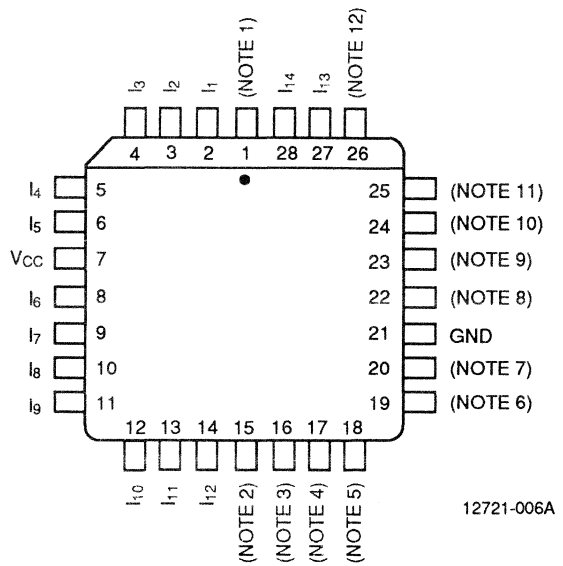
CONNECTION DIAGRAMS
Top View

SKINNYDIP



12721-005A

PLCC



12721-006A

Note	24L10	24R10	24R8	24R4
1	I_0	CLK	CLK	CLK
2	I_{15}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	I/O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	O_7
10	I/O_8	O_8	O_8	I/O_8
11	I/O_9	O_9	O_9	I/O_9
12	O_{10}	O_{10}	I/O_{10}	I/O_{10}

Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

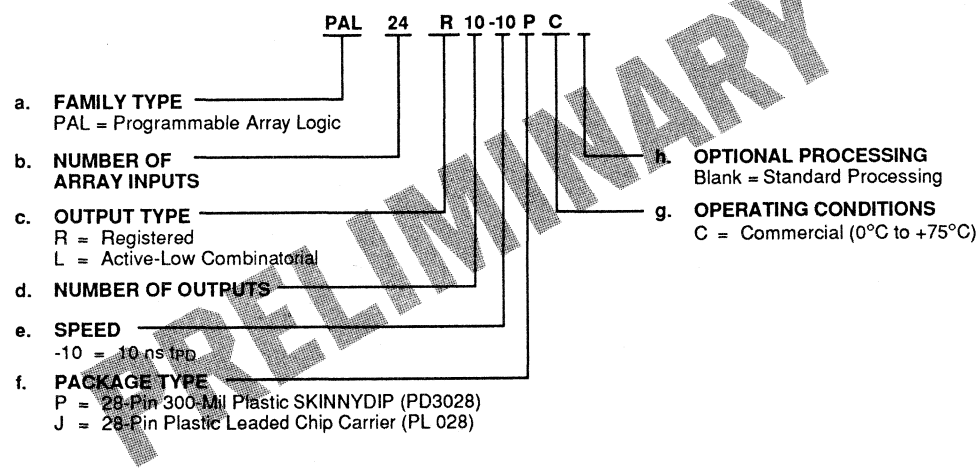
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

2

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Package Type
g. Operating Conditions
h. Optional Processing



Valid Combinations	
PAL24L10-10	PC, JC
PAL24R10-10	
PAL24R8-10	
PAL24R4-10	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Standard 28-pin PAL Family

The standard bipolar 28-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have fourteen dedicated input lines, and each combinatorial output is an I/O pin. The PAL24L10-10 has sixteen dedicated input lines, and eight of the ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL24R10-10 Series will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL24R10-10 Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL24R10-10 Series design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is unprogrammed.

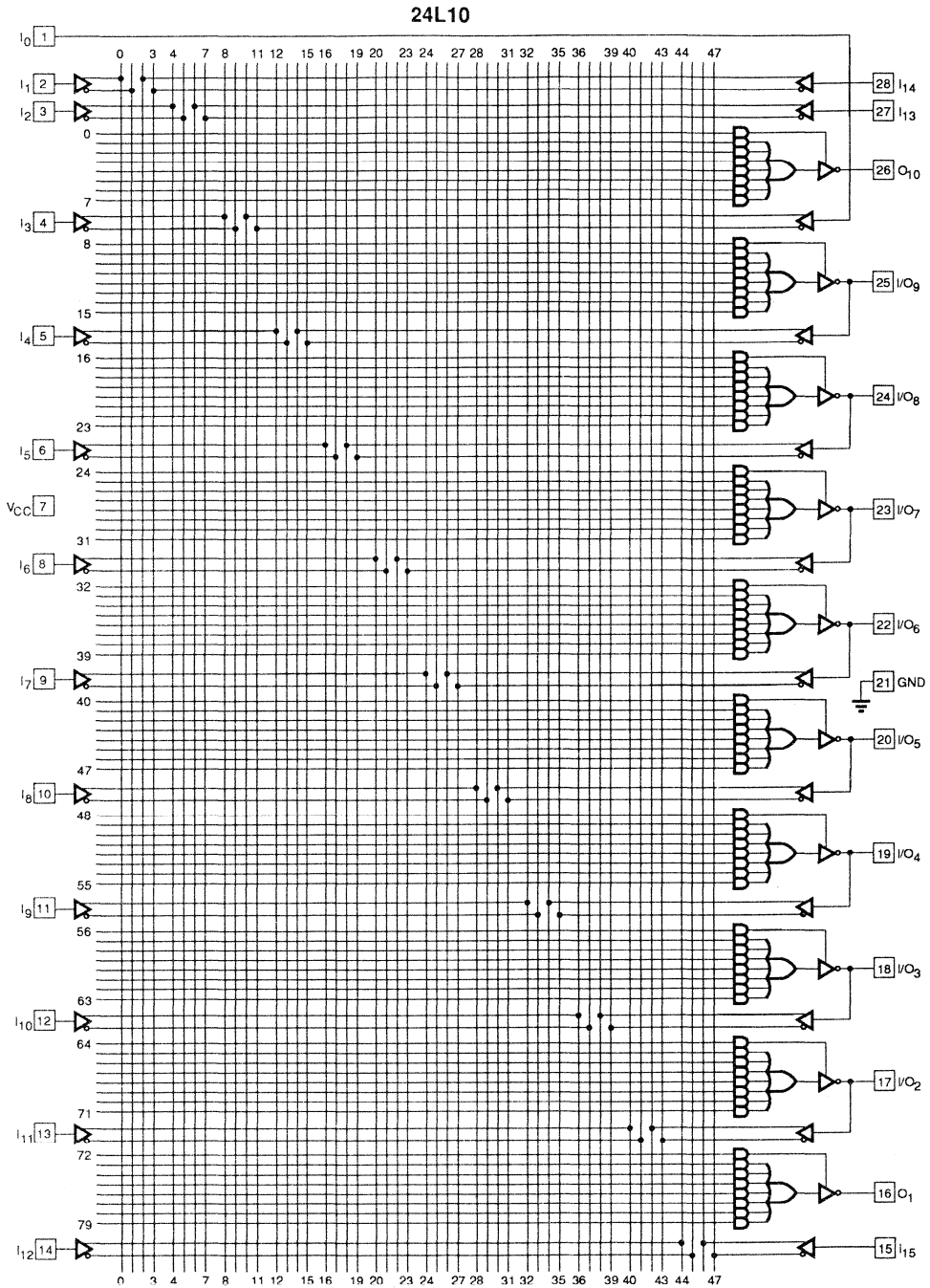
Quality and Testability

The PAL24R10-10 Series offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL24R10-10 Series is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.

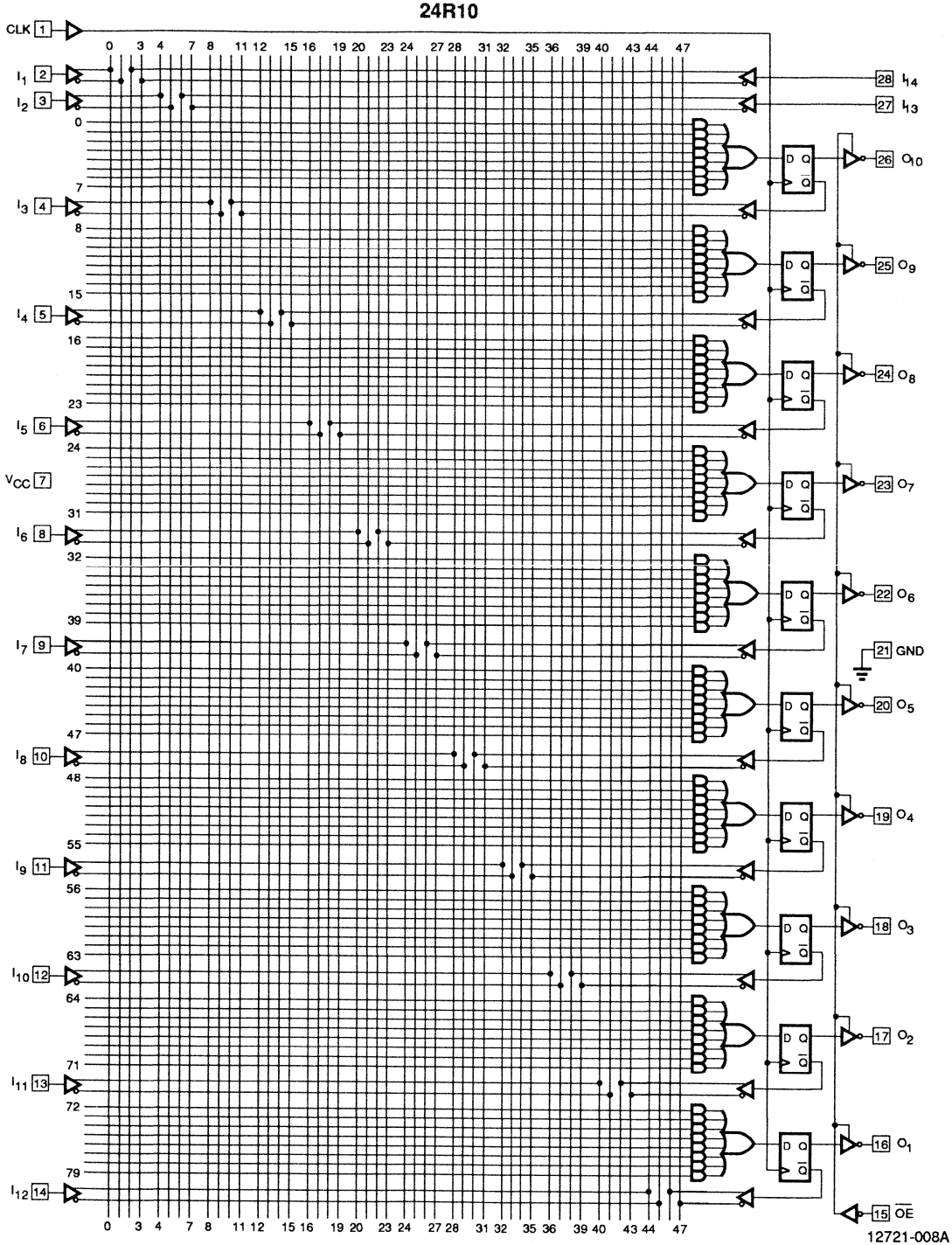
LOGIC DIAGRAM



12721-007A

LOGIC DIAGRAM

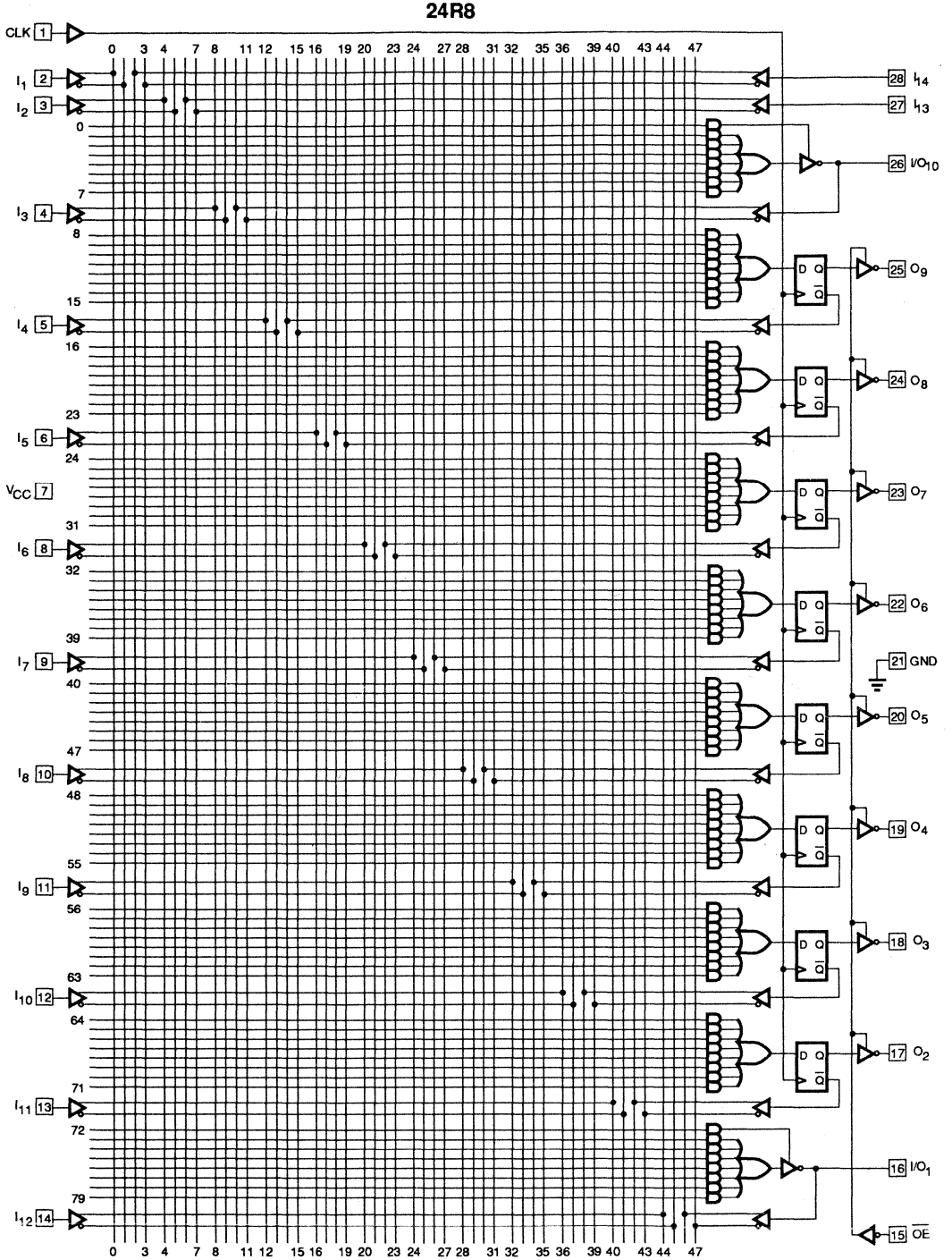
24R10



12721-008A

LOGIC DIAGRAM

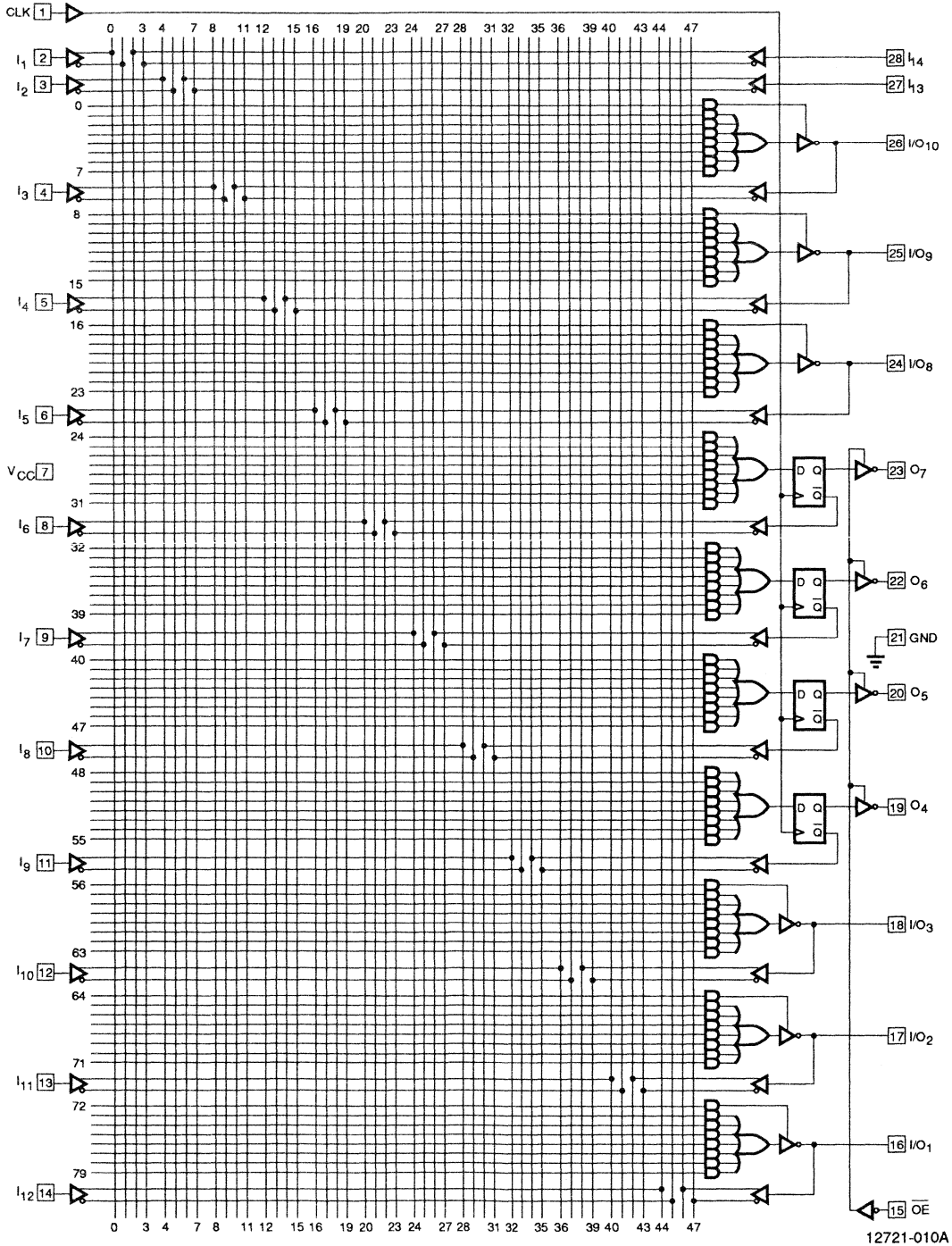
24R8



12721-009A

LOGIC DIAGRAM

24R4



12721-010A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

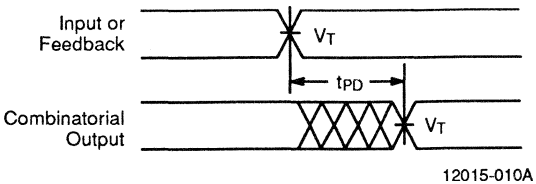
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			24L10, 24R8 24R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock				10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	8	ns
t_{CF}	Clock to Feedback (Note 4)					7	ns
t_{WL}	Clock Width	LOW		24R10, 24R8 24R4	7		ns
t_{WH}		HIGH			7		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		55.5		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		71.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			24L10, 24R8 24R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

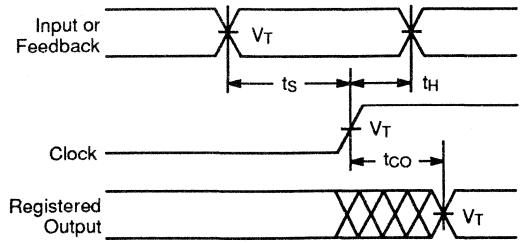
2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

SWITCHING WAVEFORMS



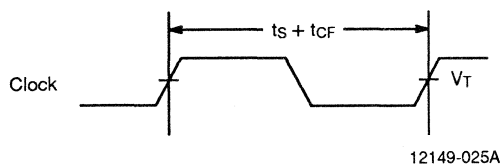
12015-010A

Combinatorial Output



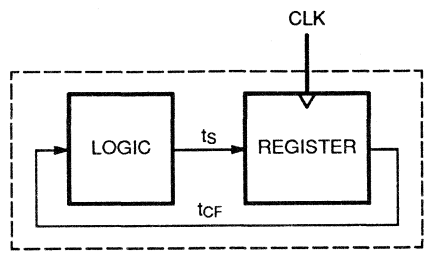
12015-012A

Registered Output

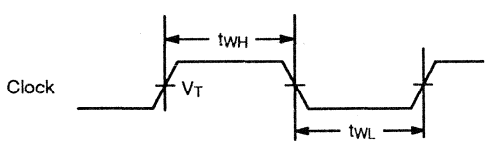


12149-025A

Clock to Feedback (f_{MAX} Internal)
See Path at Right

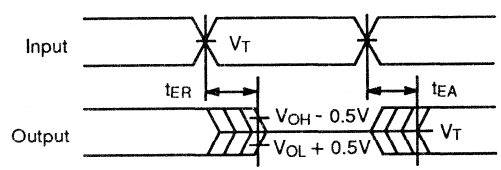


12015-021A



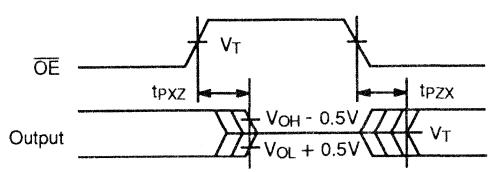
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



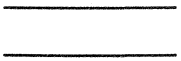
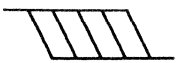
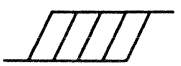
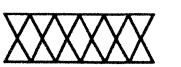
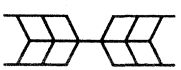
12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

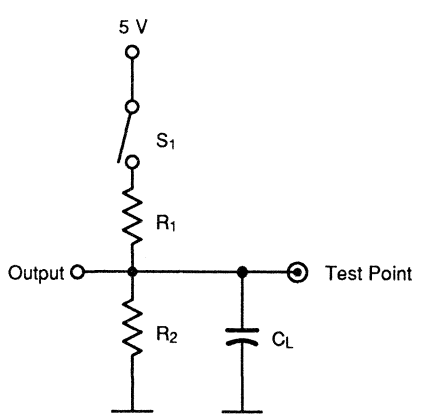
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

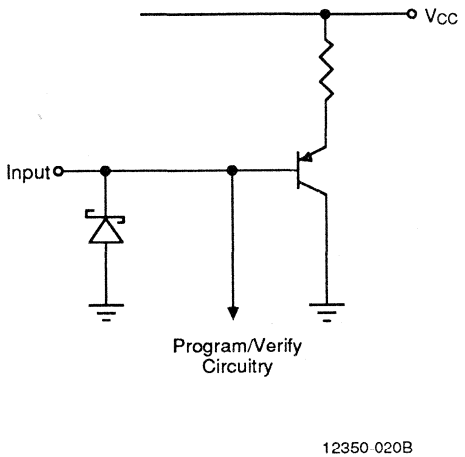


12350-019A

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

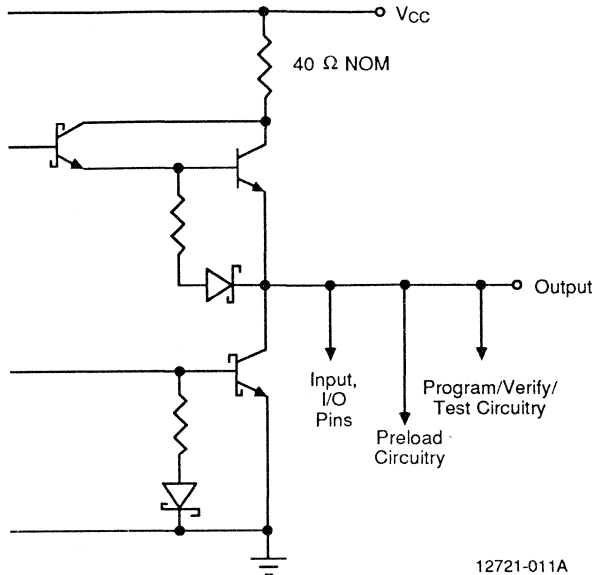
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



12350-020B

Typical Output



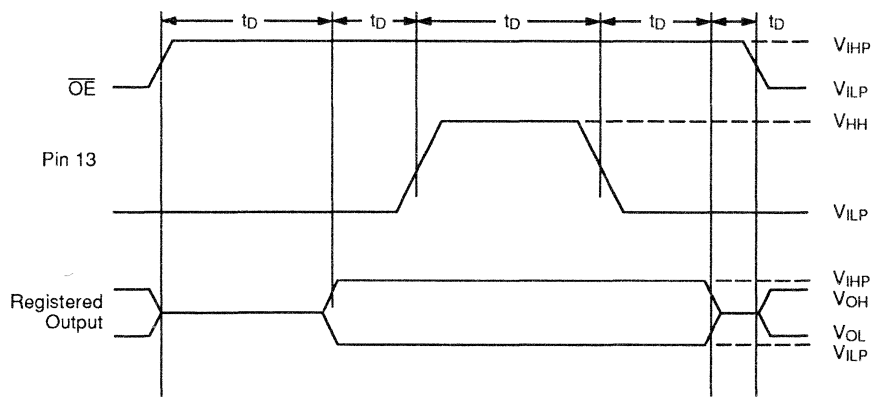
12721-011A

OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
4. Pulse pin 13 to V_{HH}, then back to V_{ILP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
7. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19.5	20	20.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload	4.5	5.0	5.5	V
t_D	Delay time	100	200	1000	ns



10294-004B

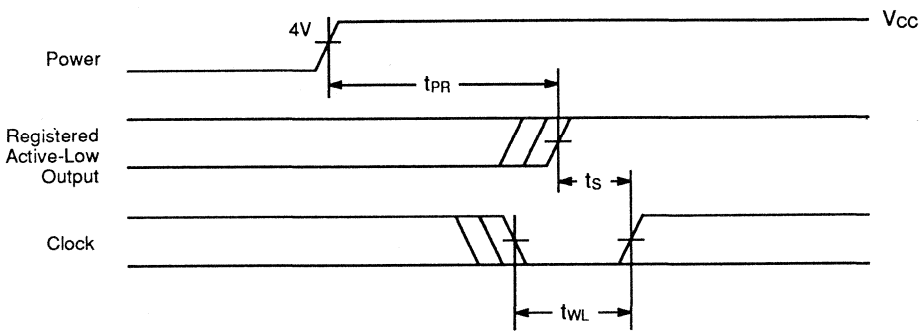
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

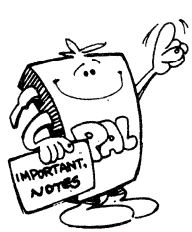
Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform

2



Preliminary COM'L

PALCE24V10H-15/25

EE CMOS 28-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High speed CMOS technology**
  - 15-ns propagation delay for "-15" version
  - 25-ns propagation delay for "-25" version
- **Outputs individually programmable as registered or combinatorial**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 28-pin plastic SKINNYDIP® and PLCC packages**
- **Programmable on standard PAL® device programmers**
- **Supported by PALASM® software**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

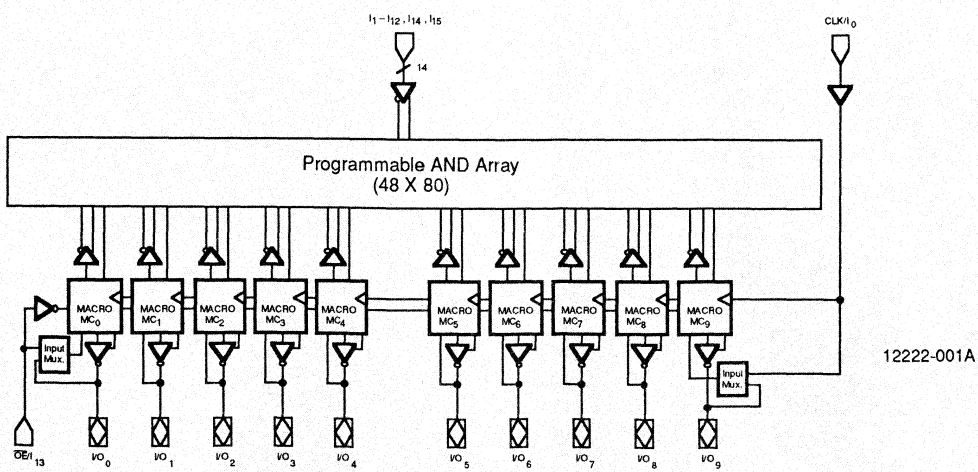
The PALCE24V10 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE24V10 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM

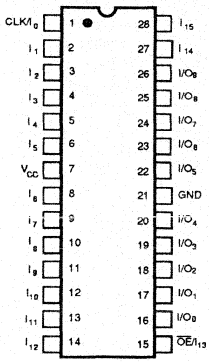


Publication # 12222 Rev B Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAMS

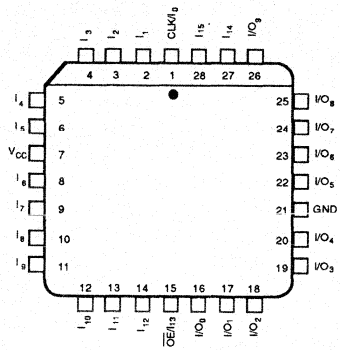
Top View

SKINNYDIP



12222-002A

PLCC



12222-003A

Pin Designations:

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
V_{CC} = Supply Voltage

Note: Pin 1 is marked for orientation.

2

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Flip-Flops
f. Power
g. Speed
h. Package Type
i. Operating Conditions

PAL CE 24 V 10 H -15 P C

a. FAMILY TYPE
PAL = Programmable Array Logic

b. TECHNOLOGY
CE = CMOS Electrically Erasable

c. NUMBER OF ARRAY INPUTS

d. OUTPUT TYPE
V = Versatile

e. NUMBER OF FLIP-FLOPS

f. POWER
H = Half Power (90 mA I_{CC})

g. SPEED
-15 = 15 ns t_{PD}
-25 = 25 ns t_{PD}

i. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

h. PACKAGE TYPE
P = 28-Pin 300-mil Plastic SKINNYDIP (PD3028)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

Valid Combinations	
PALCE24V10H-15	PC, JC
PALCE24V10H-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

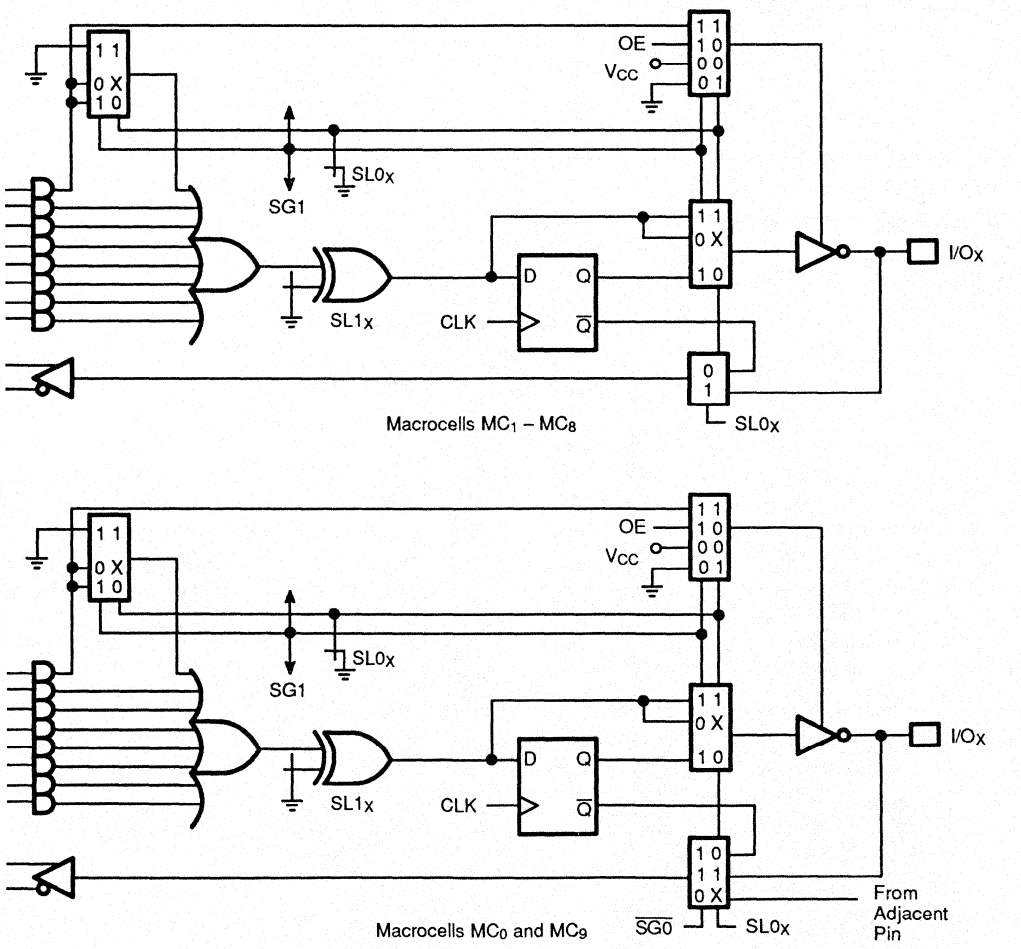
FUNCTIONAL DESCRIPTION

The PALCE24V10 is a universal PAL device. It has ten independently configurable macrocells (MC_0..MC_9). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 15 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE24V10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE24V10. First, it can be programmed as an emulated PAL device. This includes the PAL24R10 series. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE24V10. The programmer will program the PALCE24V10 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE24V10. Here the user must use the PALCE24V10 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



12222-004A

PALCE24V10 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 20 local bits ($SL0_0$ through $SL0_9$ and $SL1_0$ through $SL1_9$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE24V10 will emulate a PAL24R10 family or a simple combinatorial device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_9, $\overline{SG0}$ is added on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE24V10 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins are available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE24V10 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Because the macrocell is a dedicated output, the feedback is not used.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is the I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0, SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device has registers				
0	1	0	Registered Output	PAL24R10, 24R8, 24R4
0	1	1	Combinatorial I/O	PAL24R8, 24R4
Device has no registers				
1	0	0	Combinatorial Output	Simple Combinatorial
1	0	1	Dedicated Input	Simple Combinatorial
1	1	1	Combinatorial I/O	PAL24L10

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.

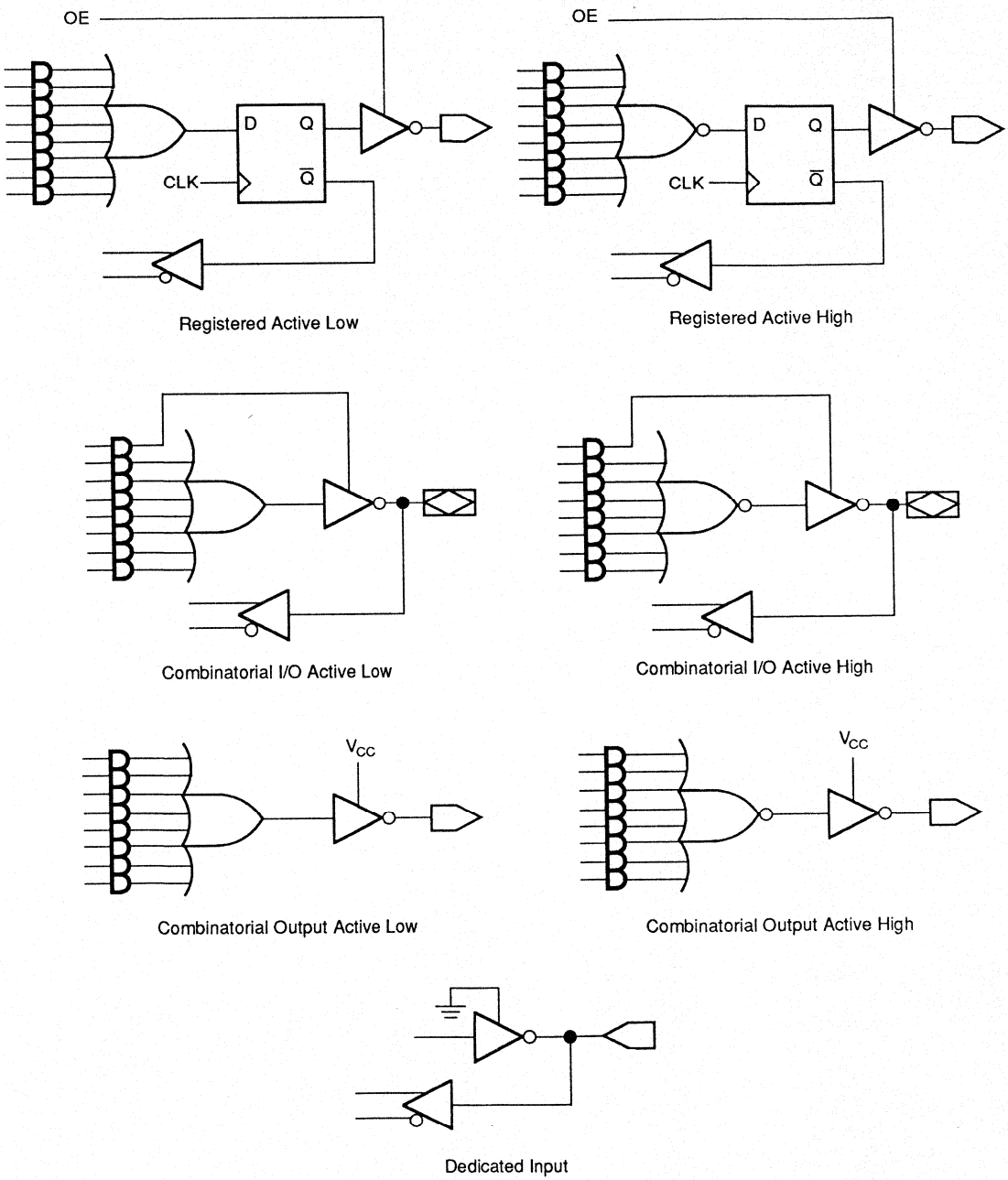


Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE24V10 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE24V10 Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE24V10 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

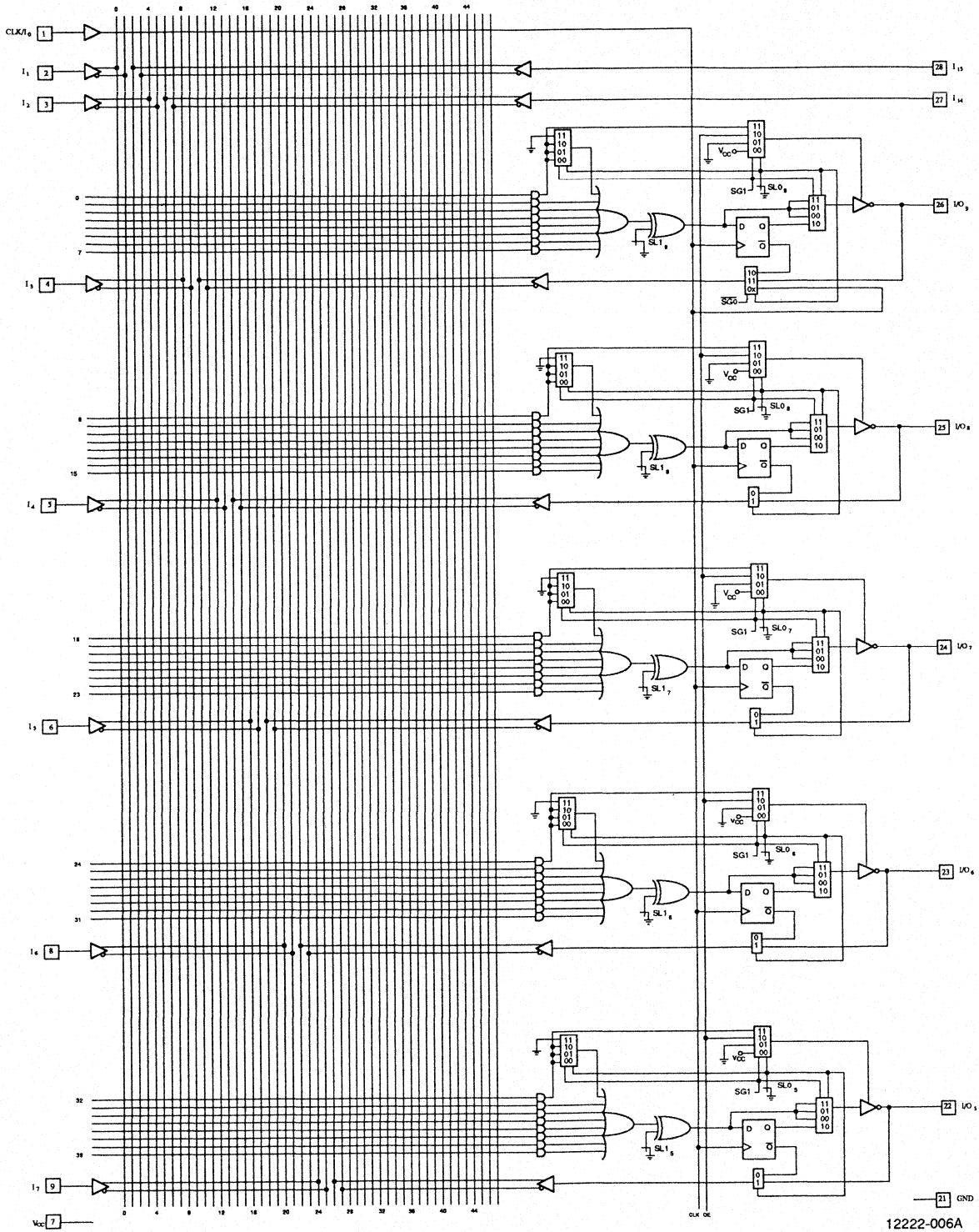
An electronic signature word is provided in the PALCE24V10. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

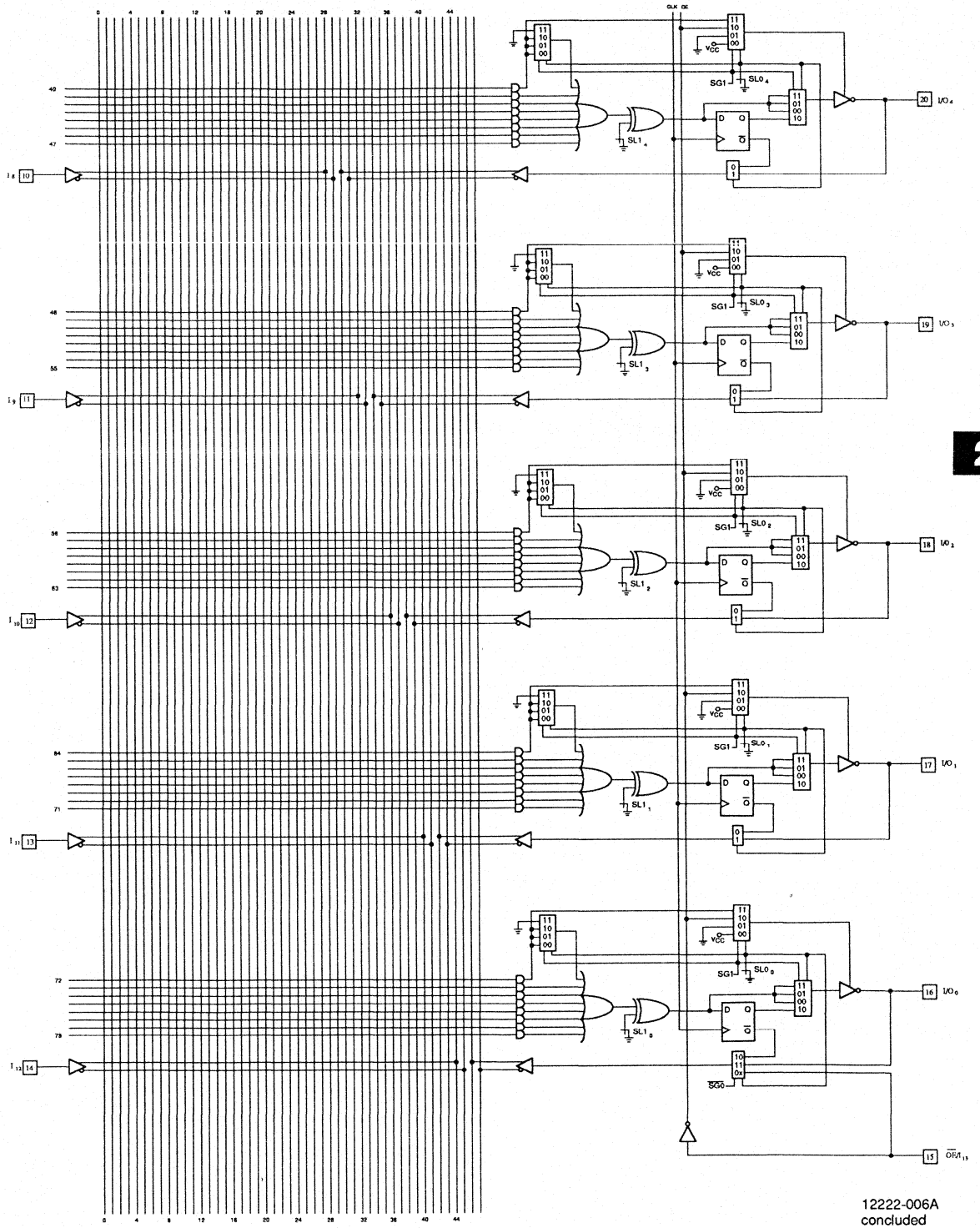
The PALCE24V10 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PALCE24V10 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

LOGIC DIAGRAM



LOGIC DIAGRAM (Continued)



12222-006A
concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max. V_{OUT} = 0.5 V (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

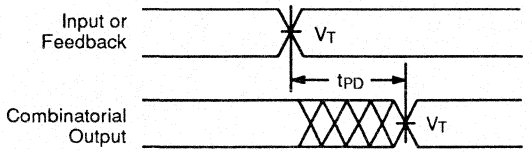
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{CF}	Clock to Feedback (Note 3)				8		10	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback	$1/(t_S+t_{CF})$	50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

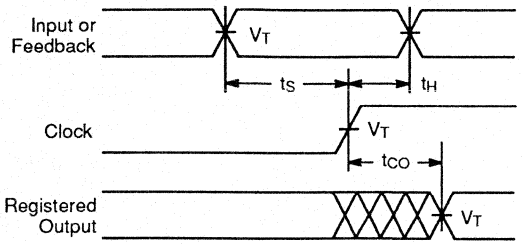
2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



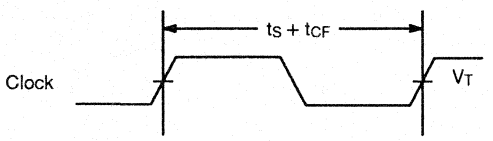
12015-010A

Combinatorial Output



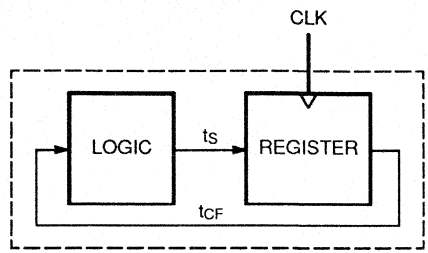
12015-012A

Registered Output

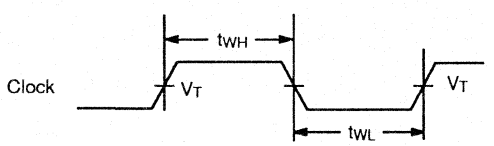


12149-025A

Clock to Feedback (f_{MAX} Internal)
See Path at Right

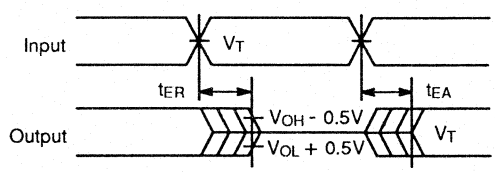


12015-021A



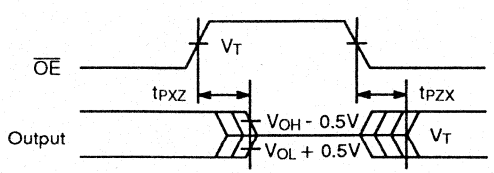
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

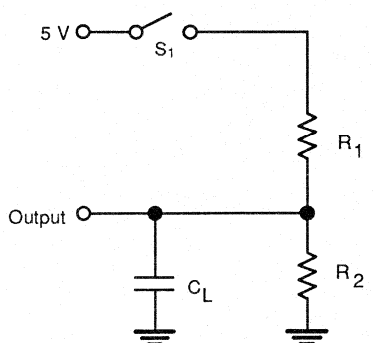
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12197-007A

Switching Test Circuit

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	200 Ω	390 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

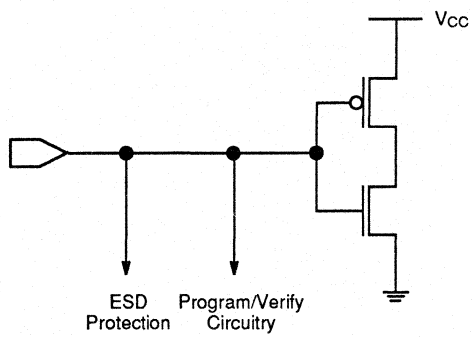
ENDURANCE CHARACTERISTICS

The PALCE24V10 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

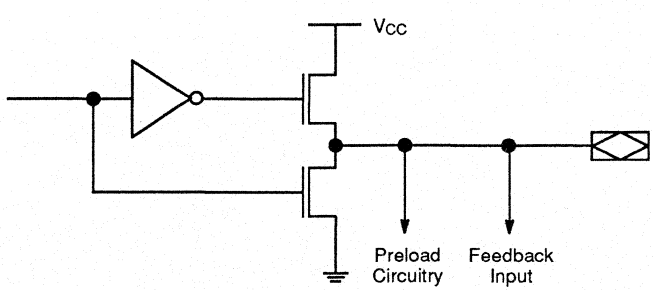
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

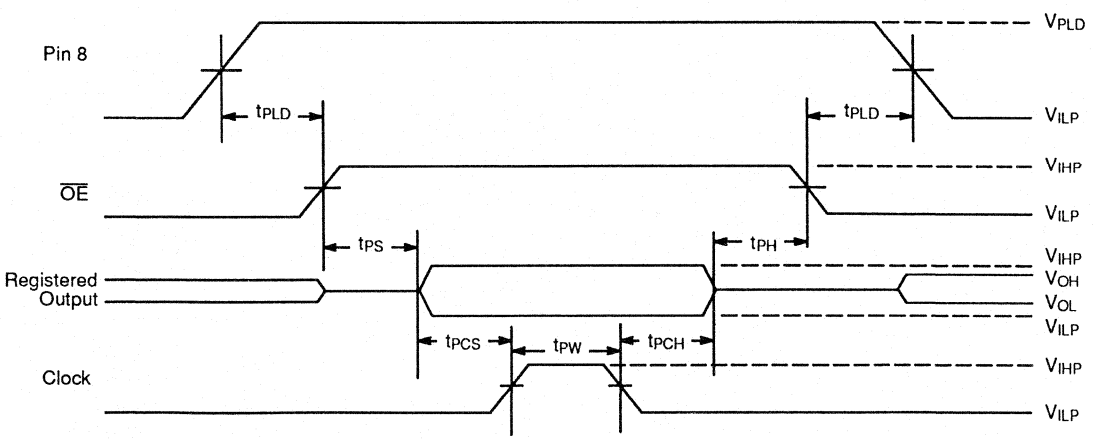
12197-013A

OUTPUT REGISTER PRELOAD

The Preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pin 8 to V_{PLD}.
3. Set $\overline{OE}$ HIGH.
4. Apply the desired value (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial output pins floating.
5. Clock pin 1 from V_{IL} to V_{IH}.
6. Remove V_{IL}/V_{IH} from all registered outputs.
7. Enable the output registers by lowering $\overline{OE}$.
8. Lower pin 8 to V_{IL}/V_{IH}.
9. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will be the inverse of the preload data.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_{PLD}	Setup and Hold Time from Preload (pin 8) to $\overline{OE}$	50	50		µs
t_{PS}	Setup Time from $\overline{OE}$ to Data	1	1		µs
t_{PH}	Hold Time from Data to $\overline{OE}$	1	1		µs
t_{PCS}	Setup Time from Data to Clock	1	1		µs
t_{PCH}	Hold Time from Clock to Data	1	1		µs
dV_r/dt	V_{PLD} Rising Slew Rate (pin 8)	10		100	V/µs
dV_f/dt	V_{PLD} Falling Slew Rate (pin 8)		2	3	V/µs
V_{PLD}	Super-Level Input Voltage	13.0	13.5	14.0	V
V_{IHP}	High-Level Input Voltage	2.4	5.0	5.5	V
V_{ILP}	Low-Level Input Voltage	0	0	0.5	V



12015-015A

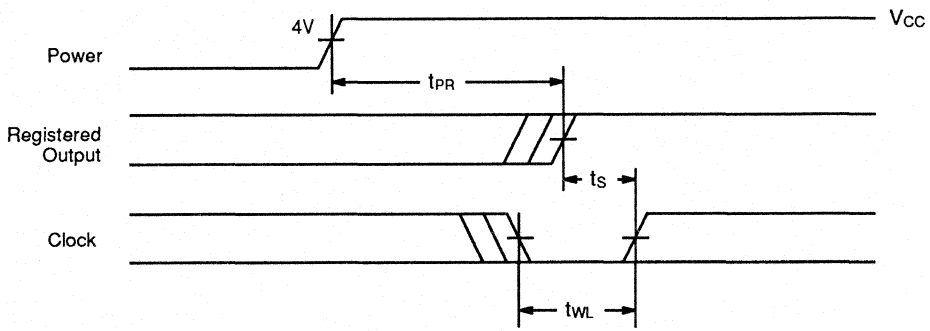
Output Register Preload Waveform

POWER-UP RESET

The PALCE24V10 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

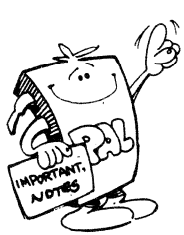
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12197-009A

Power-Up Reset Waveforms


IMPORTANT
NOTES

Final | COM'L

PALCE26V12H-20/25

28-Pin EE CMOS Versatile PAL® Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 28-pin versatile PAL programmable logic device architecture
- Electrically erasable CMOS technology provides half power (only 105 mA) at high speed (20 ns propagation delay)
- 14 dedicated inputs and 12 input/output macrocells for architectural flexibility
- Macrocells can be registered or combinatorial, and active high or active low
- Varied product term distribution allows up to 16 product terms per output
- Two clock inputs for independent functions
- Global asynchronous reset and synchronous preset for initialization
- Register preload for testability and built-in register reset on power-up
- Space-efficient 28-pin SKINNYDIP® and PLCC packages
- Center V_{CC} and GND pins to improve signal characteristics
- Supported by PALASM® software and other design tools and standard logic programmers

GENERAL DESCRIPTION

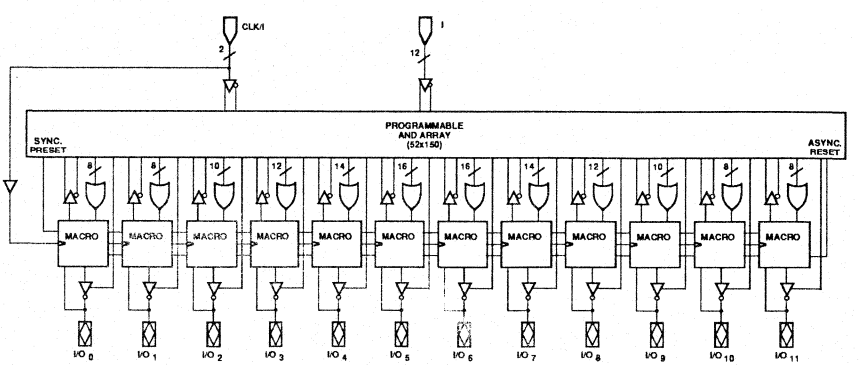
The PALCE26V12H is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12H offers many unique advantages.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software from AMD, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the programmed device. Third-party design tools and logic programmers also support the PALCE26V12H (see Programmer Reference Guide).

The PALCE26V12H utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active high or active low, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.

BLOCK DIAGRAM

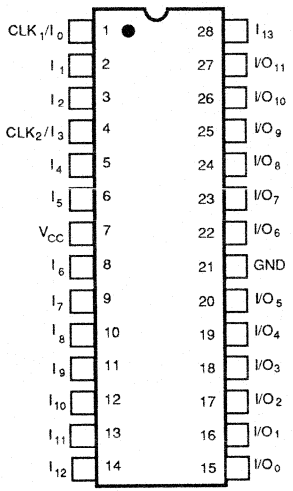


11757-001A

Publication # 11757 Rev. B Amendment /0
Issue Date: January 1990

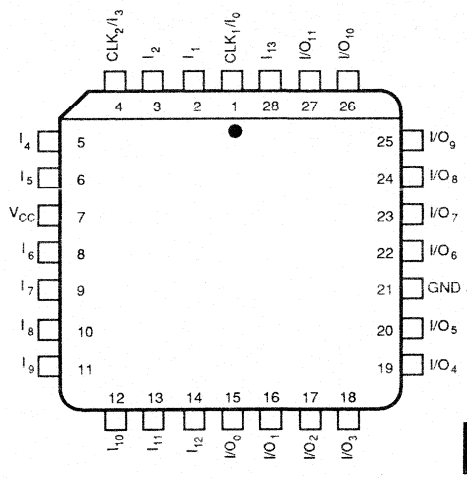
CONNECTION DIAGRAMS
Top View

SKINNYDIP



11757-005A

PLCC



11757-007A

2

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

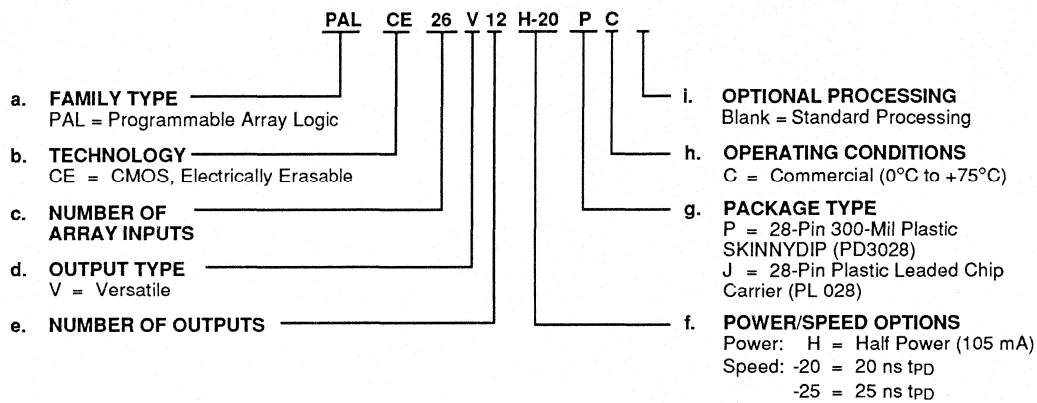
Note:

Pin 1 is marked for orientation.

ORDERING INFORMATION
Commercial Products

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Power/Speed Options
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations	
PALCE26V12H-20	PC, JC
PALCE26V12H-25	

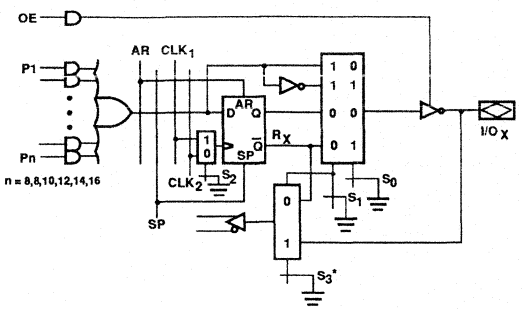
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The PALCE26V12H has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC}. Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.



* When S_3 = 1 (unprogrammed), the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757–004A

Figure 1. PALCE26V12H Macrocell

S_3	S_1	S_0	Output Configuration
1	0	0	Registered Output and Feedback, Active Low
1	0	1	Registered Output and Feedback, Active High
1	1	0	Combinatorial I/O, Active Low
1	1	1	Combinatorial I/O, Active High
0	0	0	Registered I/O, Active Low
0	0	1	Registered I/O, Active High
0	1	0	Combinatorial Output, Registered Feedback, Active Low
0	1	1	Combinatorial Output, Registered Feedback, Active High

S_2	Clock Input
1	CLK_1/I_0
0	CLK_2/I_3

1 = Unprogrammed EE bit
0 = Programmed EE bit

The OR gates feed the twelve I/O macrocells (see figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active high or active low, with register or I/O pin feedback (see figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0-S_3. Multiplexer controls initially float to V_{CC} (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.

Registered or Combinatorial

Each macrocell of the PALCE26V12H includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S_1.

Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S_2 determines the clock input.

Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed (t_{CF} specification applies), or I/O feedback for use of the pin as a direct input (t_{CO} specification applies). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S_1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S_3) that allows the alternative feedback path to be selected. When S_3 = 1, S_1 selects register feedback for registered outputs (S_1 = 0) and I/O feedback for combinatorial outputs (S_1 = 1). When S_3 = 0, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all in-

puts are left disconnected from the term (the unprogrammed state).

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high.

Preset/Reset

For initialization, the PALCE26V12 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH or the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12H will be HIGH or LOW depending on whether the output is active low or active high, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1 ms maximum.

Register Preload

The register on the PALCE26V12H can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading ilegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE26V12H design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload, and the array will read as if every bit is disconnected. The security bit can only be erased in conjunction with erasure of the entire pattern.

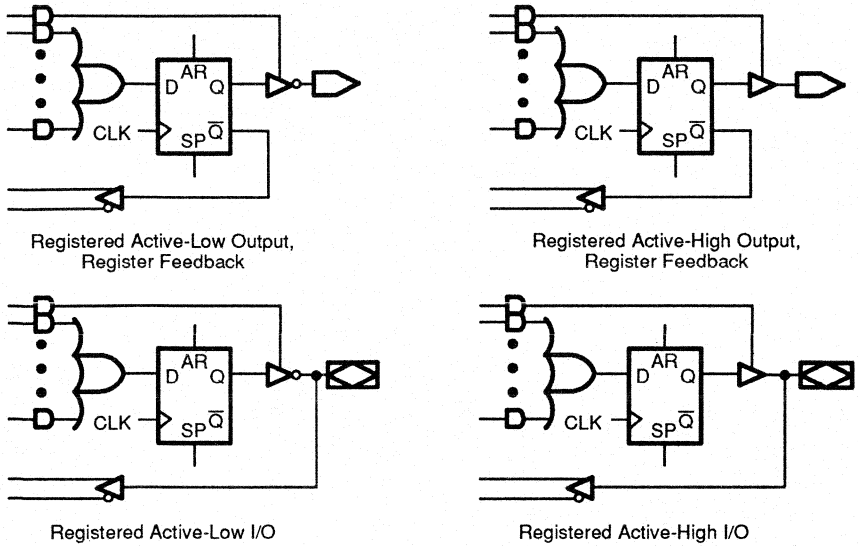
Quality and Testability

The PALCE26V12H offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Programming and Erasing

The PALCE26V12 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PALCE26V12 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.



Registered Active-Low Output, Register Feedback

Registered Active-High Output, Register Feedback

Registered Active-Low I/O

Registered Active-High I/O

Registered Outputs

Combinatorial Active-Low I/O

Combinatorial Active-High I/O

Combinatorial Active-Low Output, Register Feedback

Combinatorial Active-High Output, Register Feedback

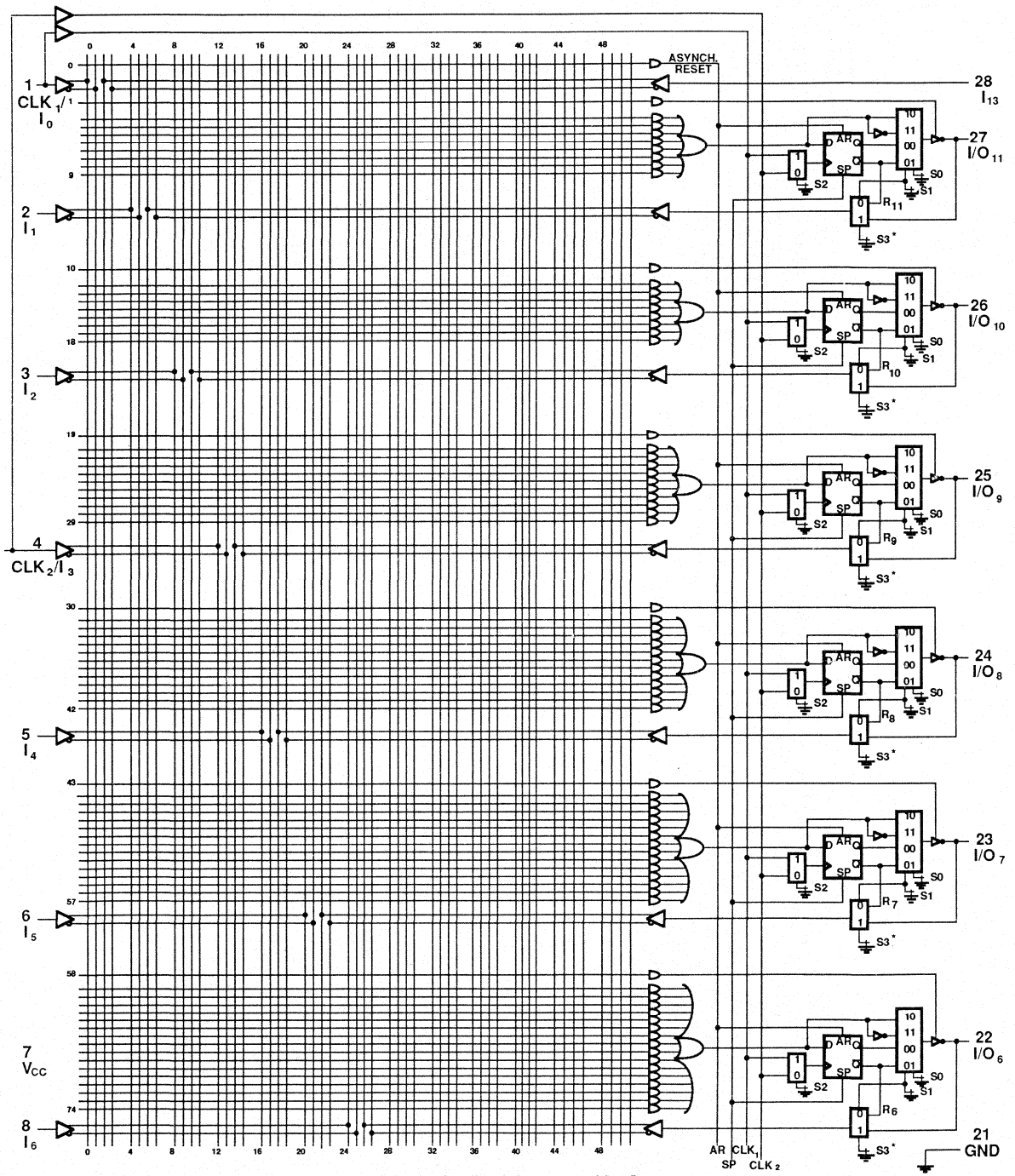
11757-003A

Combinatorial Outputs

Figure 2. PALCE26V12H Macrocell Configuration Options

LOGIC DIAGRAM

PALCE26V12H

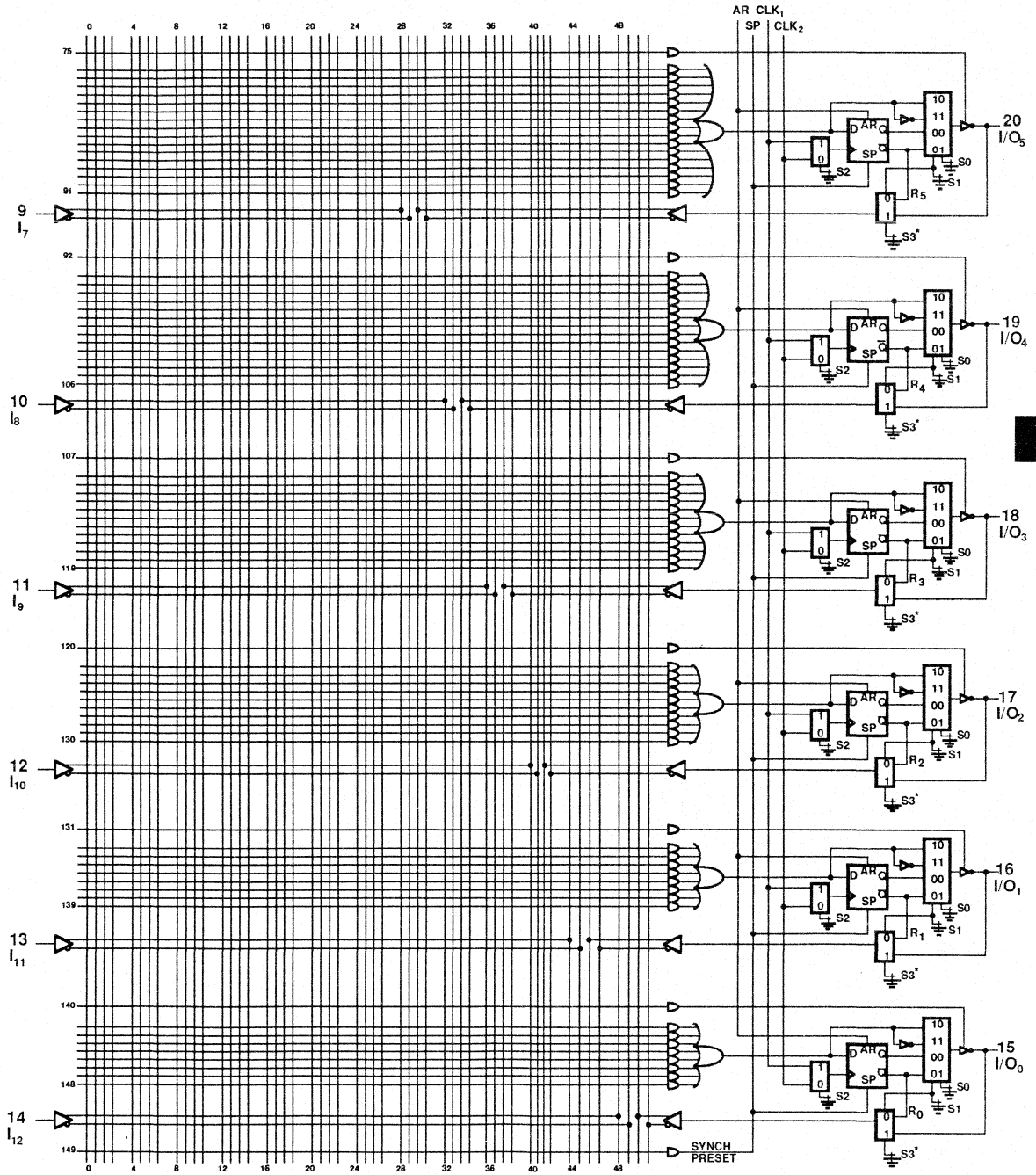


* When S_3 = 1 (unprogrammed), the feedback is selected by S_1.
When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757-006A

LOGIC DIAGRAM (Continued)

PALCE26V12H



* When S_3 = 1 (unprogrammed), the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757-006A
(Concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.6 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

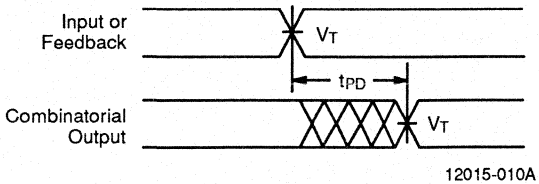
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			13		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				12		15	ns
t_{CF}	Clock to Feedback (Note 3)				10		13	ns
t_{AR}	Asynchronous Reset to Registered Output				25		30	ns
t_{ARW}	Asynchronous Reset Width			20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			20		25		ns
t_{SPR}	Synchronous Preset Recovery Time			13		15		ns
t_{WL}	Clock Width	LOW		10		13		ns
t_{WH}		HIGH		10		13		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	40		33.3		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	43		35		MHz
t_{EA}	Input to Output Enable Using Product Term Control				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				20		25	ns

Notes:

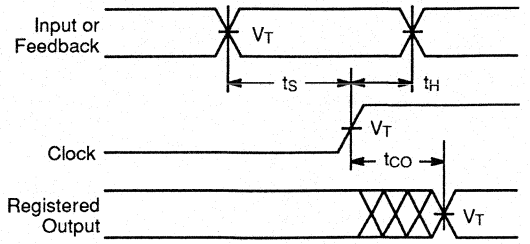
2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



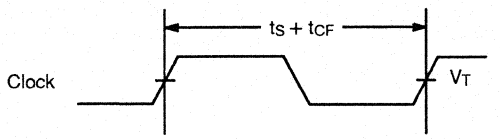
12015-010A

Combinatorial Output



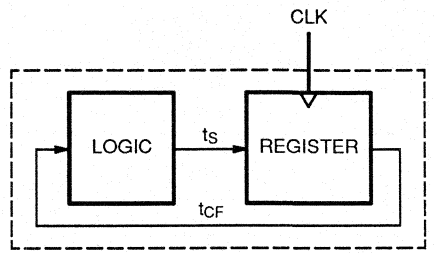
12015-012A

Registered Output

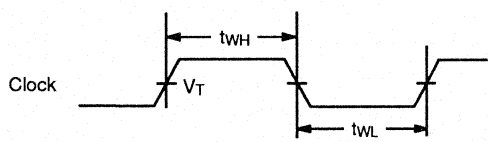


12149-025A

Clock to Feedback (f_{MAX} Internal)
See Path at Right

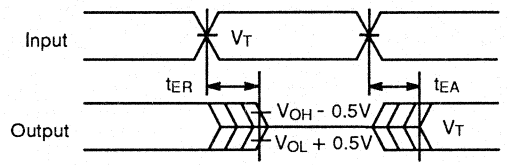


12015-021A



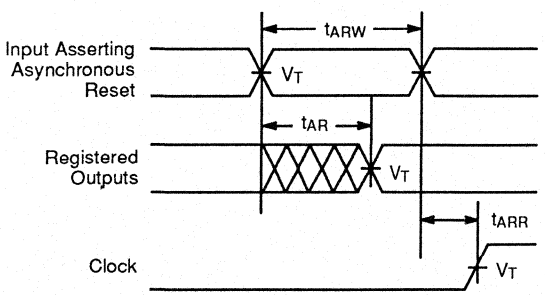
12015-011A

Clock Width



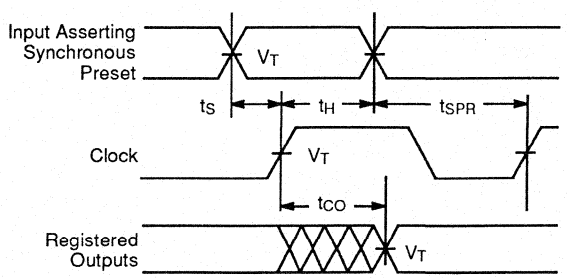
12015-013A

Input to Output Disable/Enable



11757-009A

Asynchronous Reset



11757-010A

Synchronous Preset

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

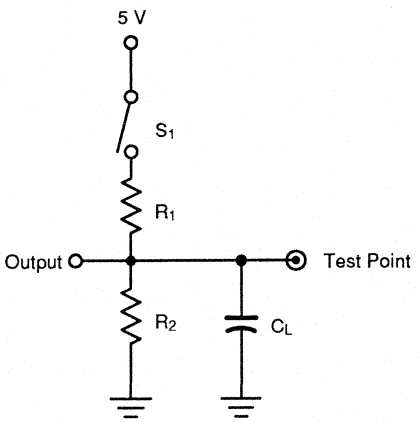
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT



12350-019A

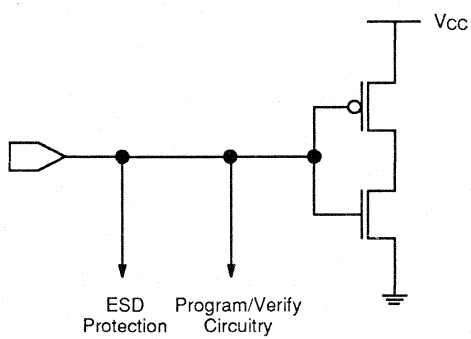
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

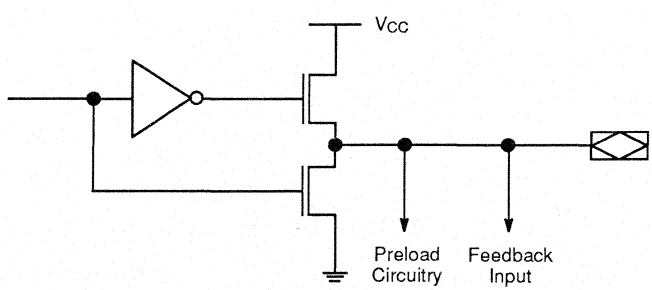
The PALCE26V12 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

Symbol	Parameter	Min.	Unit	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

12197-013A

OUTPUT REGISTER PRELOAD

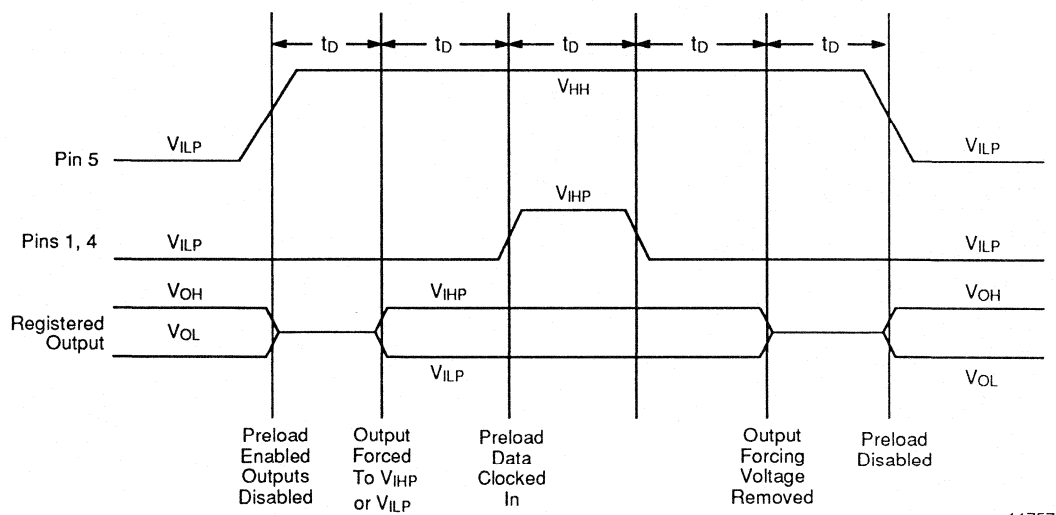
The PALCE26V12H registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature will simplify testing since any state can loaded into the registers to control test sequencing.

The pin levels and timing necessary to perform the Preload function are detailed below.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pin 5 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock appropriate pins, 1 and/or 4, from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered outputs.
6. Lower pin 5 to V_{IL}/V_{IH}.
7. Enable outputs according to programmed pattern. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the programmed polarity.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level Input Voltage	10.25	10.5	10.75	V
V_{ILP}	Low-level Input Voltage	0	0	0.5	V
V_{IHP}	High-level Input Voltage	2.4	5.0	5.5	V
t_D	Delay Time	10	100		µs

Level forced on registered output pin during Preload cycle	Register Q output state after cycle
V_{IHP}	HIGH
V_{ILP}	LOW



11757-008A

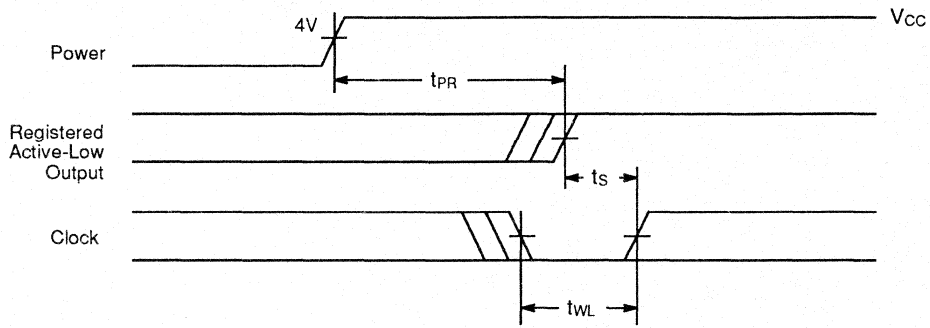
Preload Waveforms

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

2

Final COM'L

PALCE29M16H-25/35

24-Pin EE CMOS Programmable Array Logic

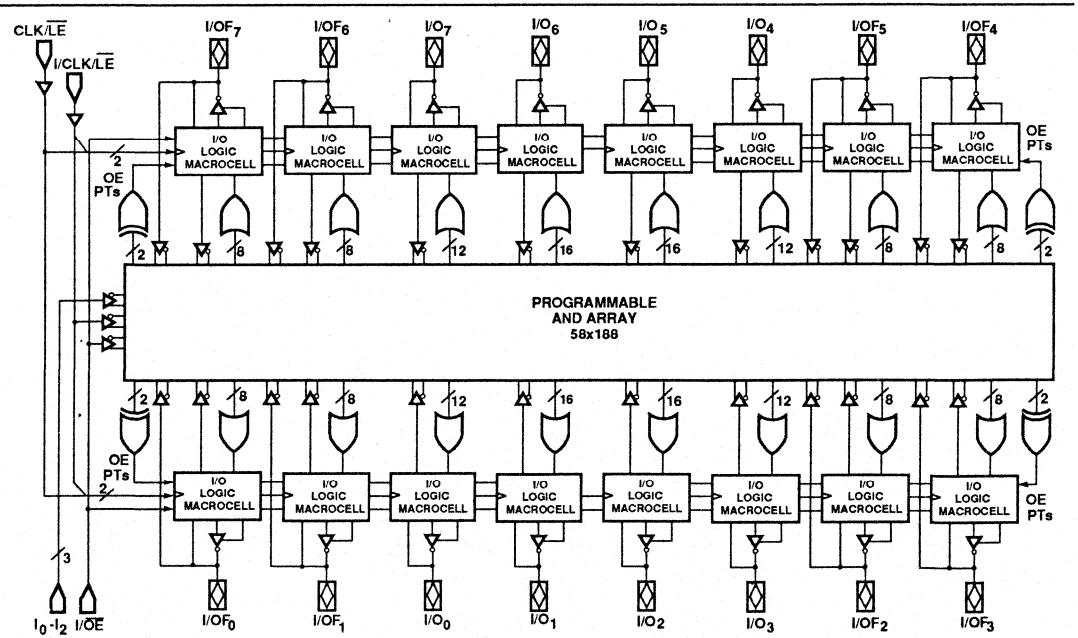
Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High-performance semicustom logic replacement; Electrically Erasable (E^2) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/ Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with two clocks/ latch enables ($\overline{LE}$s) and LOW/HIGH clock/$\overline{LE}$ polarity
- Register/Latch Preload permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-pin 300-mil SKINNYDIP® and 28-pin plastic leaded chip carrier packages

GENERAL DESCRIPTION

The PALCE29M16H is a high-speed, E^2-based CMOS Programmable Array Logic device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming and excellent reliability. Programmable Array Logic (PAL®) devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.



08740-001A

Figure 1. Block Diagram

Publication # 08740 Rev. D Amendment /0
Issue Date: January 1990

GENERAL DESCRIPTION (Continued)

The PALCE29M16H uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to twenty-nine array inputs and sixteen outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as "Combinatorial," "Registered," or "Latched" with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29M16H by providing a varied number of logic product terms per output. Eight outputs have eight product terms each, four outputs have twelve product terms each, and the other four outputs have sixteen product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product terms per bank of four outputs. Each output can also be permanently enabled or disabled.

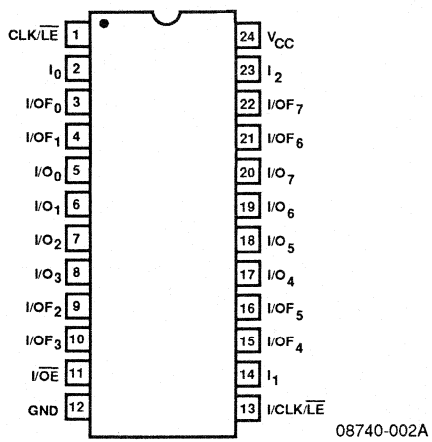
System operation has been enhanced by the addition of common asynchronous-PRESET and RESET product terms and a power-up RESET feature. The PALCE29M16H also incorporates PRELOAD and Observability functions which permit full logic verification of the design.

The PALCE29M16H is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS

(Top View)

SKINNYDIP



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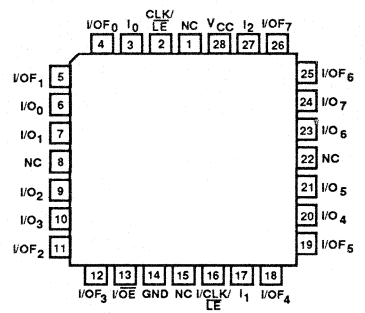
Note:
Pin 1 is marked for orientation

PLCC



08740-003A

Pin Designations:

I	= Input
I/O	= Input/Output
I/OF	= Input/Output with Dual Feedback
V_{CC}	= Supply Voltage
GND	= Ground
CLK/$\overline{LE}$	= Clock/Latch Enable
NC	= No Connection

PIN DESCRIPTION

The following describes the functionality of all the pins on the 24-pin SKINNYDIP. The 28-pin chip carrier has the same functionality with NO CONNECTS on pins 1, 8, 15, 22.

CLK/$\overline{LE}$ (PIN 1): Used as a dedicated clock/latch enable pin for all registers/latches on the device if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/CLK/$\overline{LE}$ PIN (PIN 13): Used as dedicated input or as an alternate clock/latch enable pin for all the registers/latches if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/$\overline{OE}$ PIN (PIN 11): Used as a dedicated input pin to the AND array or as the Output Enable control pin (Active LOW) for all macrocells with pin-controlled Output Enable selected.

I_0-I_2 (PINS 2, 14, 23): Dedicated input pins.

I/OF_0-I/OF_7 (PINS 3, 4, 9, 10, 15, 16, 21, 22): Eight bidirectional I/O pins with two independent feedback paths to the AND array. The first feedback path is a dedicated I/O pin feedback to the AND array for combinatorial input. The second feedback path consists of direct register/latch feedback to the array (see Figure 2b).

I/O_0-I/O_7 (PINS 5, 6, 7, 8, 17, 18, 19, 20): Eight bidirectional I/O pins with user-programmable register/latch or I/O pin feedback to the AND array (see Figure 2a).

V_{CC} (PIN 24): Supply Voltage.

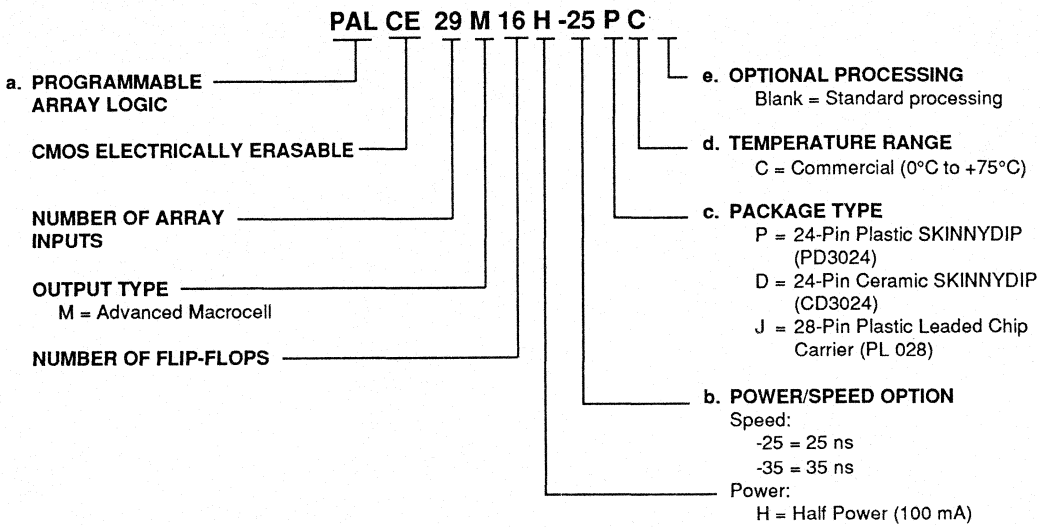
GND (PIN 12): Circuit Ground.

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power/Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
PALCE29M16H-25 PALCE29M16H-35	PC, DC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:

Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Inputs

The PALCE29M16H has twenty-nine inputs to drive each product term (up to fifty-eight inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these twenty-nine inputs, three are dedicated inputs, sixteen are from eight I/O logic macrocells with two feedbacks, eight are from other I/O logic macrocells with single feedback, one is the I/$\overline{OE}$ input and one the I/CLK/$\overline{LE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the E^2 cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29M16H has 188 product terms; 176 of these product terms provide logic capability and twelve are architectural or control product terms. Among the twelve control product terms, two are for common Asynchronous-PRESET and RESET, one is for Observability, and one is for PRELOAD. The other eight are common Output Enable product terms. The Output Enable of each bank of four macrocells can be programmed to be controlled by a common Output Enable pin or two AND/XOR product terms. It may be also permanently enabled or permanently disabled.

Each product term on the PALCE29M16H consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from eight to sixteen wide, with an average of eleven logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

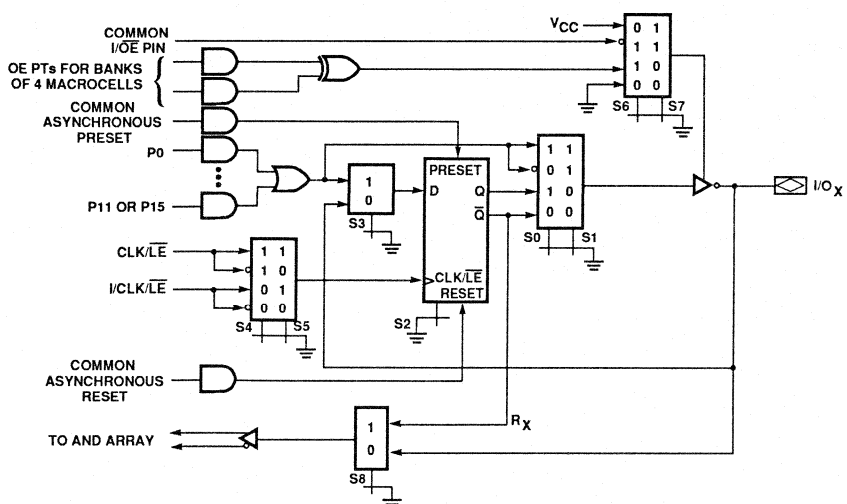
Common asynchronous-PRESET and RESET product terms are connected to all Registered/Latched inputs/outputs.

When the asynchronous-PRESET product term is asserted (HIGH) all the registers/latches will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-RESET product term is asserted (HIGH) all the registers/latches will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the RESET/PRESET, PRELOAD, and power-up RESET modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29M16H has sixteen macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers are used in synchronous logic applications while latches are used in asynchronous applications.



08740-004A

Figure 2a. PALCE29M16H Macrocell (Single Feedback)

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0-I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29M16H has one dedicated CLK/$\overline{LE}$ pin and an I/CLK/$\overline{LE}$ pin. All macrocells have a programmable select to choose between these two pins as the clock or the latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by two AND-XOR product terms which are available for each bank of four I/O Logic Macrocells.

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain nine E^2 cells, while the other eight macrocells contain eight E^2 cells for programming the input/output functions (see Table 1).

E^2 cell S1 controls whether the macrocell will be combinatorial or registered/latched. S0 controls the output polarity (active-HIGH or active-LOW). S2 determines whether the input/output is a register or a latch. S3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable E^2 cells S4 and S5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S6 and S7 are used to control Output Enable as pin controlled, two product term controlled, permanently enabled or permanently disabled. S8 controls a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable E^2 cells S0-S8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the virgin erased state (charged, disconnected), an architectural cell is said to have a value of "1"; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0."

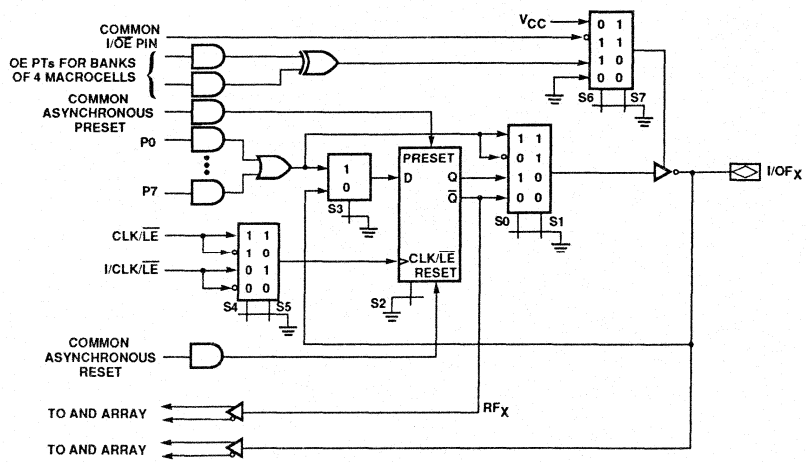


Figure 2b. PALCE29M16H Macrocell (Dual Feedback)

S3	I/O Cell
1	Output Cell
0	Input Cell

S2	Storage Element
1	Register
0	Latch

S1	Output Type
1	Combinatorial
0	Register/Latch

S0	Output Polarity
1	Active LOW
0	Active HIGH

S8	Feedback*
1	Register/Latch
0	I/O

* Applies to macrocells with single feedback only.

Table 1a. PALCE29M16H I/O Logic Macrocell Architecture Selections

S4	S5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE
0	1	I/CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
0	0	I/CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE

S6	S7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	XOR PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

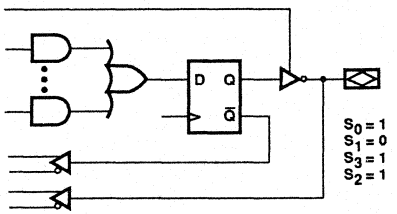
1 = Erased State (Charged or disconnected).
0 = Programmed State (Discharged or connected).

Table 1b. PALCE29M16H I/O Logic Macrocell Clock Polarity and Output Enable Selections

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

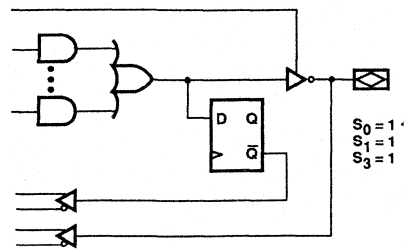
(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).

Output Registered/Active Low



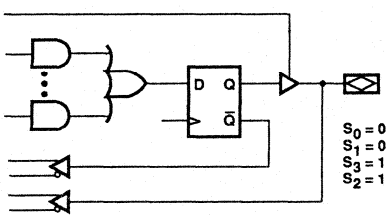
08811-006A

Output Combinatorial/Active Low



08811-007A

Output Registered/Active High



08811-008A

Output Combinatorial/Active High

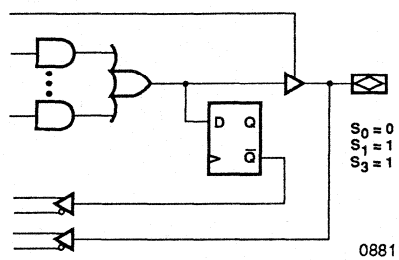


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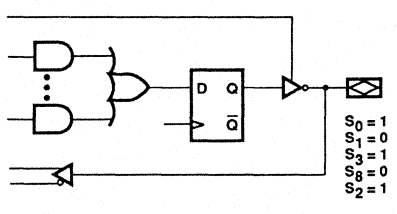
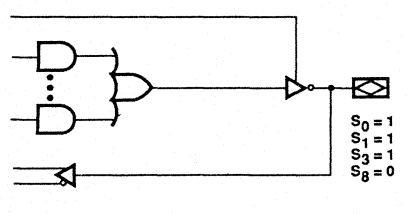
Figure 3a. Dual Feedback Macrocells

Output Registered/Active Low, I/O Feedback



08811-010A

Output Combinatorial/Active Low, I/O Feedback



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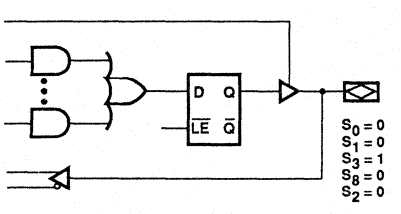
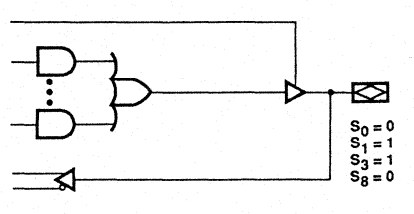
Output Latched/Active High, I/O Feedback



08811-012A

Output Combinatorial/Active High, I/O Feedback

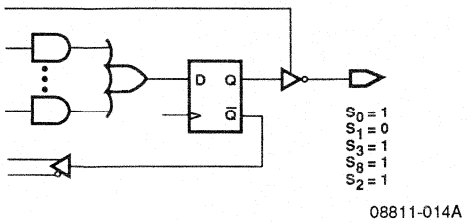


08811-013A

Figure 3b. Single Feedback Macrocells

POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL (Continued)

Output Registered/Active Low, Register Feedback



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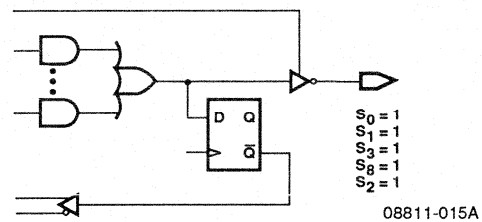
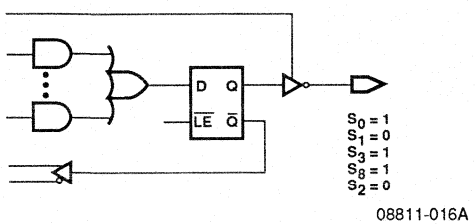
Output Combinatorial/Active Low, Register Feedback



08811-015A

Output Latched/Active Low, Latched Feedback



08811-016A

Output Combinatorial/Active Low, Latched Feedback

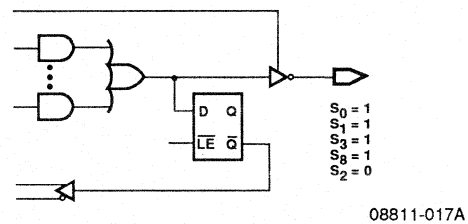


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Figure 3b. Single Feedback Macrocells (Continued)

Input Registered/Latched

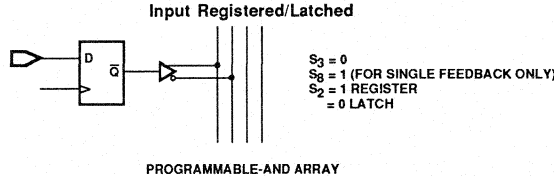

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Figure 3c. All Macrocells

DESIGNED-IN TESTABILITY AND DEBUGGING

Preload

To simplify testing, the PALCE29M16H is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. Both product term controlled and supervoltage-enabled PRELOAD modes are available. This offers even more test capability than previously implemented in AMD's PAL devices. The TTL-level PRELOAD product term can be useful during debugging, where supervoltages may not be available.

PRELOAD allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into an arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way any transition can be checked.

Since PRELOAD can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

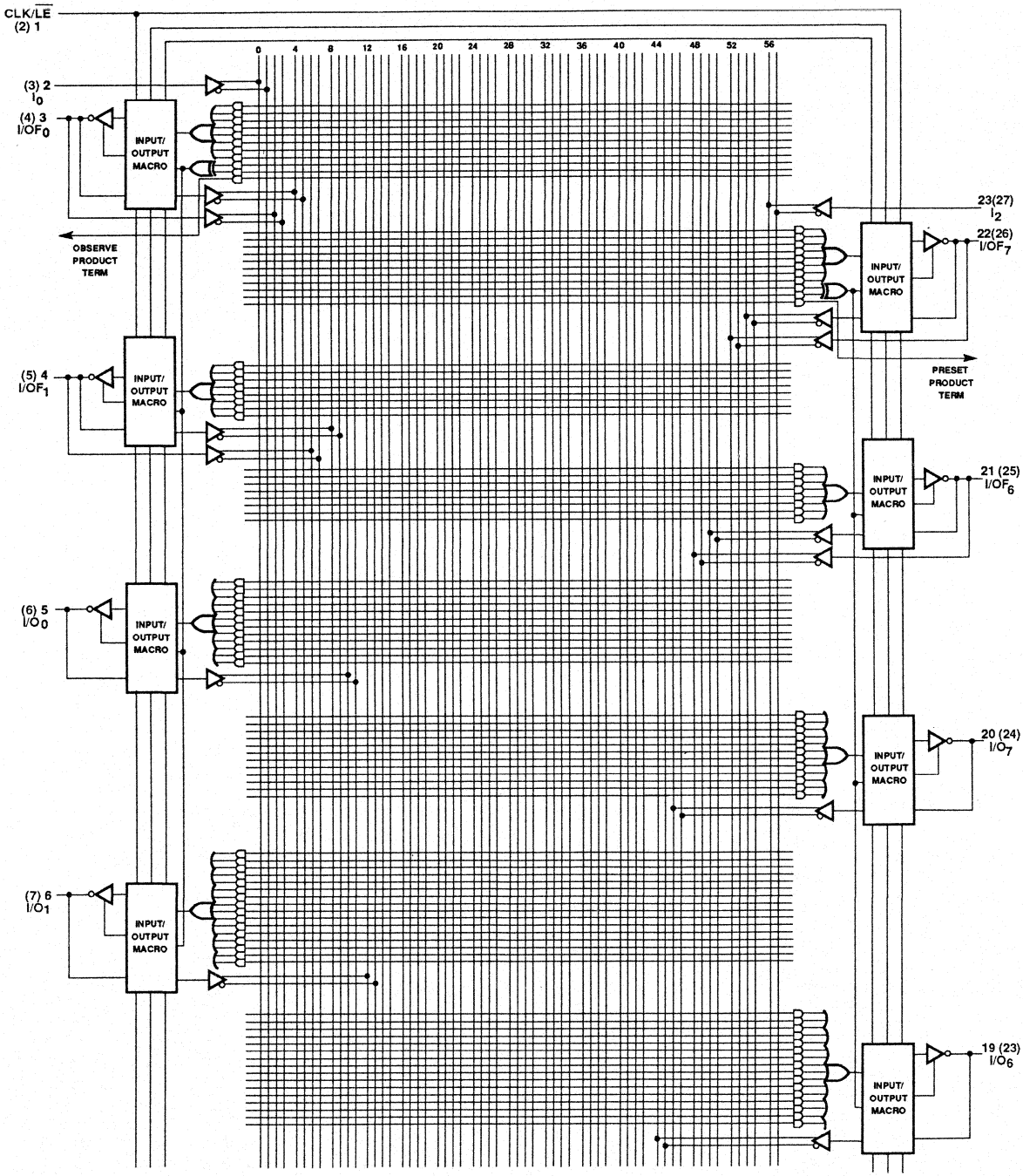
The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, PRELOAD, and the observability modes. The only way to erase the protection cell is by charging the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

LOGIC DIAGRAM

DIP (PLCC) Pinouts



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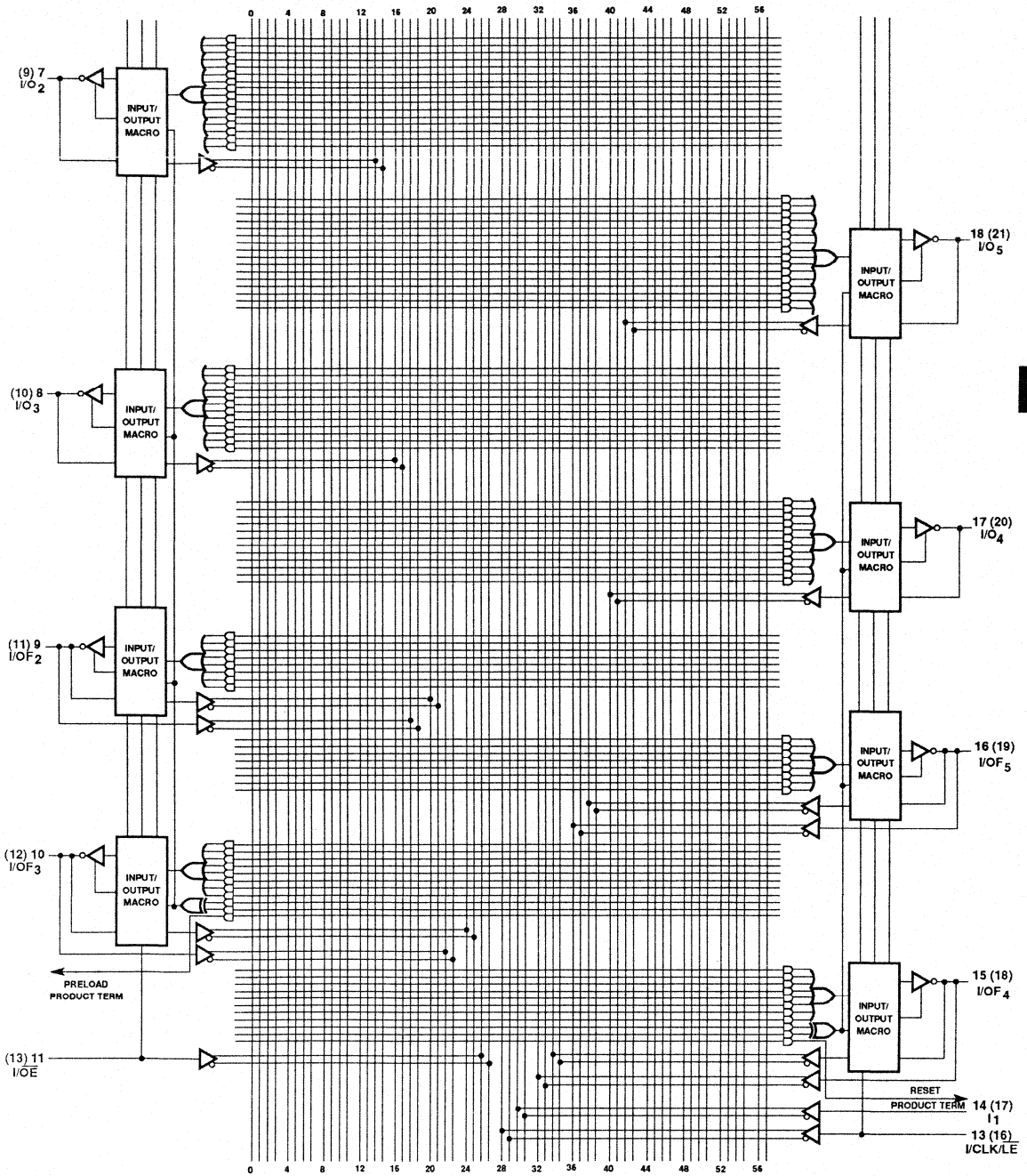
LOGIC DIAGRAM (Continued)

DIP (PLCC) Pinouts

Continued From Previous Page



08740-028A
Concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage (Except Pin I/$\overline{OE}$)	–0.5 V to V_{CC} + 0.5 V
DC Input Voltage (Pin I/$\overline{OE}$)	–0.6 V to +16 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
DC Input Current	–1 mA to +1 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 6 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
		I_{OL} = 4 mA			0.33	
		I_{OL} = 20 µA			0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			100	mA

Notes:

1. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	

Note:

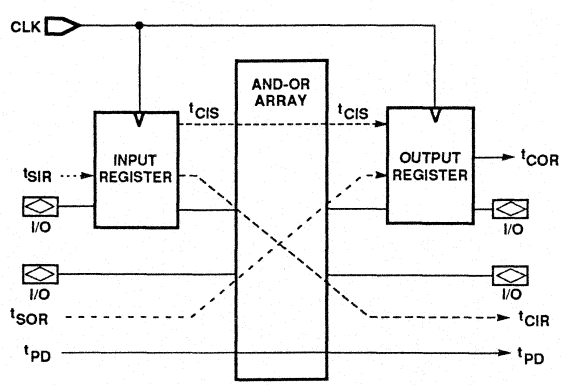
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS

Over commercial range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 35 pF.

Registered Operation

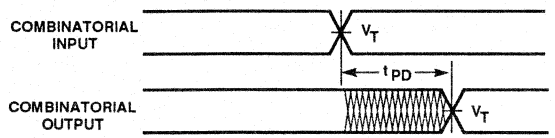
Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Output						
t_{PD}	Input or I/O Pin to Combinatorial Output		25		35	ns
Output Register						
t_{SOR}	Input or I/O Pin to Output Register Setup	15		20		ns
t_{COR}	Output Register Clock to Output		15		20	ns
t_{HOR}	Data Hold Time for Output Register	0		0		ns
Input Register						
t_{SIR}	I/O Pin to Input Register Setup	2		4		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28		36	ns
t_{HIR}	Data Hold Time for Input Register	6		8		ns
Clock and Frequency						
t_{CIS}	Register Feedback to Output Register/Latch Setup	20		30		ns
f_{MAX}	Maximum Frequency $1/(t_{SOR} + t_{COR})$	33.3		25		MHz
f_{MAXI}	Maximum Internal Frequency $1/t_{CIS}$	50		33.3		MHz
t_{CWH}	Pin Clock Width HIGH	8		12		ns
t_{CWL}	Pin Clock Width LOW	8		12		ns



08811-020A

Input/Output Register Specs

SWITCHING WAVEFORMS



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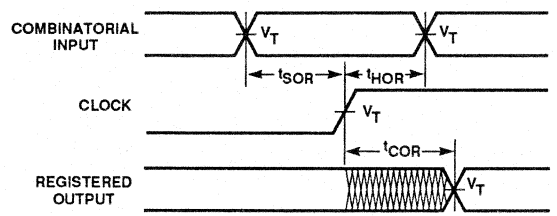
Combinatorial Output



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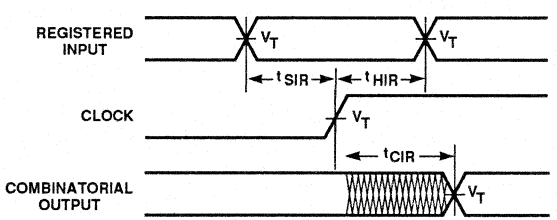
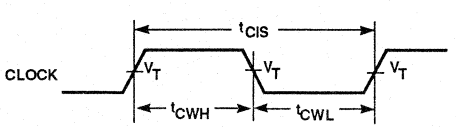
Output Register



08811-024A

Input Register



08740-026A

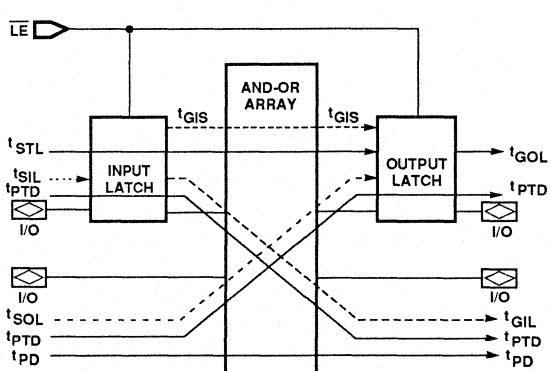
Clock Width

SWITCHING CHARACTERISTICS (Continued)

Over commercial range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 35 pF.

Latched Operation

Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Output						
t_{PD}	Input or I/O Pin to Combinatorial Output		25		35	ns
t_{PTD}	Input or I/O Pin to Output via One Transparent Latch		28		36	ns
Output Latch						
t_{SOL}	Input or I/O Pin to Output Latch Setup	15		20		ns
t_{GOL}	Latch Enable to Transparent Mode Output		15		20	ns
t_{HOL}	Data Hold Time for Output Latch	0		0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		25		ns
Input Latch						
t_{SIL}	I/O Pin to Input Latch Setup	2		4		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28		36	ns
t_{HIL}	Data Hold Time for Input Latch	6		8		ns
Latch Enable						
t_{GIS}	Latch Feedback to Output Register/Latch Setup	20		30		ns
t_{GWH}	Pin Enable Width HIGH	8		12		ns
t_{GWL}	Pin Enable Width LOW	8		12		ns



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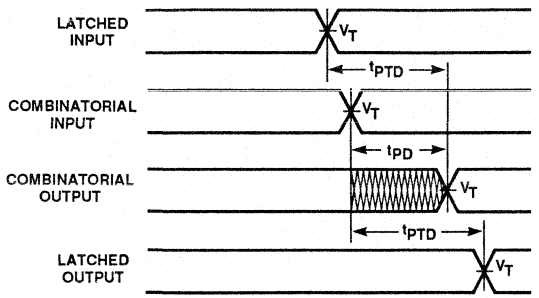
Input/Output Latch Specs



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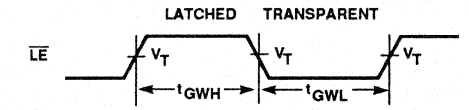
Latch (Transparent Mode)



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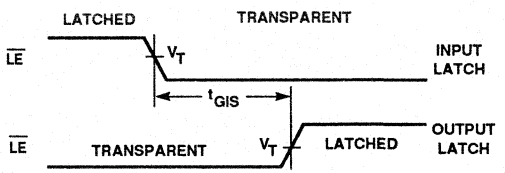
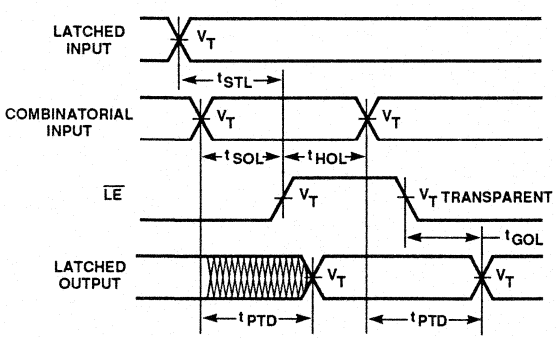
$\overline{LE}$ Width



08811-031A

Input and Output Latch Relationship



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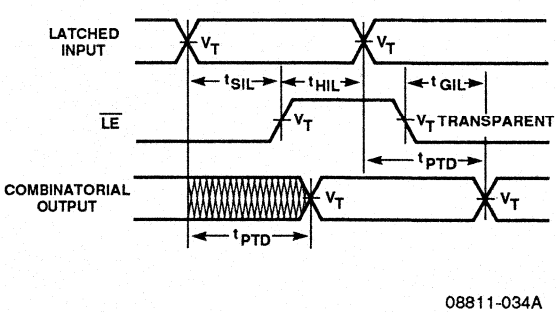
Output Latch



08811-034A

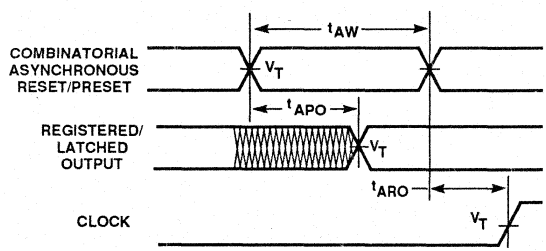
Input Latch

Reset/Preset, Enable

Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
t_{APO}	Input or I/O Pin to Output Register/Latch RESET/PRESET		30		40	ns
t_{AW}	Asynchronous RESET/PRESET Pulse Width	15		20		ns
t_{ARO}	Asynchronous RESET/PRESET to Output Register/Latch Recovery	15		20		ns
t_{ARI}	Asynchronous RESET/PRESET to Input Register/Latch Recovery	12		15		ns
Output Enable Operation						
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20		30	ns
t_{PXZ}*	I/$\overline{OE}$ Pin to Output Disable		20		30	ns
t_{EA}	Input or I/O to Output Enable via PT		25		35	ns
t_{ER}*	Input or I/O to Output Disable via PT		25		35	ns

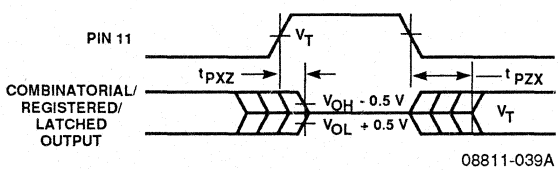
* Output disable times do not include test load RC time constants.

SWITCHING WAVEFORMS (Continued)



08811-037A

Output Register/Latch Reset/Preset



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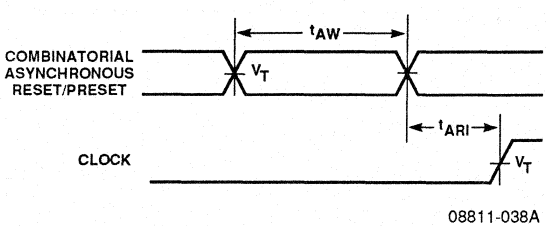
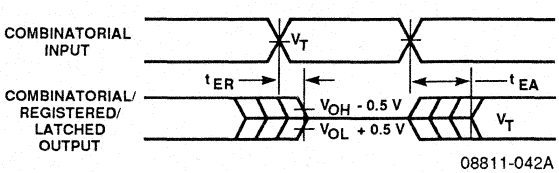
Pin 11 to Output Disable/Enable



08811-038A

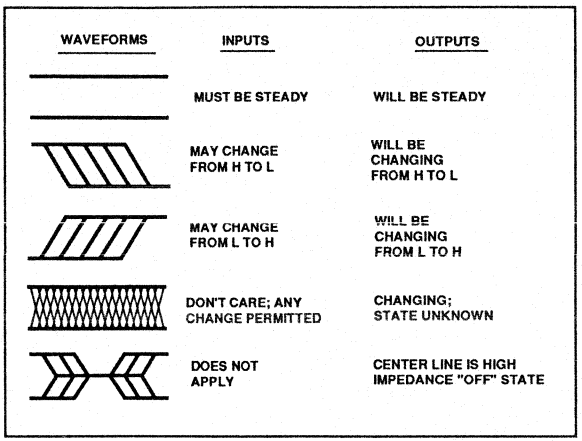
Input Register/Latch Reset/Preset



08811-042A

Input to Output Disable/Enable

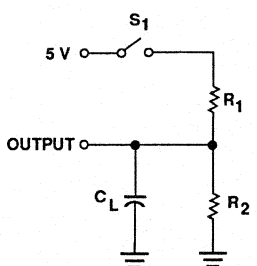
KEY TO SWITCHING WAVEFORMS



KS000010-PAL

2

SWITCHING TEST CIRCUIT



08811-044A

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GO}	Closed	35 pF	620 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed	35 pF	620 Ω	390 Ω	1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF	620 Ω	390 Ω	H→Z: V_{OH} -0.5 V L→Z: V_{OL} +0.5 V

PRELOAD AND OBSERVABILITY

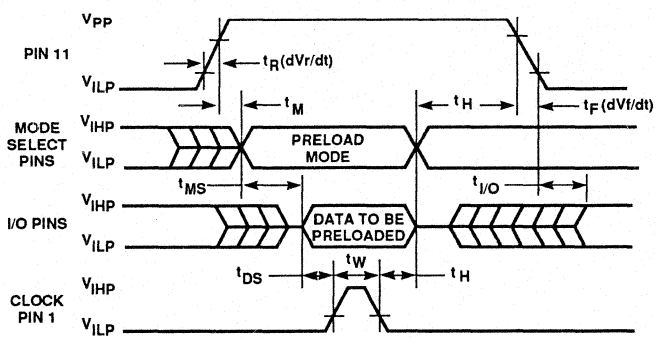
The PALCE29M16H has special preload and observability modes designed in. The PRELOAD mode is very useful during structured vector testing after programming, while the observe mode allows the designer to see the contents of any buried registers.

The PRELOAD waveform is shown in Figure 6. The PRELOAD registers mode is selected with the mode-select pins, the desired data to be loaded into the registers is placed on the appropriate I/O pins, and a positive pulse on pin 1 is applied. This clocks the new values into the registers, and the device can then be returned to normal operating mode.

The observability function allows the user to observe the outputs of all sixteen registers. To use the observability mode, simply select the observe registers mode with the mode-select pins. The register output is automatically selected (combinatorial mode is off), and the output will be the true side of the register (Q). The data will be present as long as the mode-select pins access the observe mode (even if pin 11 goes LOW, the output pins will still retain the data out of the registers). To exit the observe mode, simply change the mode-select pins while pin 11 is still at V_{PP}.

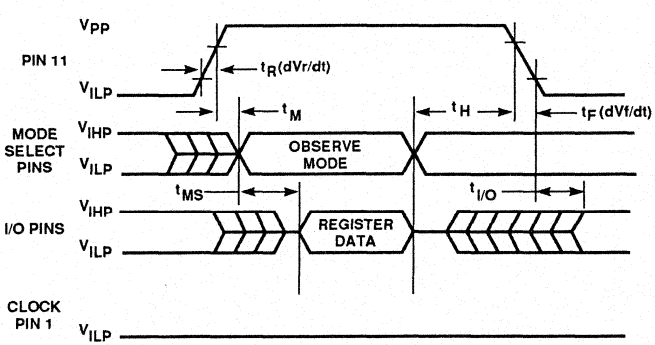
During observability, pin 1 should remain LOW. If pin 1 goes HIGH, the device will interpret this as a clock signal, and the previous data may be lost. As long as pin 1 remains LOW, the state of the registers will not change when going from normal-mode operation to observe mode or back.

Product terms provide an alternative method of enabling preload and observability. The preload and obervability product terms, when asserted, perform the same functions as the mode select pins and pin 11.



08811-040A

Figure 6. Preload Waveform



08811-041A

Figure 7. Observability Waveform

PRELOAD DC ELECTRICAL CHARACTERISTICS (T_A = 25°C ± 5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{PP}	PRELOAD Voltage	14.5	15.0	15.5	V
V_{ILP}	Input LOW Level During Prog/Verify	0	0	0.5	V
V_{IHP}	Input HIGH Level During Prog/Verify	3.0	4.0	V_{CC}	V
V_{OL}	Verify LOW		0.2	0.5	V
V_{OH}	Verify HIGH	2.4	3.4		V

Note:
AC undershoot on any input should be limited to –1 V.

Table 2.

	Pin 23	Pin 14	Pin 13	Pin 2
Preload	L	H	H	L
Observe	H	L	H	H

Table 3. Mode Pins

2

PRELOAD AC ELECTRICAL CHARACTERISTICS (T_A = 25°C ± 5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_M	Setup Before Applying Mode	50	50		µs
t_{MS}	Mode Setup Prior to Applying Data	1.0	1.0*		µs
t_{DS}	Data Setup Prior to Applying PRELOAD Latch Pulse	1.0	1.0*		µs
t_H	Data/Mode Hold After Latch Pulse	1.0	1.0*		µs
t_W	Data Latch Pulse Width	1.0	1.0*		µs
$t_{I/O}$	I/O Valid After Pin 11 Drops from V_{PP} to TTL Levels			100	µs
dVr/dt	V_{PP} Rising Slew Rate (Pin 11)	10		100	V/µs
dVf/dt	V_{PP} Falling Slew Rate (Pin 11)		2.0	3.0	V/µs

* Recommended value is as close to 1.0 µs plus tolerance as practical, but not less than 1.0 µs.

Table 4.

ENDURANCE CHARACTERISTICS

All PALCE29M16H devices are given multiple erase cycles (endurance cycles) at the factory.

Parameter Symbol	Parameter Description	Value	Unit	Test Conditions
t_{DR}	Minimum Pattern Data Retention Time	10	Years	Maximum Storage Temperature
N	Minimum Reprogramming Cycles	100	Cycles	Operating Conditions

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		100	µs
t_s	Input or Feedback Setup Time	See Switching Characteristics table		
t_w	Clock Width			
t_R	V_{CC} Rise Time	500		µs

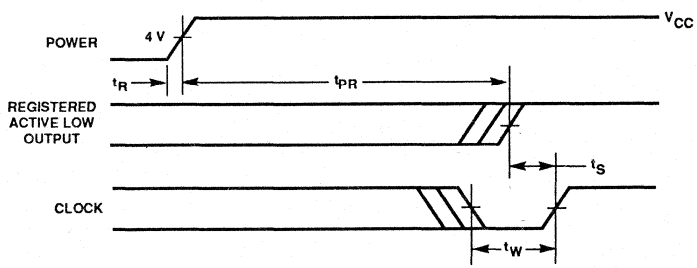


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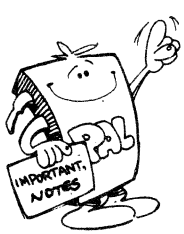
Figure 5. Power-Up Reset Waveform

2



Final COM'L

PALCE29MA16H-25/35

24-Pin EE CMOS Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High-performance semi-custom logic replacement; Electrically Erasable (E^2) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/ Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with common pin clock/latch enable ($\overline{LE}$) or individual product term clock/$\overline{LE}$ with LOW/HIGH clock/ $\overline{LE}$ polarity
- Register/Latch Preload permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-pin 300-mil SKINNYDIP® and 28-pin plastic leaded chip carrier packages

GENERAL DESCRIPTION

The PALCE29MA16H is a high-speed, E^2-based CMOS Programmable Array Logic device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming and excellent reliability. Programmable Array Logic (PAL®) devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

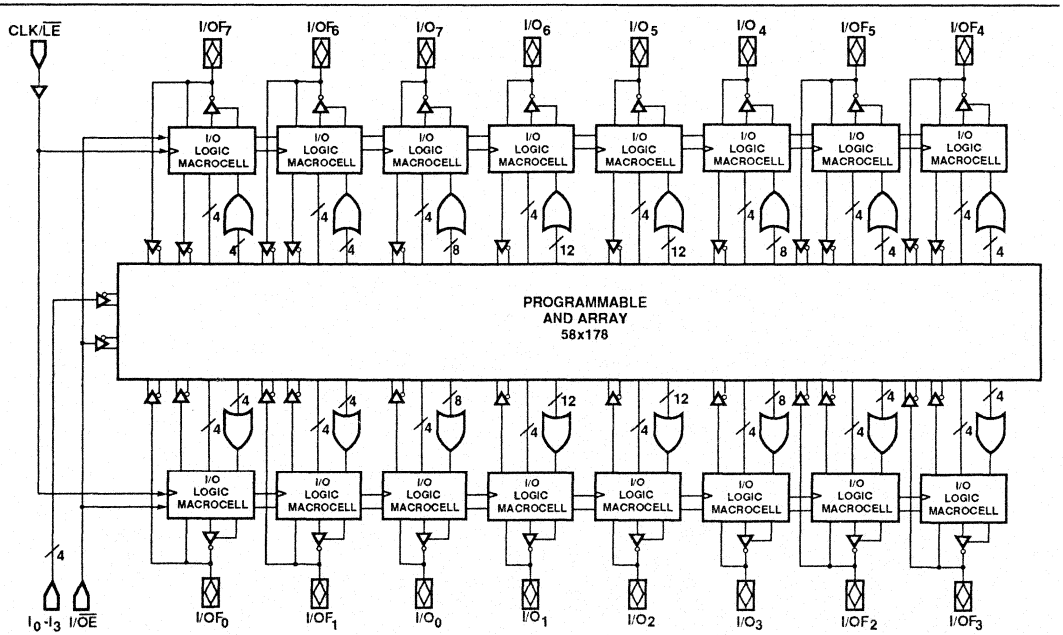


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Figure 1. Block Diagram

Publication # 08811 Rev. D Amendment /0
Issue Date: January 1990

GENERAL DESCRIPTION (Continued)

The PALCE29MA16H uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to twenty-nine array inputs and sixteen outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as "Combinatorial," "Registered," or "Latched" with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29MA16H by providing a varied number of logic product terms per output. Eight outputs have four product terms each, four outputs have eight product terms each, and the other four outputs have twelve product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or individual Output Enable product term. Each output can also be permanently enabled or disabled.

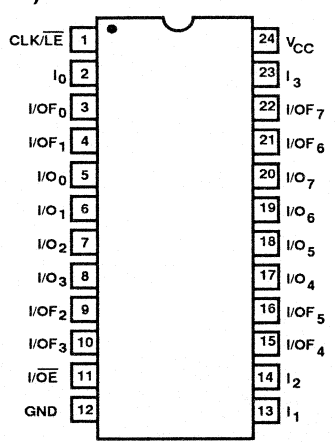
System operation has been enhanced by the addition of common asynchronous-PRESET and RESET product terms and a power-up RESET feature. The PALCE29MA16H also incorporates PRELOAD and Observability functions which permit full logic verification of the design.

The PALCE29MA16H is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS

(Top View)

SKINNYDIP



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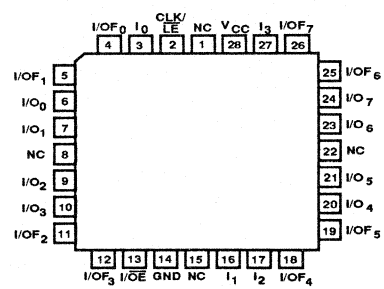
Note:
Pin 1 is marked for orientation.

PLCC



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Pin Designations:

I	= Input
I/O	= Input/Output
I/OF	= Input/Output with Dual Feedback
V_{CC}	= Supply Voltage
GND	= Ground
CLK/$\overline{LE}$	= Clock or Latch Enable
NC	= No Connection

PIN DESCRIPTION

The following describes the functionality of all the pins on the 24-pin SKINNYDIP. The 28-pin chip carrier has the same functionality with NO CONNECTS on pins 1, 8, 15, 22.

CLK/$\overline{LE}$ (PIN 1): Used as a dedicated clock/latch enable pin for all registers/latches on the device if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/$\overline{OE}$ PIN (PIN 11): Used as a dedicated input pin to the AND array or as the Output Enable control pin (Active LOW) for all macrocells with pin-controlled Output Enable selected.

I_0-I_3 (PINS 2, 13, 14, 23): Dedicated input pins.

I/OF_0-I/OF_7 (PINS 3, 4, 9, 10, 15, 16, 21, 22): Eight bidirectional I/O pins with two independent feedback paths to the AND array. The first feedback path is a dedicated I/O pin feedback to the AND array for combinatorial input. The second feedback path consists of direct register/latch feedback to the array (see Figure 2b).

I/O_0-I/O_7 (PINS 5, 6, 7, 8, 17, 18, 19, 20): Eight bidirectional I/O pins with user-programmable register/latch or I/O pin feedback to the AND array (see Figure 2a).

V_{CC} (PIN 24): Supply Voltage

GND (PIN 12): Circuit Ground.

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power/Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing

PAL CE 29 MA 16 H -25 P C

a. PROGRAMMABLE ARRAY LOGIC

CMOS ELECTRICALLY ERASABLE

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
MA = Advanced Asynchronous Macrocell

NUMBER OF FLIP-FLOPS

b. POWER/SPEED OPTION
Speed:
-25 = 25 ns
-35 = 35 ns
Power:
H = Half Power (100 mA)

c. PACKAGE TYPE
P = 24-Pin Plastic SKINNYDIP (PD3024)
D = 24-Pin Ceramic SKINNYDIP (CD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

d. TEMPERATURE RANGE
C = Commercial (0°C to +75°C)

e. OPTIONAL PROCESSING
Blank = Standard processing

Valid Combinations	
PALCE29MA16H-25 PALCE29MA16H-35	PC, DC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:

Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Inputs

The PALCE29MA16H has twenty-nine inputs to drive each product term (up to fifty-eight inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these twenty-nine inputs, four are dedicated inputs, sixteen are from eight I/O logic macrocells with two feedbacks, eight are from other I/O logic macrocells with single feedback and one is the I/$\overline{OE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the E^2 cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29MA16H has 178 product terms; 112 of these product terms provide logic capability and others are architectural product terms. Among the control product terms, one is for Observability, and one is for PRELOAD. The Output Enable of each macrocell can be programmed to be controlled by a common Output Enable pin or an individual product term. It may also be permanently enabled or permanently disabled. In addition, independent product terms for each macrocell control PRESET, RESET and CLK/$\overline{LE}$.

Each product term on the PALCE29MA16H consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from four to twelve wide, with an average of seven logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Individual asynchronous-PRESET and RESET product terms are connected to all Registered/Latched inputs/outputs.

When the asynchronous-PRESET product term is asserted (HIGH), the register/latch will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-RESET product term is asserted (HIGH), the register/latch will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the RESET/PRESET, PRELOAD, and power-up RESET modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29MA16H has sixteen macrocells, one for each I/O pin. Each I/O macrocell can be programmed for

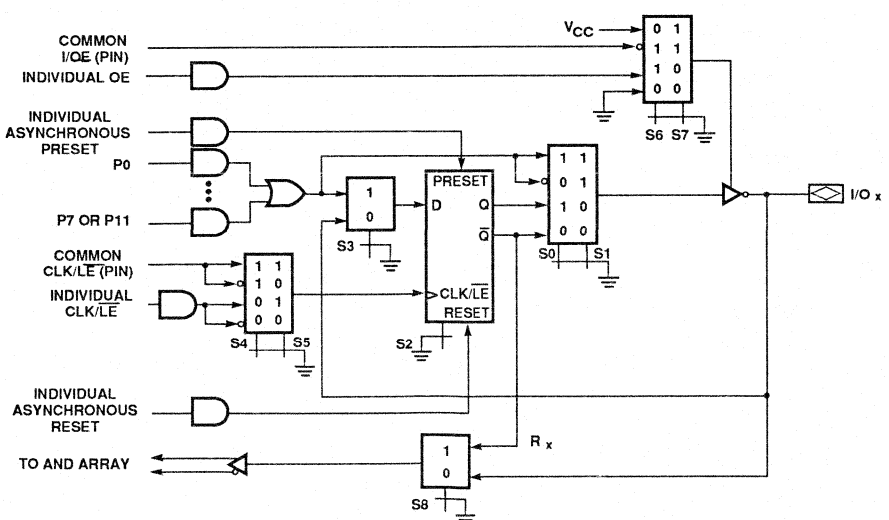

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Figure 2a. PALCE29MA16H Macrocell (Single Feedback)

combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers are used in synchronous logic applications while latches are used in asynchronous applications. Registers with product term controlled clocks can also be used in asynchronous applications.

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0-I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29MA16H has one dedicated CLK/$\overline{LE}$ pin and an individual CLK/$\overline{LE}$ product term. All macrocells have a programmable select to choose between these two as the clock or the latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by a product term.

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain nine E^2 cells, while the other eight macrocells contain eight E^2 cells for programming the input/output functions (see Table 1).

E^2 cell S1 controls whether the macrocell will be combinatorial or registered/latched. S0 controls the output polarity (active-HIGH or active-LOW). S2 determines whether the input/output is a register or a latch. S3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable E^2 cells S4 and S5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S6 and S7 are used to control Output Enable as pin controlled, product term controlled, permanently enabled, or permanently disabled. S8 controls a feedback multiplexer for the macrocells with a single feedback path only.

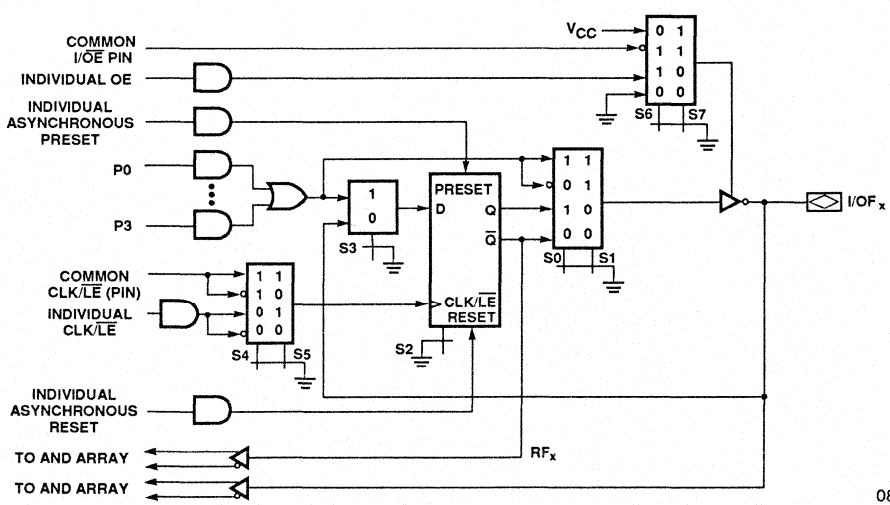


Figure 2b. PALCE29MA16H Macrocell (Dual Feedback)

Using the programmable E^2 cells S0-S8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the virgin erased state (charged, disconnected), an architectural cell is said to have a value of "1;" in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0."

S3	I/O Cell
1	Output Cell
0	Input Cell

S2	Storage Element
1	Register
0	Latch

S1	Output Type
1	Combinatorial
0	Register/Latch

S0	Output Polarity
1	Active LOW
0	Active HIGH

S8	Feedback*
1	Register/Latch
0	I/O

* Applies to macrocells with single feedback only.

Table 1a. PALCE29MA16H I/O Logic Macrocell Architecture Selections

S4	S5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE
0	1	CLK/$\overline{LE}$ PT positive-going edge, active-LOW LE
0	0	CLK/$\overline{LE}$ PT negative-going edge, active-HIGH LE

S6	S7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

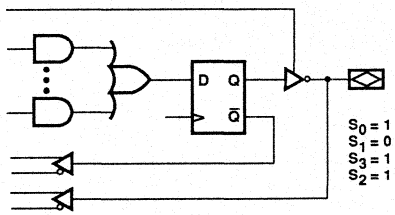
1 = Erased State (Charged or disconnected).
0 = Programmed State (Discharged or connected).

Table 1b. PALCE29MA16H I/O Logic Macrocell Clock Polarity and Output Enable Selections

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable.)

Output Registered/Active Low



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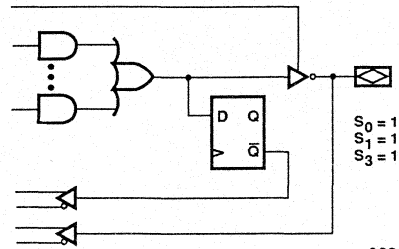
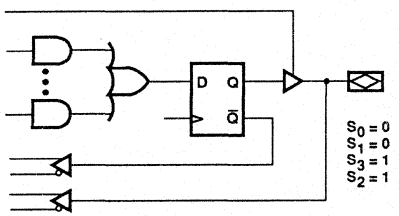
Output Combinatorial/Active Low



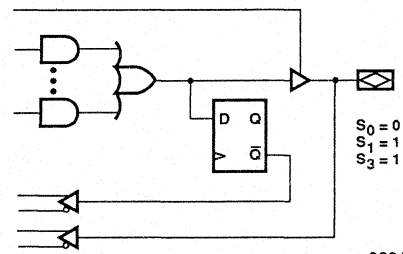
08811-007A

Output Registered/Active High



08811-008A

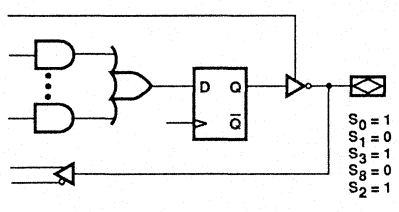
Output Combinatorial/Active High



08811-009A

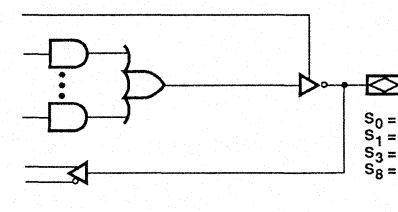
Figure 3a. Dual-Feedback Macrocells

Output Registered/Active Low, I/O Feedback



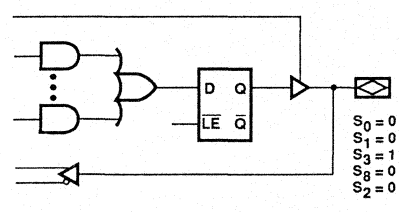
08811-010A

Output Combinatorial/Active Low, I/O Feedback



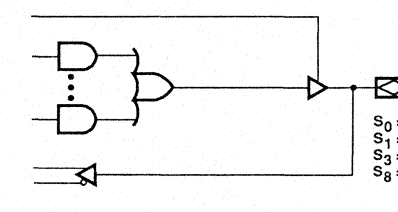
08811-011A

Output Latched/Active High, I/O Feedback



08811-012A

Output Combinatorial/Active High, I/O Feedback

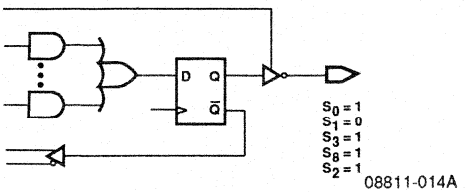


08811-013A

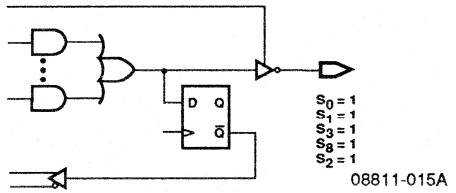
Figure 3b. Single-Feedback Macrocells

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL (Continued)

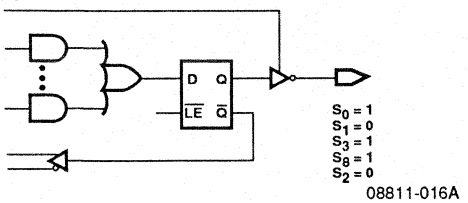
Output Registered/Active Low, Register Feedback



Output Combinatorial/Active Low, Register Feedback



Output Latched/Active Low, Latched Feedback



Output Combinatorial/Active Low, Latched Feedback

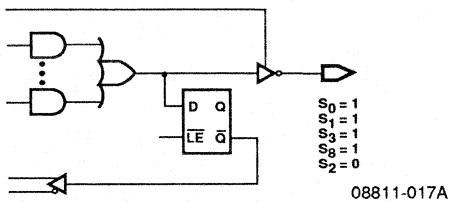


Figure 3b. Single-Feedback Macrocell (Continued)

Input Registered/Latched

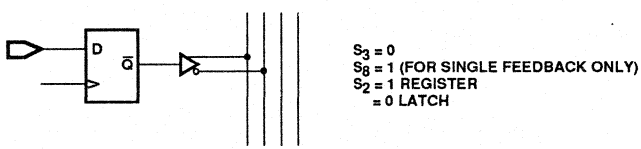


Figure 3c. All Macrocells

DESIGNED-IN TESTABILITY AND DEBUGGING

Preload

To simplify testing, the PALCE29MA16H is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. Both product term controlled and supervoltage-enabled PRELOAD modes are available. This offers even more test capability than previously implemented in AMD's PAL devices. The TTL-level PRELOAD product term can be useful during debugging, where supervoltages may not be available.

PRELOAD allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state", which can be checked to validate the transition from the "present state". In this way any transition can be checked.

Since PRELOAD can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

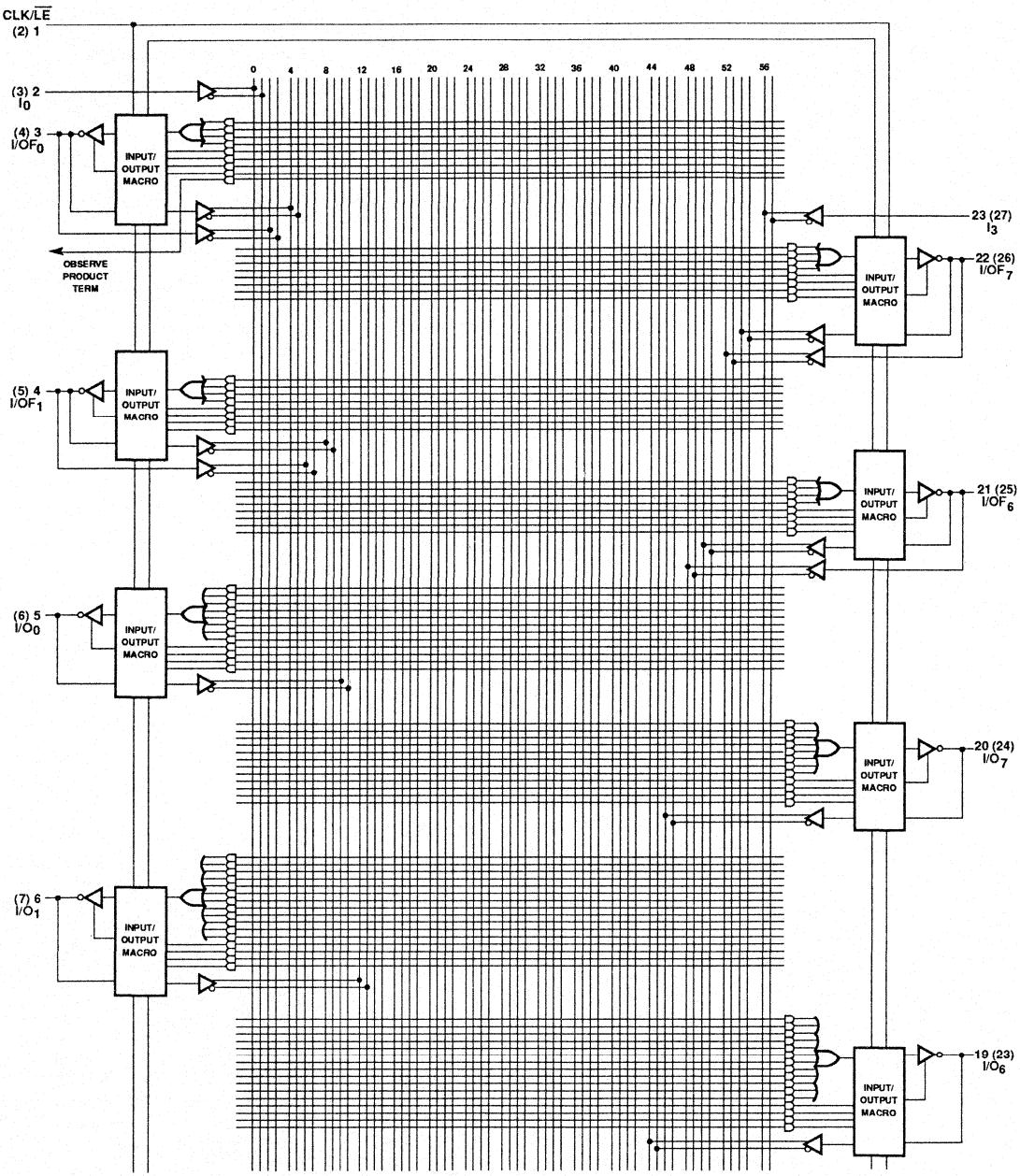
The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, PRELOAD, and the observability modes. The only way to erase the protection cell is by charging the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

LOGIC DIAGRAM

SKINNYDIP (PLCC) Pinouts

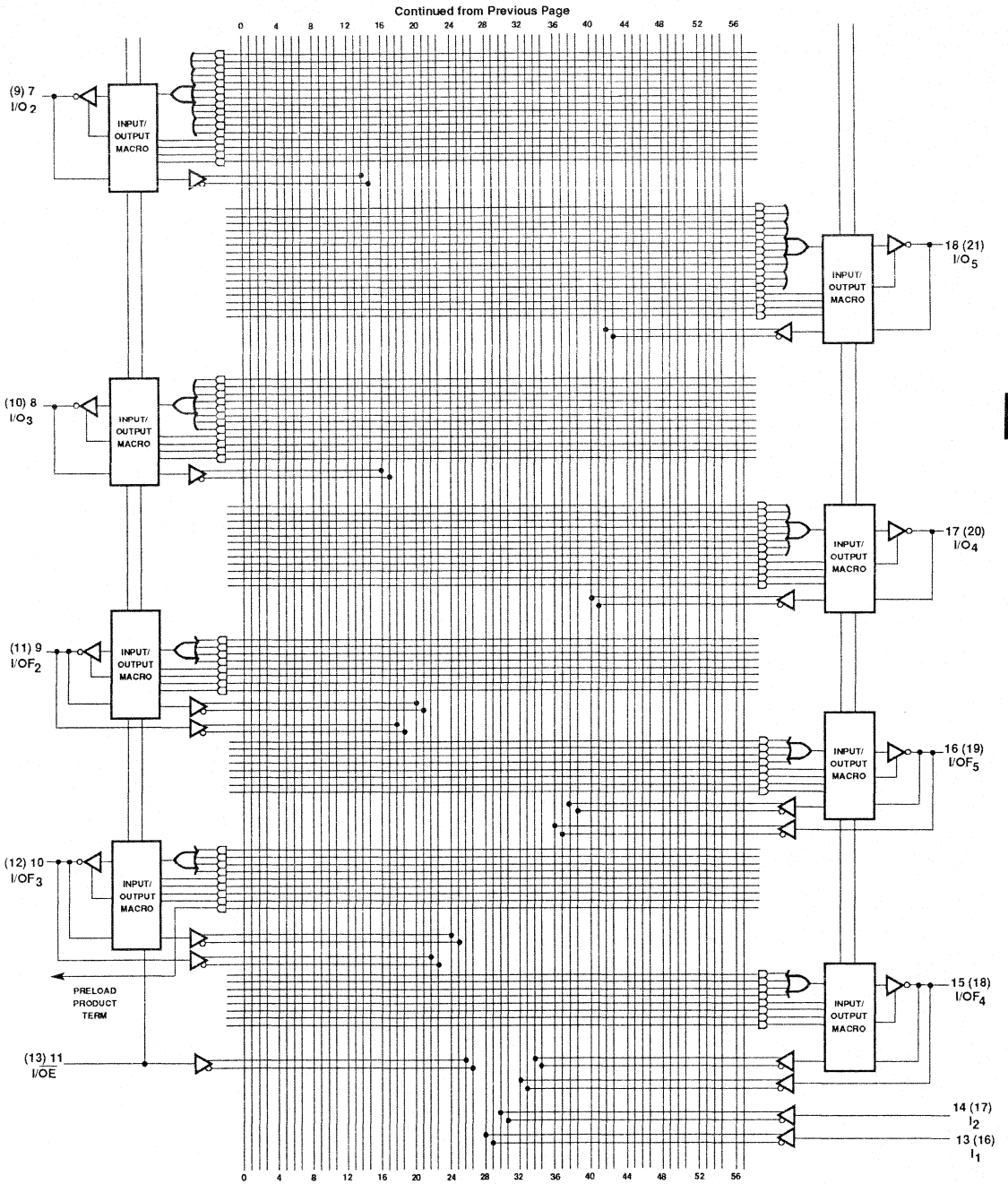


Continued on Next Page

08811-019A

LOGIC DIAGRAM (Continued)

SKINNYDIP (PLCC) Pinouts



08811-019A
(Concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage (Except Pin I/$\overline{OE}$)	−0.5 V to V_{CC} + 0.5 V
DC Input Voltage (Pin I/$\overline{OE}$)	−0.6 V to 16 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
DC Input Current	−1 mA to +1 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 6 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
		I_{OL} = 4 mA			0.33	
		I_{OL} = 20 µA			0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		−30	−90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			100	mA

Notes:

1. These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	

Note:

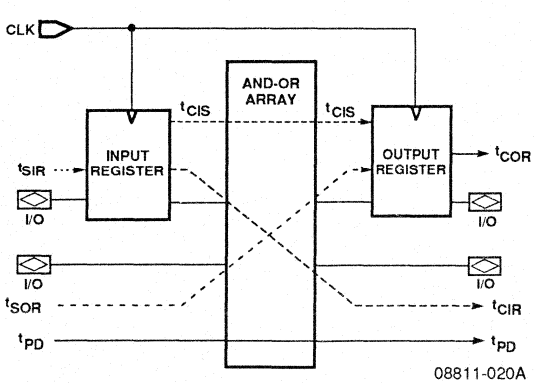
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS

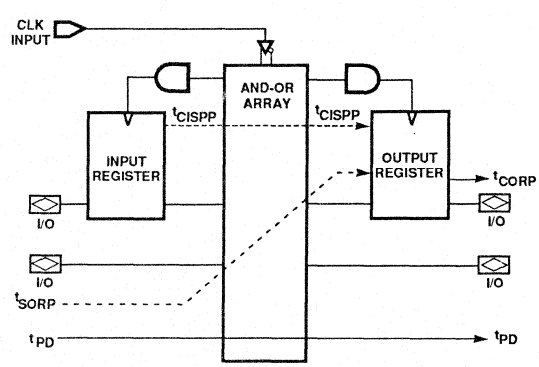
Over commercial range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 35 pF.

Registered Operation

Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Output						
t_{PD}	Input or I/O Pin to Combinatorial Output		25		35	ns
Output Register - Pin Clock						
t_{SOR}	Input or I/O Pin to Output Register Setup	15		20		ns
t_{COR}	Output Register Clock to Output		15		20	ns
t_{HOR}	Data Hold Time for Output Register	0		0		ns
Output Register - Product Term Clock						
t_{SORP}	I/O Pin or Input to Output Register Setup	4		6		ns
t_{CORP}	Output Register Clock to Output		29		34	ns
t_{HORP}	Data Hold Time for Output Register	10		12		ns
Input Register - Pin Clock						
t_{SIR}	I/O Pin to Input Register Setup	2		4		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28		36	ns
t_{HIR}	Data Hold Time for Input Register	6		8		ns
Clock and Frequency						
t_{CIS}	Register Feedback (Pin Driven Clock) to Output Register/Latch (Pin Driven) Setup	20		30		ns
t_{CISPP}	Register Feedback (PT Driven Clock) to Output Register/Latch (PT Driven) setup	25		30		ns
f_{MAX}	Maximum Frequency (Pin Driven) $1/(t_{SOR} + t_{COR})$	33.3		25		MHz
f_{MAXI}	Maximum Internal Frequency (Pin Driven) $1/t_{CIS}$	50		33.3		MHz
f_{MAXP}	Maximum Frequency (PT Driven) $1/(t_{SORP} + t_{CORP})$	30		25		MHz
f_{MAXIPP}	Maximum Internal Frequency (PT Driven) $1/t_{CISPP}$	40		33.3		MHz
t_{CWH}	Pin Clock Width HIGH	8		12		ns
t_{CWL}	Pin Clock Width LOW	8		12		ns
t_{CWHP}	PT Clock Width HIGH	12		15		ns
t_{CWLP}	PT Clock Width LOW	12		15		ns

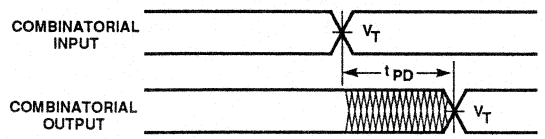


Input/Output Register Specs (Pin CLK Reference)



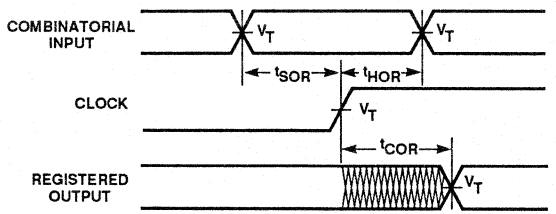
Input/Output Register Specs (PT CLK Reference)

SWITCHING WAVEFORMS



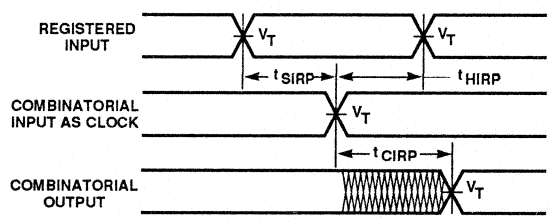
08811-022A

Combinatorial Output



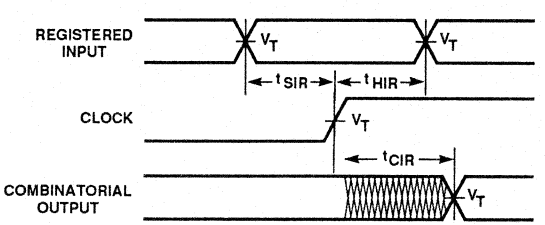
08811-023A

Output Register (Pin Clock)



08811-024A

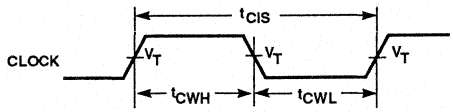
Output Register (PT Clock)



08811-025A

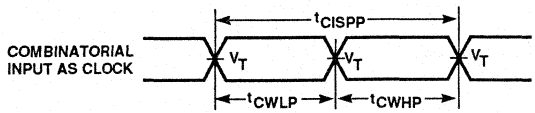
Input Register

SWITCHING WAVEFORMS (Continued)



08811-026A

Pin Clock Width



08811-027A

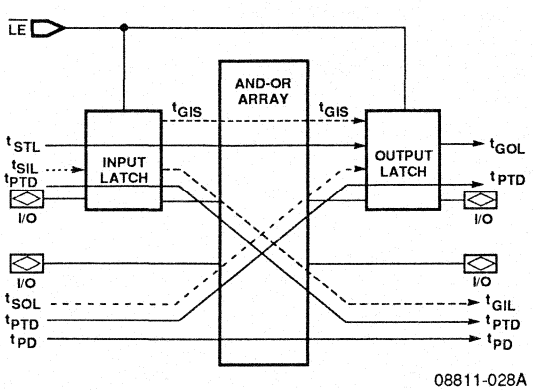
PT Clock Width

SWITCHING CHARACTERISTICS (Continued)

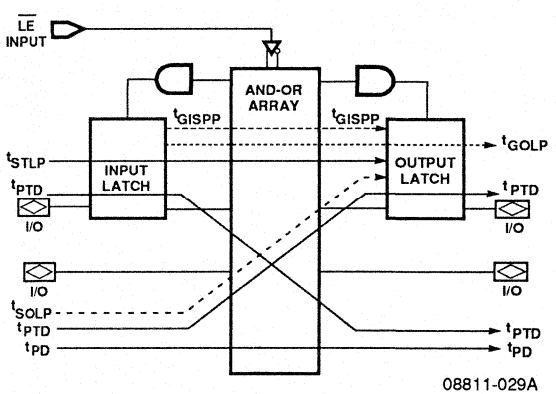
Over commercial range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 35 pF.

Latched Operation

Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Output						
t_{PD}	Input or I/O Pin to Combinatorial Output		25		35	ns
t_{PTD}	Input or I/O Pin to Output via Transparent Latch		28		36	ns
Output Latch - Pin LE						
t_{SOL}	Input or I/O Pin to Output Latch Setup	15		20		ns
t_{GOL}	Latch Enable to Transparent Mode Output		15		20	ns
t_{HOL}	Data Hold Time for Output Latch	0		0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		25		ns
Output Latch - PT LE						
t_{SOLP}	Input or I/O Pin to Output Latch Setup	4		6		ns
t_{GOLP}	Latch Enable to Transparent Mode Output		29		34	ns
t_{HOLP}	Data Hold Time for Output Latch	10		12		ns
t_{STLP}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	10		15		ns
Input Latch - Pin LE						
t_{SIL}	I/O Pin to Input Latch Setup	2		4		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28		36	ns
t_{HIL}	Data Hold Time for Input Latch	6		8		ns
Latch Enable						
t_{GIS}	Latch Feedback (Pin Driven) to Output Register/Latch (Pin Driven) Setup	20		30		ns
t_{GISPP}	Latch Feedback (PT Driven) to Output Register/Latch (PT Driven) Setup	25		30		ns
t_{GWH}	Pin Enable Width HIGH	8		12		ns
t_{GWL}	Pin Enable Width LOW	8		12		ns
t_{GWHP}	PT Enable Width HIGH	12		15		ns
t_{GWLP}	PT Enable Width LOW	12		15		ns

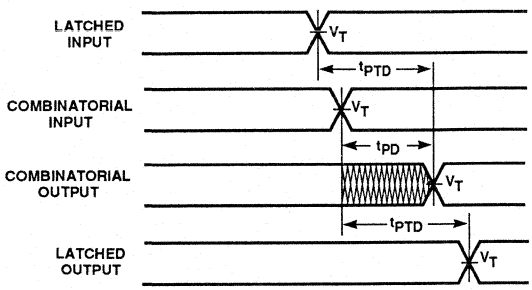


Input/Output Latch Specs (Pin $\overline{LE}$ Reference)



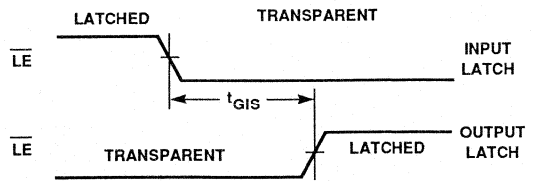
Input/Output Latch Specs (Pin $\overline{LE}$ Reference)

SWITCHING WAVEFORMS (Continued)



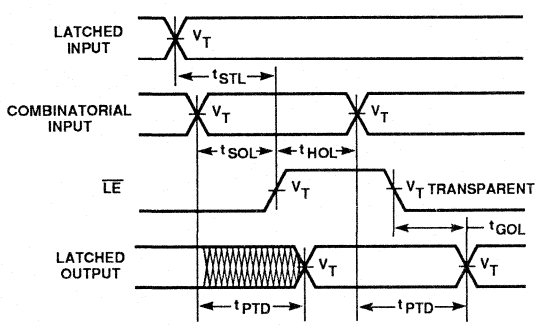
08811-030A

Latch (Transparent Mode)



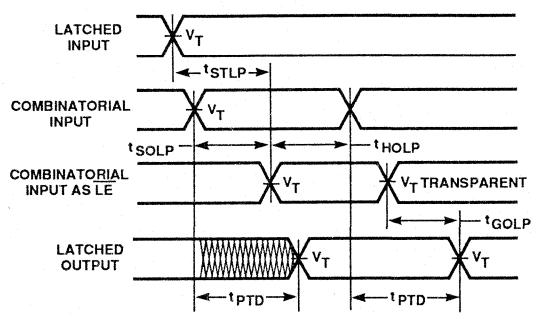
08811-031A

Input/Output Latch Relationship



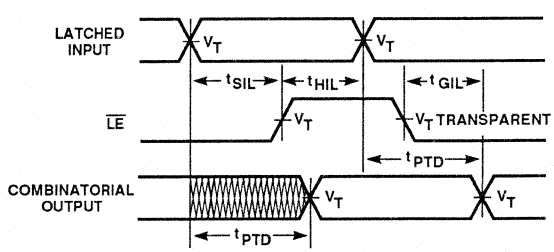
08811-032A

Output Latch (Pin $\overline{LE}$)



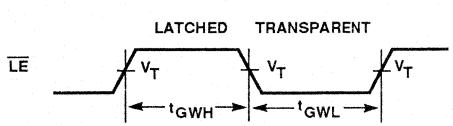
08811-033A

Output Latch (PT $\overline{LE}$)



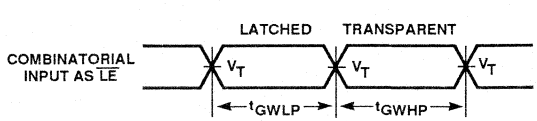
08811-034A

Input Latch (Pin $\overline{LE}$)



08811-035A

Pin $\overline{LE}$ Width



08811-036A

PT $\overline{LE}$ Width

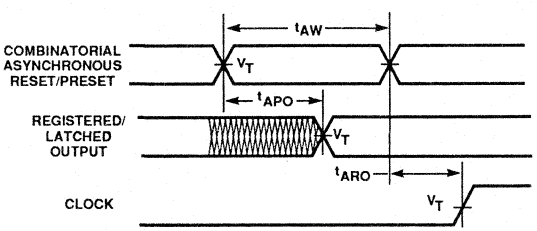
Reset/Preset, Enable

Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
t_{APO}	Input or I/O Pin to Output Register/Latch RESET/PRESET		30		40	ns
t_{AW}	Asynchronous RESET/PRESET Pulse Width	15		20		ns
t_{ARO}	Asynchronous RESET/PRESET to Output Register/Latch Recovery	15		20		ns
t_{ARI}	Asynchronous RESET/PRESET to Input Register/Latch Recovery	12		15		ns
t_{ARPO}	Asynchronous RESET/PRESET to Output Register/Latch Recovery PT Clock/LE	4		6		ns
t_{ARPI}	Asynchronous RESET/PRESET to Input Register/Latch Recovery PT Clock/LE	6		10		ns
Output Enable Operation						
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20		30	ns
t_{PXZ}*	I/$\overline{OE}$ Pin to Output Disable		20		30	ns
t_{EA}	Input or I/O to Output Enable via PT		25		35	ns
t_{ER}*	Input or I/O to Output Disable via PT		25		35	ns

* Output disable times do not include test load RC time constants.

2

SWITCHING WAVEFORMS (Continued)



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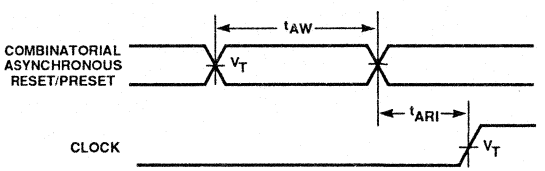
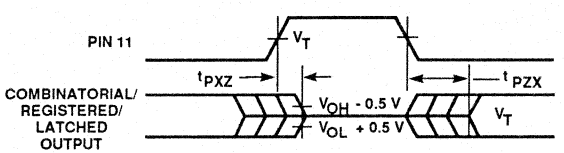
Output Register/Latch Reset/Preset



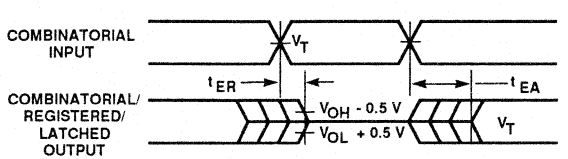
08811-038A

Input Register/Latch Reset/Preset



08811-039A

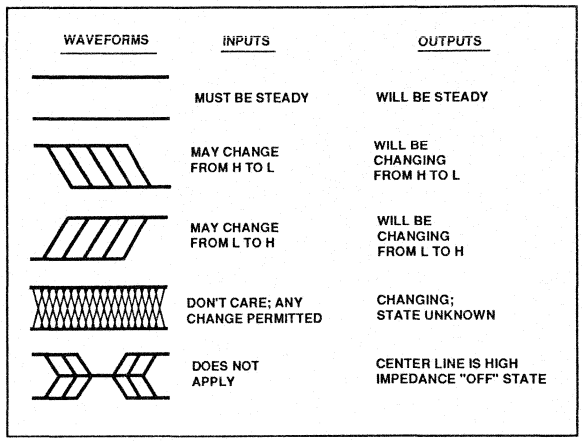
Pin 11 to Output Disable/Enable



08811-042A

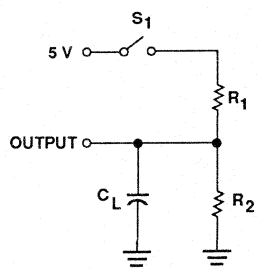
Input to Output Disable/Enable

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



08811-044A

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GO}	Closed	35 pF	620 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed	35 pF	620 Ω	390 Ω	1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF	620 Ω	390 Ω	H→Z: V_{OH} -0.5 V L→Z: V_{OL} +0.5 V

PRELOAD and OBSERVABILITY

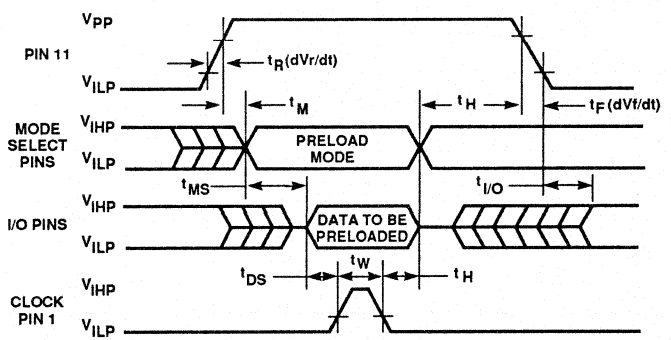
The PALCE29MA16H has special preload and observability modes designed in. The PRELOAD mode is very useful during structured vector testing after programming, while the observe mode allows the designer to see the contents of any buried registers.

The PRELOAD waveform is shown in Figure 6. The PRELOAD registers mode is selected with the mode-select pins, the desired data to be loaded into the registers is placed on the appropriate I/O pins, and a positive pulse on pin 1 is applied. This clocks the new values into the registers, and the device can then be returned to normal operating mode.

The observability function allows the user to observe the outputs of all sixteen registers. To use the observability mode, simply select the observe registers mode with the mode-select pins. The register output is automatically selected (combinatorial mode is off), and the output will be the true side of the register (Q). The data will be present as long as the mode-select pins access the observe mode (even if pin 11 goes LOW, the output pins will still retain the data out of the registers). To exit the observe mode, simply change the mode-select pins while pin 11 is still at V_{PP}.

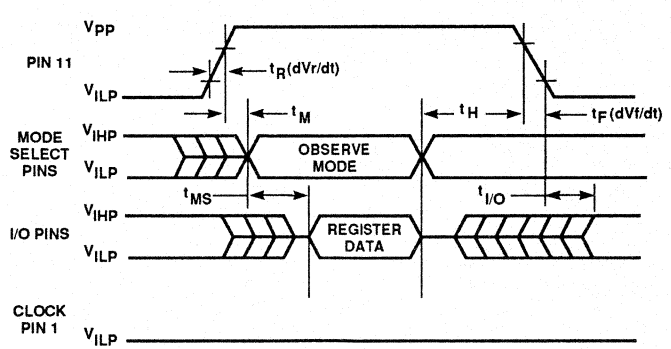
During observability, pin 1 should remain LOW. If pin 1 goes HIGH, the device will interpret this as a clock signal, and the previous data may be lost. As long as pin 1 remains LOW, the state of the registers will not change when going from normal-mode operation to observe mode or back.

Product terms provide an alternative method of enabling preload and observability. The preload and observability product terms, when asserted, perform the same functions as the mode select pins and pin 11.



08811-040A

Figure 6. Preload Waveform



08811-041A

Figure 7. Observability Waveform

PRELOAD DC ELECTRICAL CHARACTERISTICS (T_A = 25°C ± 5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{PP}	PRELOAD Voltage	14.5	15.0	15.5	V
V_{ILP}	Input LOW Level During Prog/Verify	0	0	0.5	V
V_{IHP}	Input HIGH Level During Prog/Verify	3.0	4.0	V_{CC}	V
V_{OL}	Verify LOW		0.2	0.5	V
V_{OH}	Verify HIGH	2.4	3.4		V

Note:
AC undershoot on any input should be limited to –1 V.

Table 2.

	Pin 23	Pin 14	Pin 13	Pin 2
Preload	L	H	H	L
Observe	H	L	H	H

Table 3. Mode Pins

PRELOAD AC ELECTRICAL CHARACTERISTICS (T_A = 25°C ± 5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_M	Setup Before Applying Mode	50	50		µs
t_{MS}	Mode Setup Prior to Applying Data	1.0	1.0*		µs
t_{DS}	Data Setup Prior to Applying PRELOAD Latch Pulse	1.0	1.0*		µs
t_H	Data/Mode Hold After Latch Pulse	1.0	1.0*		µs
t_W	Data Latch Pulse Width	1.0	1.0*		µs
$t_{I/O}$	I/O Valid After Pin 11 Drops from V_{PP} to TTL Levels			100	µs
dVr/dt	V_{PP} Rising Slew Rate (Pin 11)	10		100	V/µs
dVf/dt	V_{PP} Falling Slew Rate (Pin 11)		2.0	3.0	V/µs

* Recommended value is as close to 1.0 µs plus tolerance as practical, but not less than 1.0 µs.

Table 4.

ENDURANCE CHARACTERISTICS

All PALCE29MA16H devices are given multiple erase cycles (endurance cycles) at the factory.

Parameter Symbol	Parameter Description	Value	Unit	Test Conditions
t_{DR}	Minimum Pattern Data Retention Time	10	Years	Maximum Storage Temperature
N	Minimum Reprogramming Cycles	100	Cycles	Operating Conditions

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		100	µs
t_s	Input or Feedback Setup Time	See Switching Characteristics table		
t_w	Clock Width			
t_R	V_{CC} Rise Time	500		µs

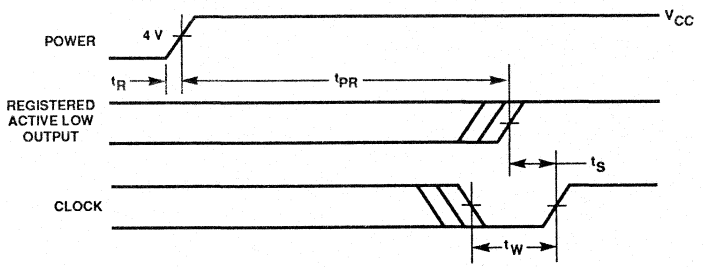


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Figure 5. Power-Up Reset Waveform

PAL32VX10/A

24-Pin Versatile with XOR Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Increased logic power**
  - Up to 32 inputs and 10 outputs
- **Dual independent feedback paths allow buried state registers or input registers**
- **Programmable flip-flops allow J-K, S-R, T or D types for efficient use of product terms**
- **10 input/output macrocells for flexibility**
- **Programmable registered or combinatorial outputs**
- **Individual user-programmable output polarity**
- **Global register asynchronous/synchronous preset/reset**
- **Automatic register preset on power up**
- **Preloadable output registers for testability**
- **Varied product term distribution**
  - Up to 16 product terms per output
- **300-mil SKINNYDIP® or PLCC packages**
- **Pin-compatible superset of PAL22V10**

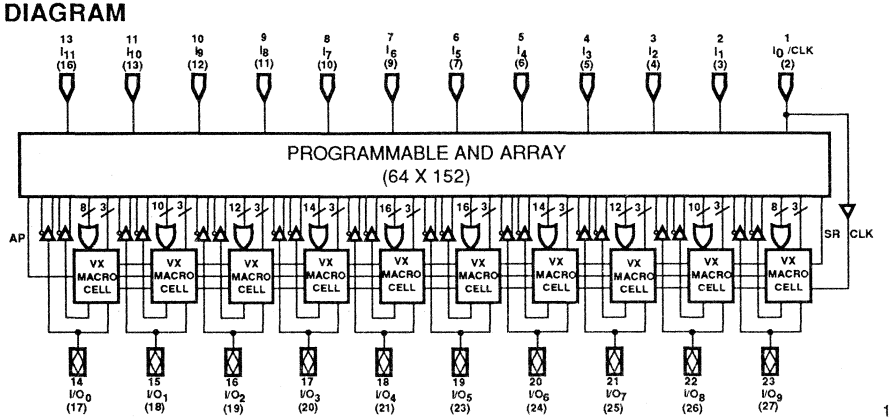
GENERAL DESCRIPTION

The PAL32VX10/A is a high-density Programmable Array Logic (PAL®) device which implements a sum-of-products transfer function via a user-programmable AND logic array and a fixed OR logic array. Featured are ten highly flexible input/output macrocells which are user-configurable for combinatorial or registered operation. Each flip-flop can be programmed to be either a J-K, S-R, T, or D-type for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial and registered configurations. This can be achieved even when register feedback is present, and allows implementation of buried flip-flops while preserving the external macrocell input. The PAL32VX10/A is supplied in a space-saving 300-mil-wide dual in-line package offering a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping. Security fuses defeat readout after programming and make proprietary designs difficult to copy.

The PAL32VX10/A is fabricated using Advanced Micro Devices' advanced oxide-isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Preloadable output registers facilitate functional testing.

The PAL32VX10/A can be programmed on standard PAL device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by AMD's PALASM® software as well as by other programmable logic CAD tools available from third-party vendors.

BLOCK DIAGRAM



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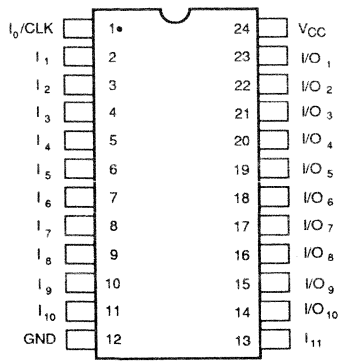
Publication # 10290 Rev. B Amendment/0
Issue Date: January 1990

CONNECTION DIAGRAMS

Top View

SKINNYDIP



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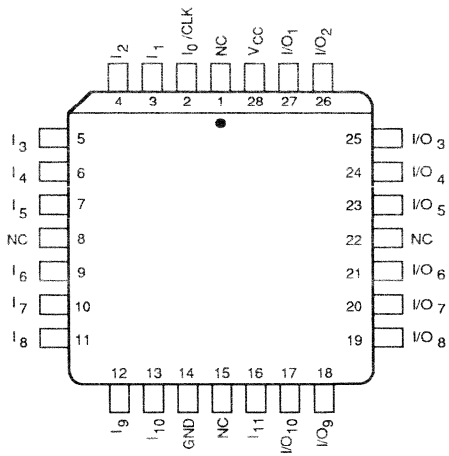
PLCC



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Note:

Pin 1 is marked for orientation.

PIN DESIGNATIONS

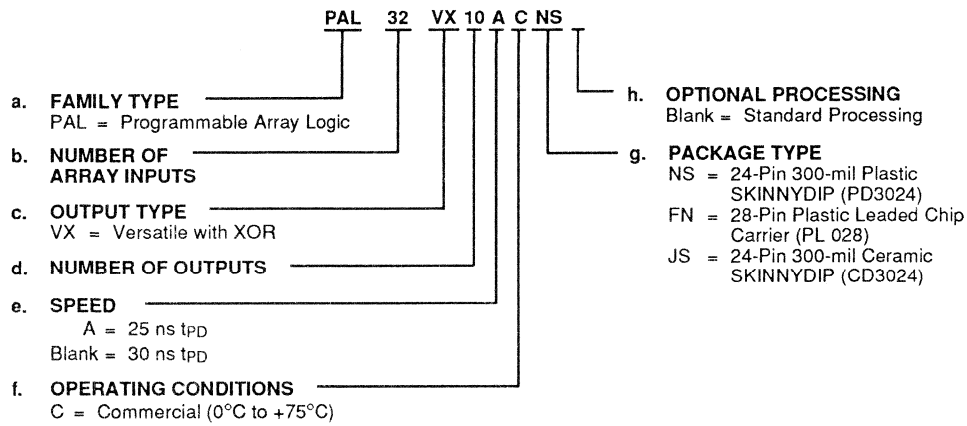
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Operating Conditions
g. Package Type
h. Optional Processing



Valid Combinations	
PAL32VX10	CNS, CFN, CJS
PAL32VX10A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

FUNCTIONAL DESCRIPTION

The PAL32VX10/A has twelve dedicated input lines and ten programmable I/O macrocells. Pin 1 serves either as an array input or as a clock for all flip-flops. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. The fuse matrix implements a programmable AND logic array, which drives a fixed OR logic array.

The high level of flexibility built into each macrocell, shown in Figure 1, allows the PAL32VX10/A to implement over thirty different architecture options. Each macrocell can be individually programmed to implement a variety of combinatorial or registered logic functions.

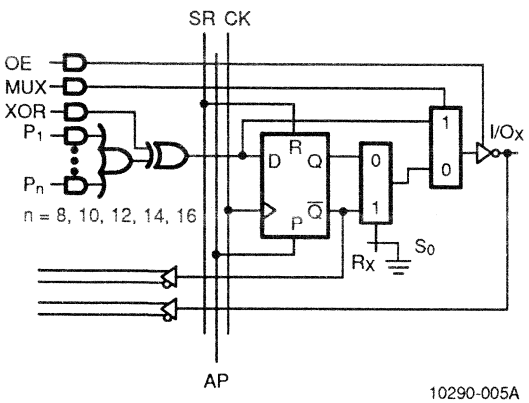


Figure 1. PAL32VX10/A Macrocell

Dual Output Feedback

Dual feedback paths associated with each macrocell provide independent feedback paths directly into the array from both the flip-flop output and the output pin. Unlike other devices which have a single feedback path, the PAL32VX10/A allows each output to have full I/O capability when configured as either a combinatorial output or a registered output, even if register feedback to the array is used. Thus registers can be loaded from their outputs.

If a macrocell is configured as a dedicated input, by disabling the three-state output buffer, the dual feedback architecture allows use of the associated register as an input register or as a "buried" state register, avoiding waste of the flip-flop, as shown in Figure 2.

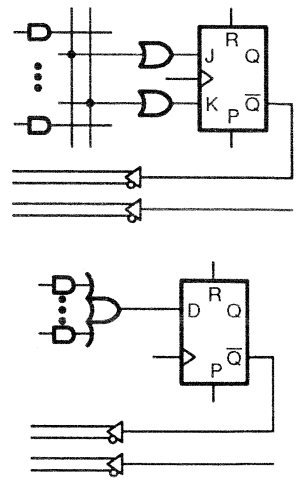


Figure 2. Buried Flip-Flops With Dedicated Inputs

Programmable Flip-flops

Each output macrocell contains a unique programmable flip-flop consisting of a basic D-type flip-flop driven by an XOR gate. This allows the user to choose the optimal flip-flop for the design, since either J-K, S-R, or T-type flip-flops can be synthesized from such a structure without wasting product terms.

As indicated in the macrocell logic diagram, one input of the XOR gate is connected to a single product term, while the second input is connected to the output of the OR logic array. The XOR gate output feeds the input of the D flip-flop. The way in which the XOR gate is used to synthesize the different flip-flop types is described in detail below.

D Flip-Flop. The D flip-flop option is implemented directly. In this configuration, the XOR gate on the input of the flip-flop can be used to program the logic polarity of the transfer function.

J-K Flip-Flop. The J-K flip-flop option can be easily synthesized with a more sophisticated manipulation of the XOR gate inputs and the D flip-flop output.

The transfer function of a J-K flip-flop can be mapped in the Karnaugh map of Figure 3, where Q+ represents the next state of the flip-flop:

J	K	Q=0	Q=1	
0	0	0	(1)	(HOLD)
0	1	0	0	(RESET)
1	1	(1)	0	(TOGGLE)
1	0	(1)	(1)	(SET)

Q+

10290-007A

Figure 3. J-K Flip-Flop Transfer Function

Dropping the (+) for simplicity, the equivalent Boolean expression for Q+ is:

$$Q = \overline{K}*Q + J*\overline{Q}$$

In general, J and K can be sum-of-product expressions which are provided in the PAL architecture only in active-high form. Thus, a direct implementation of $\overline{K}$ expressions must invoke a DeMorgan transformation, which can use excessive product terms. This can be avoided by rewriting the equation for Q without inversion on the J or K inputs.

The XOR gate can be used to construct a logically equivalent expression without any inversions on the J or K inputs. The rewritten Boolean expression is:

$$Q = Q :+: (J*\overline{Q} + K*Q)$$

To check that these expressions are logically equivalent, change the XOR to its equivalent sum-of-products form (remember $A :+: B = A*\overline{B} + \overline{A}*B$) and reduce (using DeMorgan's theorem):

$$Q = Q*\overline{(J*\overline{Q} + K*Q)} + \overline{Q}*(J*\overline{Q} + K*Q)$$

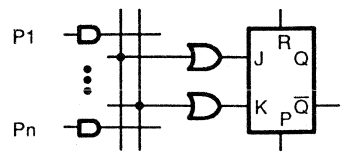
$$Q = Q*((\overline{J} + Q)*(\overline{K} + \overline{Q})) + \overline{Q}*J*\overline{Q} + \overline{Q}*K*Q$$

$$Q = Q*(\overline{J}*\overline{K} + \overline{J}*\overline{Q} + Q*\overline{K} + Q*\overline{Q}) + J*\overline{Q}$$

$$Q = \overline{J}*\overline{K}*Q + \overline{K}*Q + J*\overline{Q}$$

which simplifies to $Q = \overline{K}*Q + J*\overline{Q}$

Since J and K are, in general, sums of products, J and K in either expression can be substituted with (J1 + J2 + ... + Jm) and (K1 + K2 + ... + Kn-m), where n is the total number of product terms associated with a given output macrocell. Thus, the total n-product term resource is shared between the J and K control inputs (Figure 4). Note that all J terms will contain $\overline{Q}$ and all K terms will contain Q.



n = 8, 10, 12, 14, 16

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Figure 4. J-K Flip-Flop Logic Equivalent; J and K Can Also Be Active-Low

The above discussions have assumed that it was most convenient to "group ones" in the Karnaugh map. Sometimes it takes fewer product terms to "group zeros", i.e., implement the inversion of the desired function. The equations shown in Table 1 are equivalent and can be interchanged to optimize product term utilization. This can be readily proved through logic reductions similar to that above.

J and K active high	$Q = Q :+: (J*\overline{Q} + K*Q)$
J active high, K active low	$Q = J*\overline{Q} + \overline{K}*Q$
J active low, K active high	$\overline{Q} = \overline{J}*\overline{Q} + K*Q$
J and K active low	$Q = \overline{Q} :+: (\overline{J}*\overline{Q} + \overline{K}*Q)$

Note:

J = sum of products J1 + J2 + ... + Jm

K = sum of products K1 + K2 + ... + Kn-m

n = total number of available product terms for a given macrocell (8 to 16)

Table 1. J-K Flip-Flop Transfer Functions

S-R Flip-Flop. The S-R flip-flop has a truth table identical to that of the J-K flip-flop, with the exception that the J = K = 1 (toggle) condition is not allowed. The S-R flip-flop implementation is identical to that of the J-K flip-flop, with J-K replaced by S-R, and the S = R = 1 condition avoided.

T Flip-Flop. A T (toggle) flip-flop either holds its state or toggles, depending on the logic state of the T input. The T flip-flop is a subset of the J-K flip-flop and can be considered equivalent to a J-K type with J = K. The general transfer function and its active-low T equivalent are both given in Table 2.

$Q = Q :+: T$
$Q = \overline{Q} :+: \overline{T}$

Note:

T = sum of products T1 + T2 +T3 + ... + Tn

Table 2. J-K Flip-Flop Transfer Functions

Flip-flop Summary

The PAL32VX10/A can synthesize J-K, S-R, T, and D flip-flops, whichever is most convenient for the application, without sacrificing product terms. Additionally, the synthesized equations can use the active-high or active-low forms of the inputs, allowing the designer to minimize product term requirements.

Flip-flop Bypass

Any output in the PAL32VX10/A can be configured to be combinatorial by bypassing the output flip-flop. This is done by setting the output multiplexer to the appropriate state. The multiplexer is controlled by a product term which can be set unconditionally for a permanent combinatorial (all fuses opened, product term high) or registered (all fuses intact, product term low) output configuration, or can be programmed to bypass the output flip-flop "on the fly" allowing signals to be routed directly to output pins under user-specified conditions.

Varied Product Term Distribution

An increased number of product terms has been provided in the PAL32VX10/A over previous generation PAL devices. These terms are distributed among the ten macrocells in a varied manner, ranging from eight to sixteen terms per output. The five output pairs have 8, 10, 12, 14, or 16 product terms available for the OR gate within each macrocell. In addition, each macrocell has one XOR product term and two architecture control product terms.

Programmable I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control is implemented by a single product term, allowing specification of enable/disable functions controlled by any device input or output. Each macrocell can be configured as a dedicated input by disabling the buffer drive capability. When this is done, the associated register can still be used as an input register or buried state register, due to the independent register feedback path.

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic LOW state following a LOW-to-HIGH transition on pin 1 (I_0/CLK) when the synchronous reset (SR) product term is asserted. The register will be forced to the logic HIGH state independent of the clock when the asynchronous preset (AP) product term is asserted.

Programmable Polarity

The polarity of each macrocell output can be set active high or active low.

Combinatorial Outputs. The XOR gate provides polarity control for combinatorial outputs, with the single product term to the XOR gate controlling the invert/not invert function. With all fuses intact, there is no inversion through the XOR gate, creating an active-low output. Opening all fuses forces the product term high, inverting data and creating an active-high output.

Registered Outputs. Output polarity for registered outputs can be determined in two ways. For D-type registered outputs, polarity can be set by the XOR gate, as is the case with combinatorial outputs. Using this method to set polarity, preset and reset will not be affected.

Polarity, as observed from the output pin, can also be determined by the flip-flop output multiplexer. Note that this does not affect the polarity of the register feedback signal, but does affect preset and reset. By changing the flip-flop output multiplexer, the preset and reset functions are exchanged relative to the controlling product terms.

With the multiplexer fuse intact, the $\overline{Q}$ output is routed to the output pin, configuring an active-low output. With the multiplexer fuse opened, Q is routed to the output pin and synchronous reset becomes synchronous preset. Similarly, asynchronous reset becomes asynchronous preset.

Polarity options for J-K, S-R, and T flip-flops have been discussed in the section on programmable flip-flops.

Power-up Preset

All flip-flops power up to a logic HIGH for predictable system initialization. Outputs of the PAL32VX10/A will be HIGH or LOW depending on the state of the register output multiplexers.

Register Preload

The register on the PAL32VX10/A can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading in illegal states and observing proper recovery.

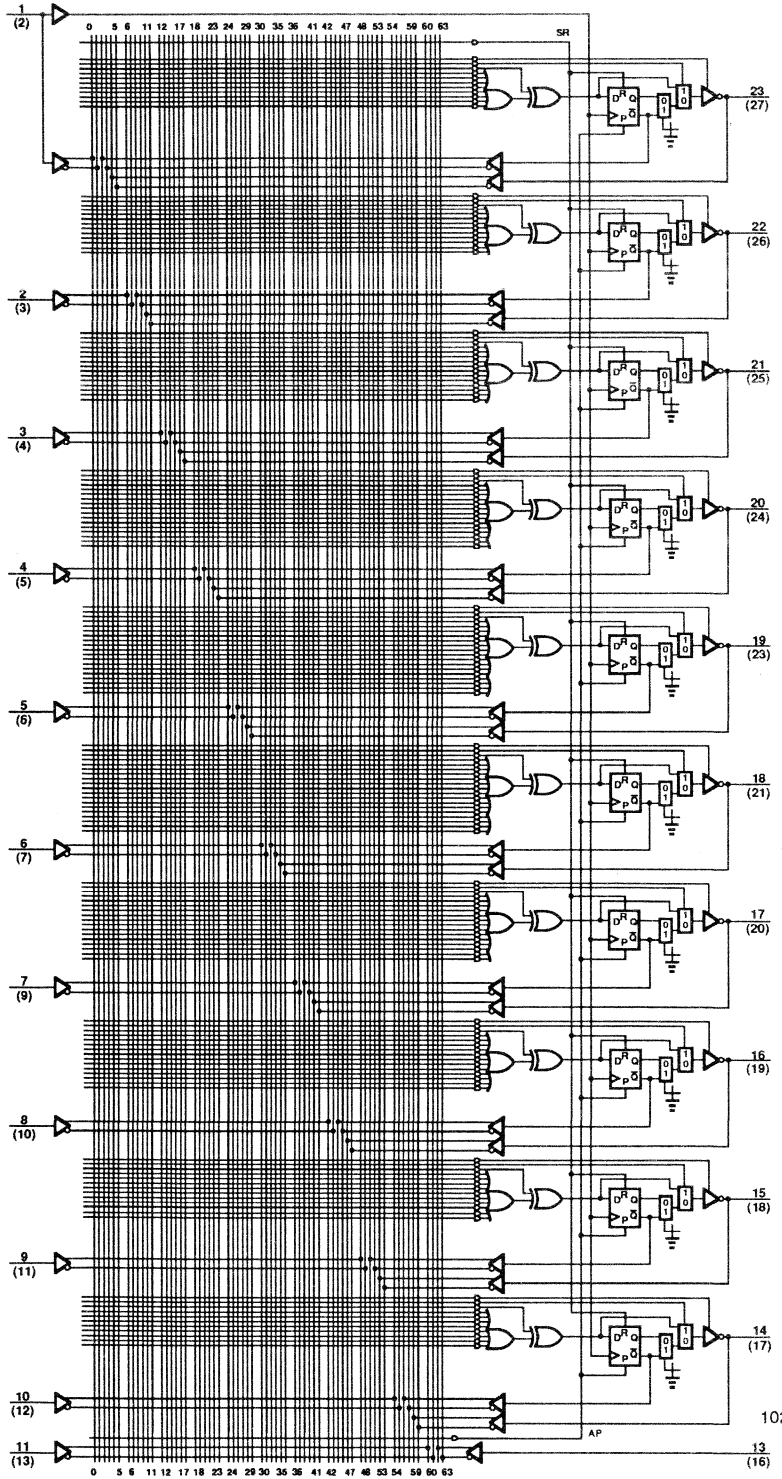
Security Fuse

After programming and verification, a PAL32VX10/A design can be secured by programming the security fuses. Once programmed, these fuses defeat readback of the internal fuse pattern by a device programmer, making proprietary designs very difficult to copy. The array will read as if every fuse is programmed.

Quality and Testability

The PAL32VX10/A offers a very high level of built-in quality. Special on-chip test circuitry provides a means of verifying performance of all AC and DC parameters prior to programming. In addition, these built-in test paths verify complete functionality of each device to provide the highest post-programming functional yields in the industry.

LOGIC DIAGRAM
SKINNYDIP
(PLCC) Pinouts



10290-004A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		11	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

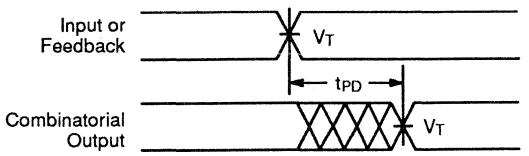
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				A		Std		Unit
					Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output	Product Terms P_1–P_n				25		30	ns
		Product Term XOR				30		35	
t_S	Setup Time from Input, Feedback, or SP to Clock	Product Terms P_1–P_n, SR			25		30		ns
		Product Term XOR			30		35		
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output					15		15	ns
t_{AP}	Asynchronous Preset to Registered Output					25		30	ns
t_{APW}	Asynchronous Preset Width				25		30		ns
t_{APR}	Asynchronous Preset Recovery Time				25		30		ns
t_{SRR}	Synchronous Reset Recovery Time				25		30		ns
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration (Product Term MUX 1→ 0)					90		90	ns
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration (Product Term MUX 0 → 1)					90		90	ns
t_{WL}	Clock Width	LOW			18		20		ns
t_{WH}		HIGH			18		20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	Product Terms P_1–P_n	25		22.5		MHz
				Product Term XOR	22.2		20		
		No Feedback	$1/(t_{WH} + t_{WL})$		27.7		25		MHz
t_{EA}	Input to Output Enable Using Product Term Control					25		30	ns
t_{ER}	Input to Output Disable Using Product Term Control					25		30	ns

Notes:

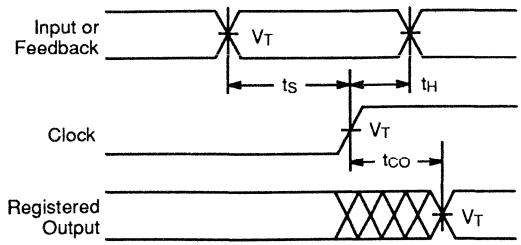
2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

SWITCHING WAVEFORMS



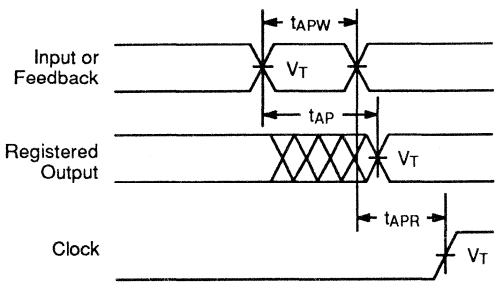
12015-010A

Combinatorial Output



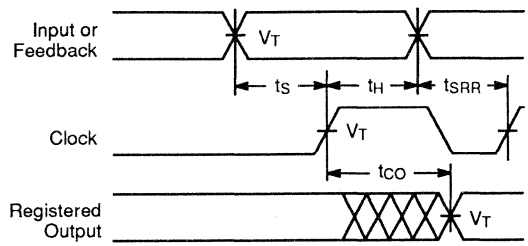
12015-012A

Registered Output



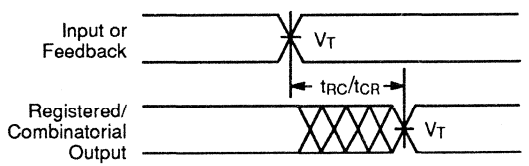
10290-007A

Asynchronous Preset



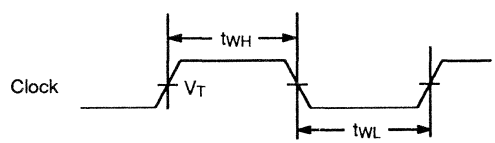
10290-008A

Synchronous Reset



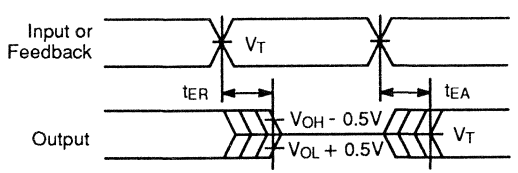
10290-009A

Configuration Change



12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

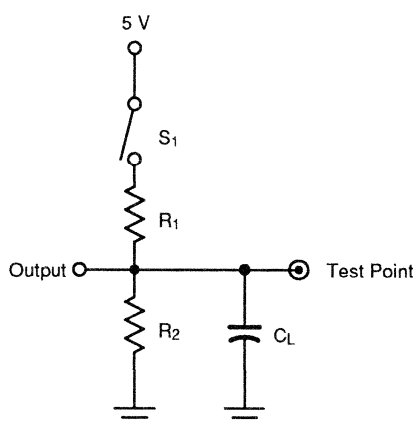
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT



12350-019A

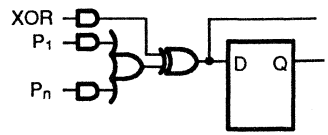
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} - 0.5 V L → Z: V_{OL} + 0.5 V

USE OF XOR PRODUCT TERM

The speed of the PAL32VX10/A is specified according to the use of the Exclusive-OR (XOR) product term in the macrocell. Note that the macrocell data input is a function of the two-input XOR gate, whose inputs are the OR of the product terms P_1–P_n and the single additional XOR product term (Figure 5).

The specification for the path through the single XOR product term is 5 ns slower than through the P_1–P_n product terms and the OR gate. As a result, if the single XOR product term is changing, the macrocell data input will not be available until 5 ns later than if only the P_1–P_n product terms were changing.

This difference between paths affects t_{PD}, t_S and f_{MAX} (feedback). As a result, these three parameters are specified both for only the P_1–P_n product terms changing ("Product terms P_1–P_n") and with the single XOR product term changing ("Product term XOR") (See table).



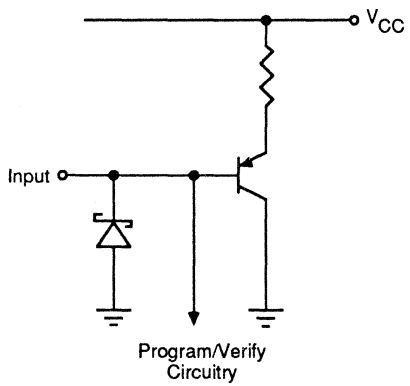
10290-012A

Figure 5. XOR Product Term

Specification		Explanation
t_{PD}, t_S, f_{MAX} (feedback)	Product Terms P_1–P_n	If only the P_1–P_n product terms are changing (XOR term is not changing)
	Product Term XOR	If XOR term is changing

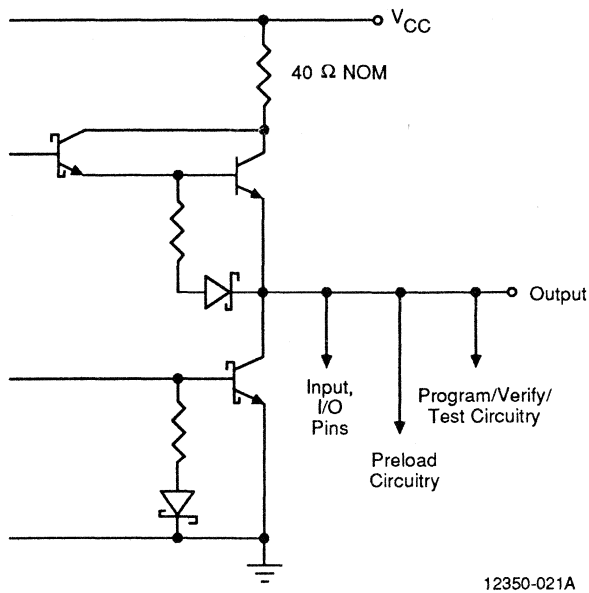
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



12350-020A

Typical Output



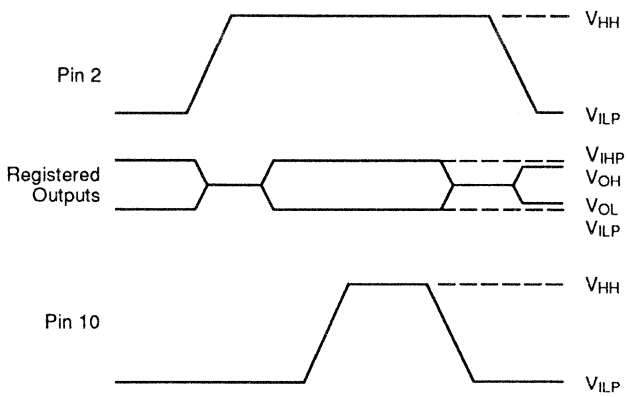
12350-021A

OUTPUT REGISTER PRELOAD

The Preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows:

1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 2 to V_{HH} (12 V).
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial outputs floating.
4. Pulse pin 10 to V_{HH}, then back to 0 V.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Remove high voltage from pin 2.
7. Enable output registers per programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11	11.5	12	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V



10290-011A

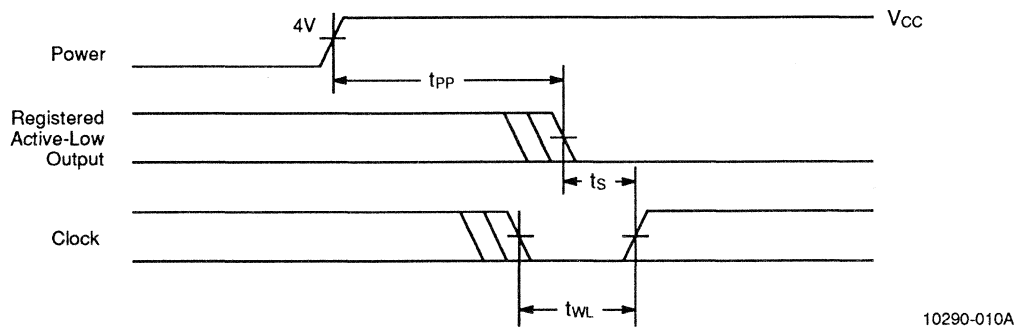
Output Register Preload Waveform

POWER-UP PRESET

The power-up preset feature ensures that all flip-flops will be preset to HIGH after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up preset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up preset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following preset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max.	Unit
t_{PP}	Power-Up Preset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Preset Waveform

PALCE610H-15/25

EE CMOS High Performance Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- AMD's Programmable Array Logic (PAL®) architecture
- Electrically-erasable CMOS technology providing half power (90 mA I_{CC}) at high speed
  -15 = 15 ns t_{PD}
  -25 = 25 ns t_{PD}
- Sixteen macrocells with configurable I/O architecture
- Registered or combinatorial operation
- Registers programmable as D, T, J–K, or S–R
- Asynchronous clocking via product term or bank register clocking from external pins
- Register preload for testability
- Power-up reset for initialization
- Space-saving 24-pin SKINNYDIP® and 28-pin PLCC packages
- Fully tested for 100% programming yield and high reliability
- Easy design with PALASM® software

2

GENERAL DESCRIPTION

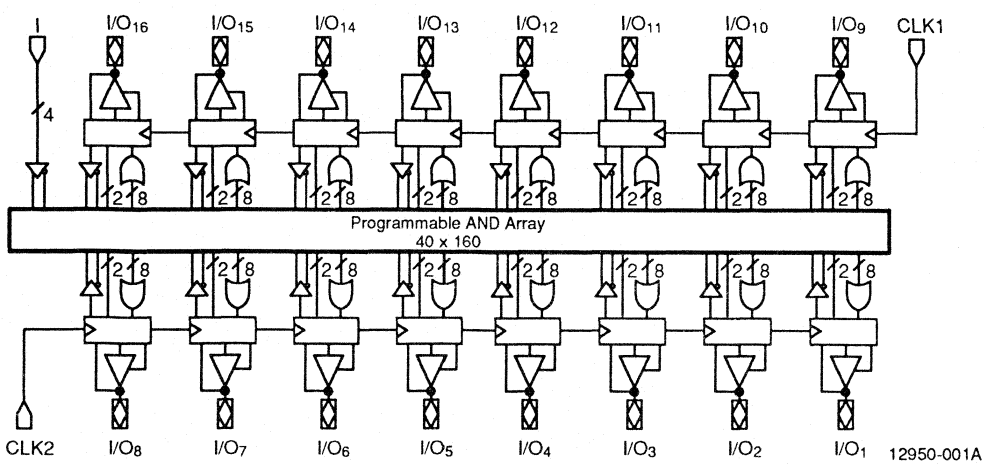
The PALCE610 is a general purpose PAL device and is functionally and fuse map equivalent to the EP610. It can accommodate logic functions with up to 20 inputs and 16 outputs. There are 16 I/O macrocells that can be individually configured to the user's specifications. The macrocells can be configured as either registered or combinatorial. The registers can be configured as D, T, J–K, or S–R flip-flops.

The PALCE610 uses the familiar sum-of-products logic with programmable-AND and fixed-OR structure. Eight product terms are brought to each macrocell to provide logic implementations.

The PALCE610 is manufactured using advanced CMOS EE technology providing high density and low power consumption. Moreover, it is a high-speed device having a worst-case t_{PD} of 15 ns. Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages are offered.

This device can be erased and reprogrammed at least 100 times. Data retention is guaranteed for 20 years. Once a device is programmed the security bit can be used to provide protection from copying a proprietary design.

BLOCK DIAGRAM

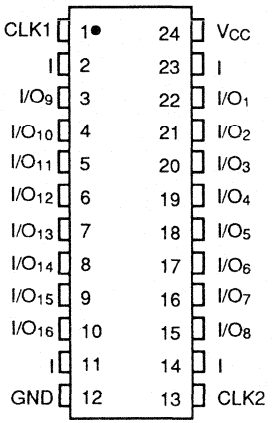


Publication # 12950 Rev. A Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAMS

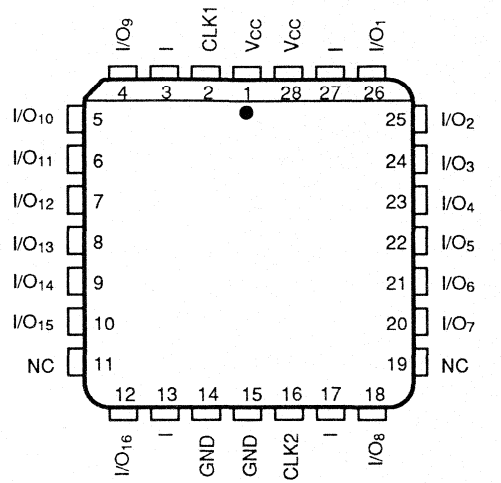
Top View

SKINNYDIP



12950-002A

PLCC



12950-003A

Note:
Pin 1 is marked for orientation

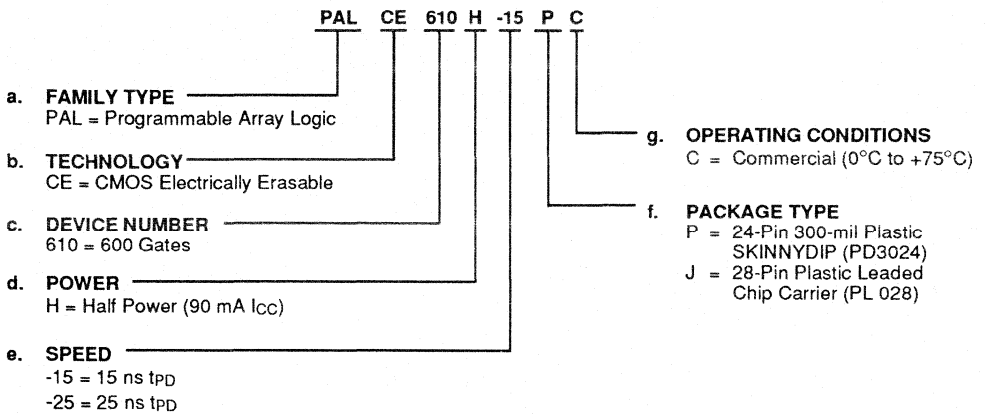
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Device Number
d. Power
e. Speed
f. Package Type
g. Operating Conditions



Valid Combinations	
PALCE610H-15	PC, JC
PALCE610H-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The PALCE610 is a general purpose programmable logic device. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J–K, or S–R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Each clock pin controls 8 of the 16 macrocells.

The programming matrix implements a programmable AND logic array which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input polarity. Unused input pins should be tied to V_{CC} or ground.

The array uses AMD's electrically erasable technology. An unprogrammed bit is disconnected and a programmed bit is connected. Product terms with all bits unprogrammed assume the logical-HIGH state and product terms with both the TRUE and Complement bits programmed assume the logical-LOW state.

The programmable functions in the PALCE610 are automatically configured from the user's design specifications, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to the programmer, configures the design according to the user's desired function.

Macrocell Configurations

The PALCE610 macrocell can be configured as either combinatorial or registered I/O. Both the combinatorial and registered configurations have output polarity control. The register can be configured as a D, T, J–K, or S–R type flip-flop. Figure 1 shows the possible configurations.

Each macrocell can select as its clock either the corresponding clock pin or the CLK/OE product term. If the clock pin is selected, the output enable is controlled by the CLK/OE product term. If the CLK/OE product term is selected, the output is always enabled.

Combinatorial I/O

All 8 product terms are available to the OR gate. The output-enable function is performed by the CLK/OE product term.

Registered Configurations

There are 4 flip-flop types available: D, T, J–K and S–R.

The registers can be configured as synchronous or asynchronous. In the synchronous configuration, the clock is controlled by the clock input pin. The output enable is controlled by the product term function. In the asynchronous configuration, the clock input is controlled by the product term. The output is always enabled.

D Flip-Flop

All 8 product terms are available to the OR gate. The D input polarity is controlled by an exclusive-OR gate. For the D flip-flop, the output level is the D-input level at the rising edge of the clock.

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

T Flip-Flop

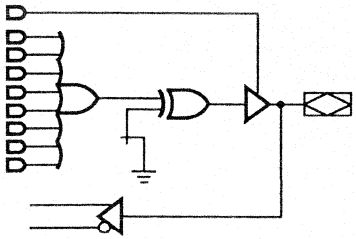
All 8 inputs are available to the OR gate. The T-input polarity is controlled by an exclusive-OR gate. For the T register, the output level toggles when the T input is HIGH and remains the same when the T input is LOW.

T	Q^n	Q^{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

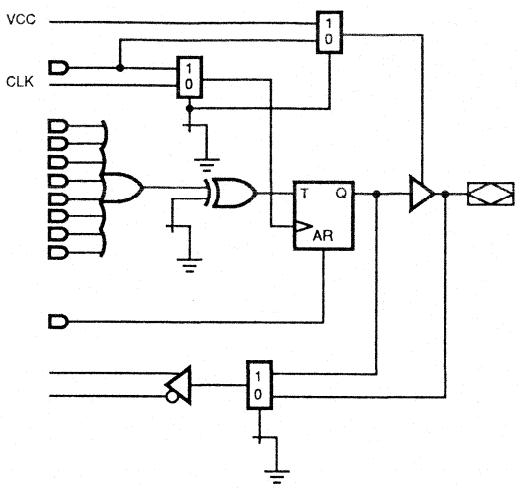
J–K Flip-Flop

The 8 product terms are divided between the J and K inputs. N product terms go to the J input and 8-N product terms go to the K input, where N can range from 0 to 8. Both the J and K inputs to the flip-flop have polarity control via exclusive-OR gates. The J–K flip-flop rules are shown below.

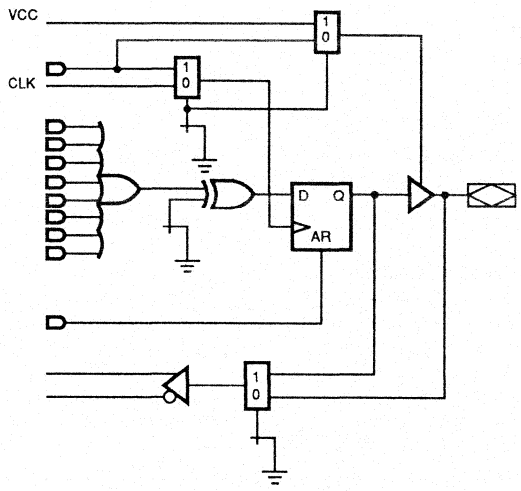
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



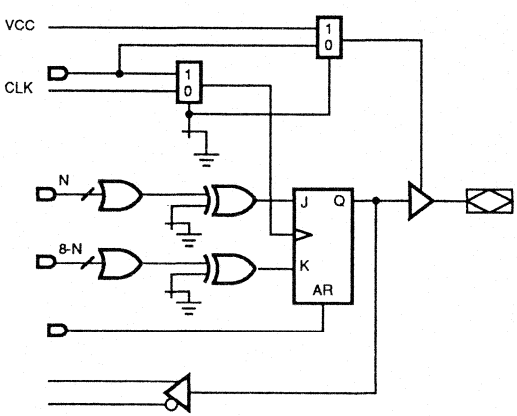
Combinatorial



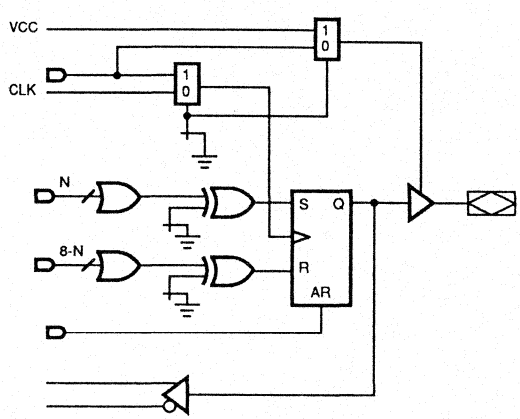
T Register



D Register



J-K Register



S-R Register

12950-004A

Figure 1. Macrocell Configurations

S–R Flip-Flop

The 8 product terms are divided between the S and R inputs. N product terms go to the S input and 8-N product terms go to the R input, where N can range from 0 to 8. Both the S and R inputs to the flip-flop have polarity control via exclusive-OR gates. The S–R flip-flop rules are shown below.

S	R	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Not Allowed	

Asynchronous Reset

All flip-flops have an asynchronous-reset product-term input. When the product term is true, the flip-flop will reset to a logic LOW, regardless of the clock and data inputs.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE610 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW. If combinatorial is selected, the output will be a function of the logic. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE610 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE610 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, preload is disabled and the array is unreadable.

Technology

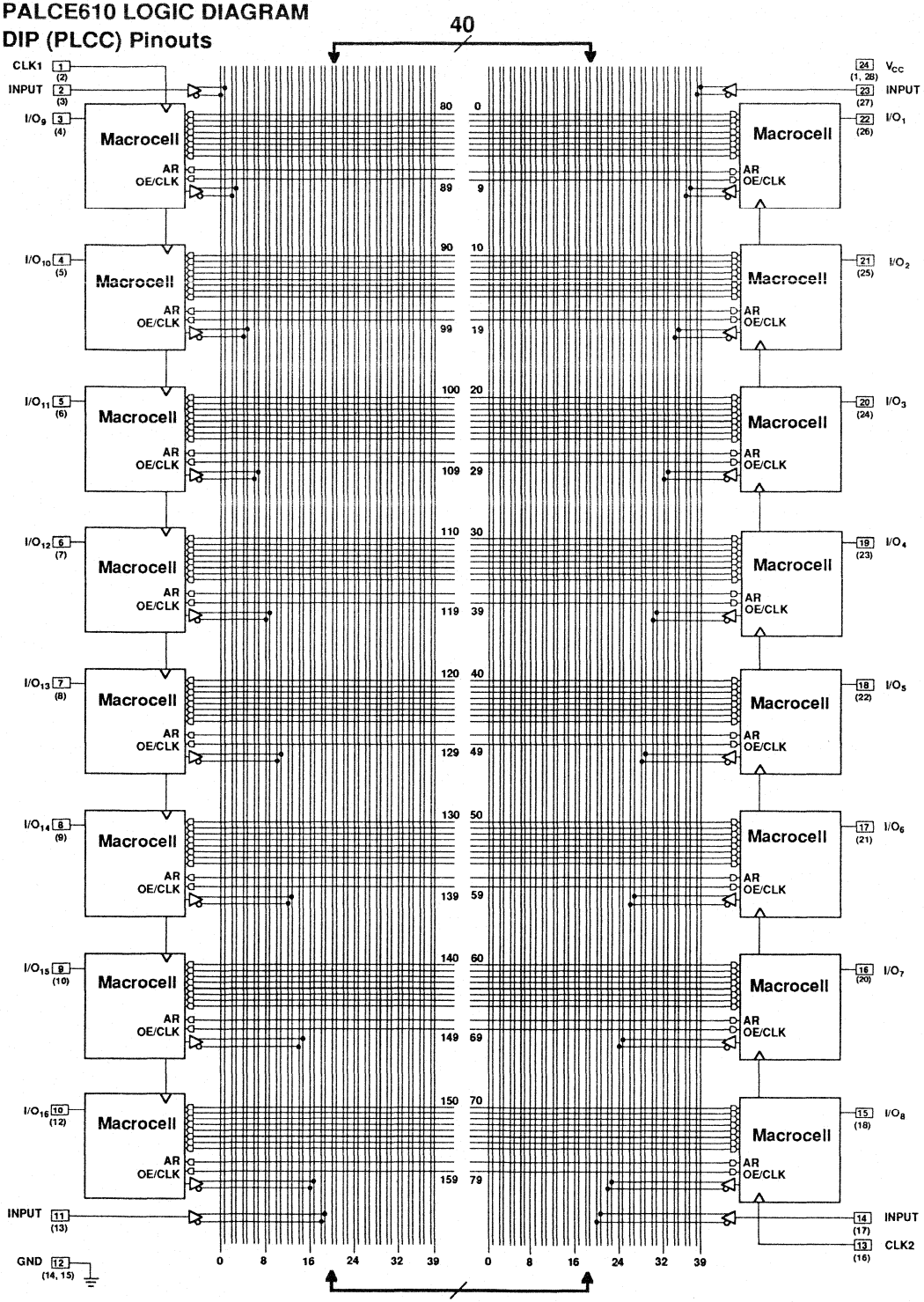
The PALCE610 is manufactured using AMD's advanced Electrically Erasable CMOS process. This technology uses an E^2 cell to replace the fuse link in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the E^2 cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer.

Programming and Erasing

The PALCE610 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PALCE610 may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

PALCE610 LOGIC DIAGRAM
DIP (PLCC) Pinouts



12950-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	I_{OH} = –4.0 mA	2.4		V
			I_{OH} = –2.0 mA	3.84		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

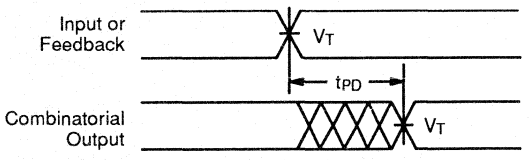
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{CF}	Clock to Feedback (Note 3)				8		10	ns
t_{WL}	Clock Width	LOW		8		10		ns
t_{WH}		HIGH		8		10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	45.5		37		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	50		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 5)			5		8		ns
t_{HA}	Hold Time (Note 5)			9		12		ns
t_{COA}	Clock to Output (Note 5)				17		27	ns
t_{CFA}	Clock to Feedback (Notes 3 and 5)				16		26	ns
t_{WLA}	Clock Width	LOW (Note 5)		8		10		ns
t_{WHA}		HIGH (Note 5)		8		10		ns
f_{MAXA}	Maximum Frequency (Notes 4 and 5)	External Feedback	$1/(t_{SA} + t_{COA})$	45		28.6		MHz
		Internal Feedback	$1/(t_{SA} + t_{CFA})$	48		29		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	62.5		41.6		MHz

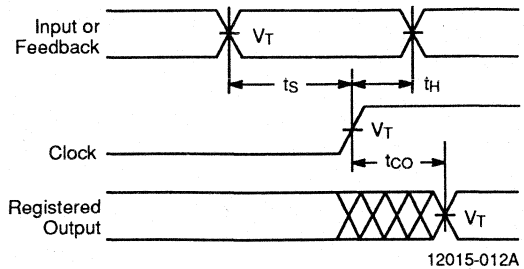
Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are measured using the asynchronous product-term clock.

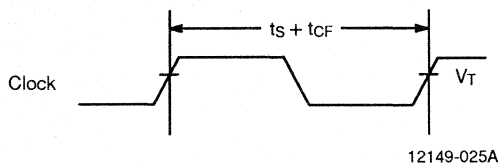
SWITCHING WAVEFORMS



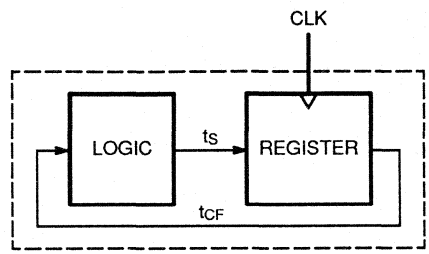
Combinatorial Output

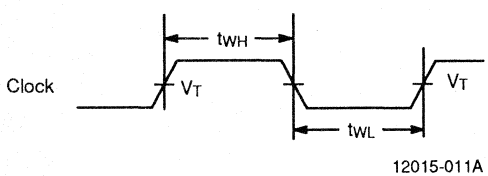


Registered Output

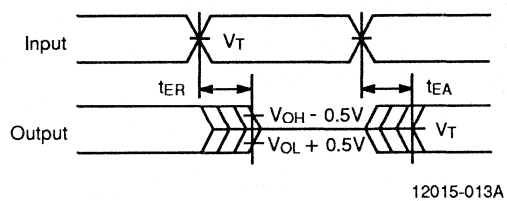


Clock to Feedback (f_{MAX} Internal)
See Path at Right





Clock Width

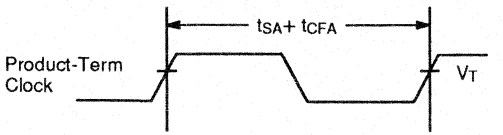


Input to Output Disable/Enable

Notes:

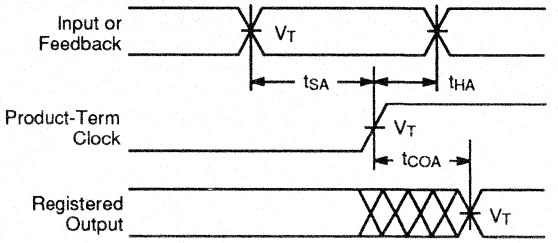
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

SWITCHING WAVEFORMS (Continued)



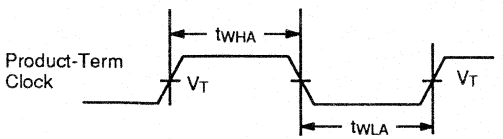
12950-008A

Clock to Feedback Using Product-Term Clock



12950-010A

Registered Output Using Product-Term Clock



12950-009A

Clock Width Using Product-Term Clock

2

Notes:

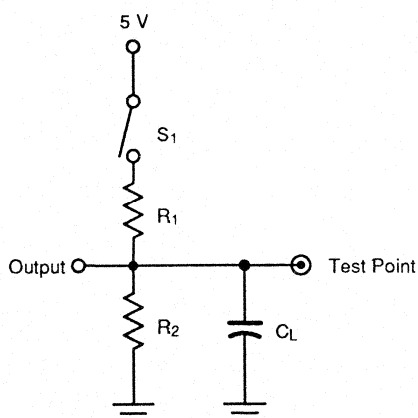
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



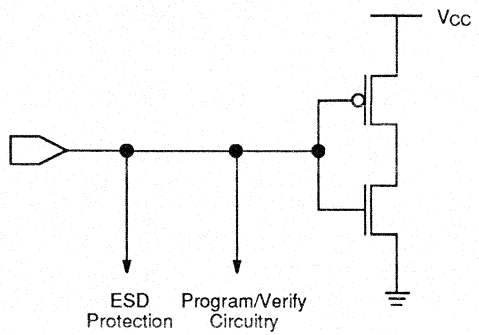
12950-012A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	35 pF	855 Ω	340 Ω	1.5 V
t_{EA}	Z → H : Open Z → L : Closed	35 pF	855 Ω	340 Ω	1.5 V
t_{ER}	H → Z : Open L → Z : Closed	5 pF	855 Ω	340 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

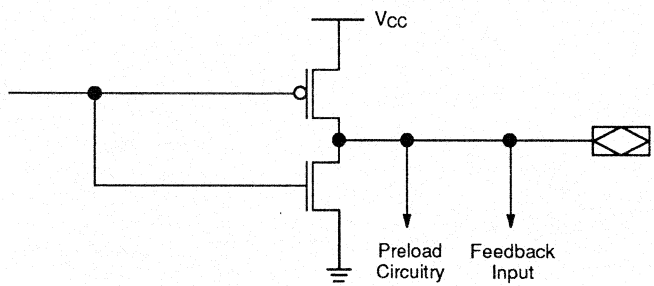
ENDURANCE

Symbol	Parameter Description	Test Conditions	Min.	Unit
t_{DR}	Pattern Data Retention Time	Max. Storage Temperature	10	Years
		Max. Operating Temperature	20	Years
N	Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

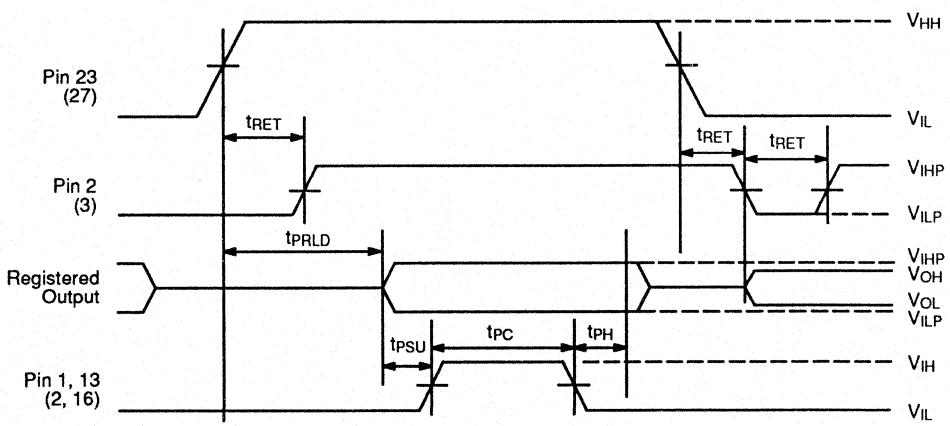
12950-011A

OUTPUT REGISTER PRELOAD

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows. PLCC pin numbers are indicated in parentheses.

1. Set pin 23 (27) to V_{HH}.
2. Set pin 2 (3) to V_{IHP}.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Connect combinatorial output pins to ground.
4. Clock pins 1 and 13 (2 and 16).
5. Remove V_{ILP}/V_{IHP} from all registered outputs.
6. Lower pin 23 (27) to V_{IL}/V_{IH}.
7. Verify V_{OL}/V_{OH} at all registered output pins.
8. Toggle pin 2 (3).
9. Enable per programmed pattern.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-Level Input Voltage	8.5	9.0	9.5	V
V_{ILP}	Low-Level Input Voltage	0	0	0.5	V
V_{IHP}	High-Level Input Voltage	2.4	5.0	5.25	V
V_{CCH}	Power Supply During Preload	4.75	5.0	5.25	V
t_{RET}	Pin 2 (3) Delay Time	200			ns
t_{PRLD}	Preload Input Data Delay	300			ns
t_{PSU}	Preload Data Setup Time	100			ns
t_{PC}	Preload Clock Width	1000	1000		ns
t_{PH}	Preload Data Hold Time	100			ns



12950-006B

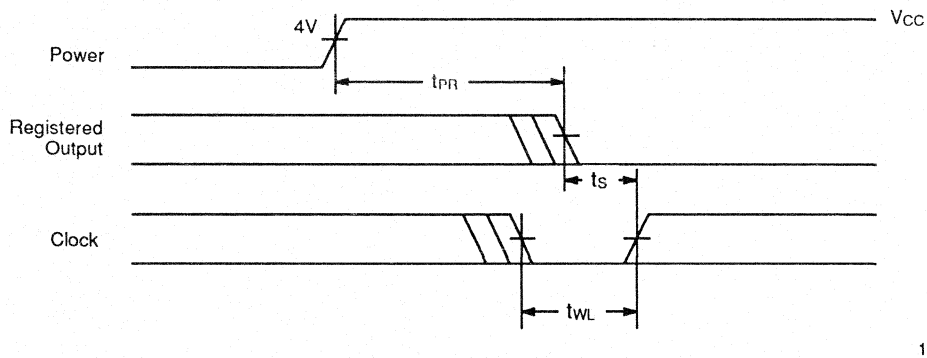
Output Register Preload Waveform

Power-Up Reset

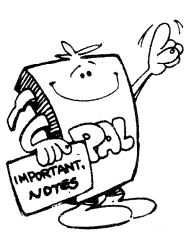
The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

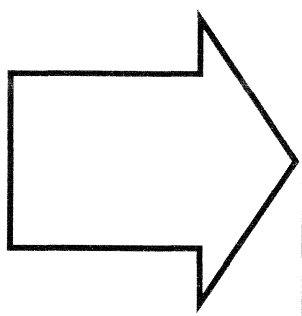
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform


IMPORTANT
NOTES



Sequencer Data Sheets

PLS105-40, PLSCE105H-37

28-Pin TTL/CMOS Programmable Logic Sequencer

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Field-programmable replacement for sequential control logic
- Advanced Mealy state machine/sequencer architecture
- Programmable AND/programmable OR array for flexibility
- Full drive: 24 mA I_{OL}, three-state outputs
- Dedicated hardware features to enhance testability
  - Diagnostic Mode access to buried state register
  - Register Preload and Power-up Preset of all flip-flops
- User-programmable pin for asynchronous flip-flop Preset/Output Enable
- Automatic "Hold" state via S-R flip-flops
- Security bit hides proprietary designs from competitors
- Supported by PALASM®software and standard PLD programmers
- Available in 28-pin plastic SKINNYDIP® and PLCC packages
- Fabricated with high-performance bipolar and electrically erasable CMOS technology

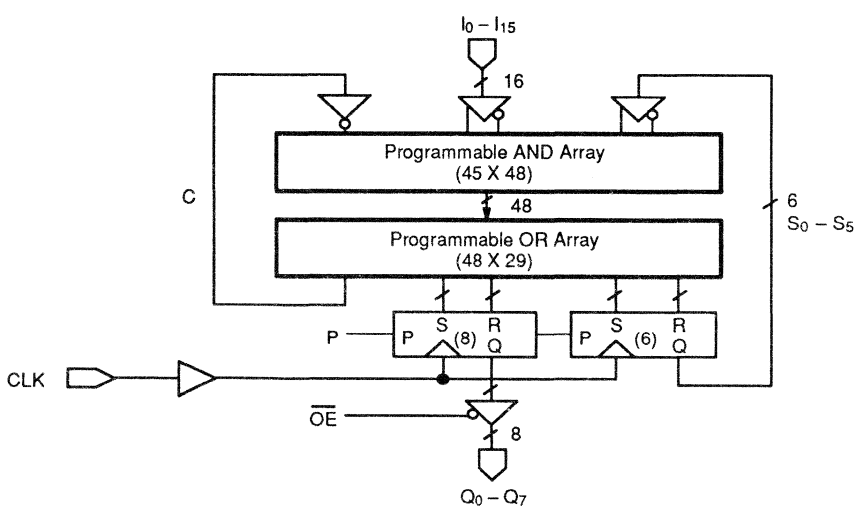
GENERAL DESCRIPTION

The PLS105 is a field-programmable replacement for sequential logic. The device functions as a Mealy state machine with a registered output. The PLS105 utilizes the familiar AND/OR PLA logic structure to implement sum-of-product equations. Both arrays are user-programmable to implement transition terms causing changes in the internal state register or output register. The PLS105-40 device is fabricated in Advanced Micro Devices' advanced oxide-isolated bipolar process. The PLSCE105H-37 device is fabricated in a high-speed, EE CMOS process; it offers significant power improvement (I_{CC} of 100 mA) over competing parts.

The PLS105 device is fully supported by industry-standard CAD tools, including the PALASM design software package. Device programming is accomplished by using standard PLD programmers.

3

BLOCK DIAGRAM

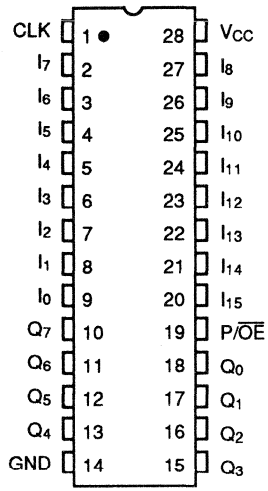


10250-001A

Publication # 10250 Rev. D Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAMS

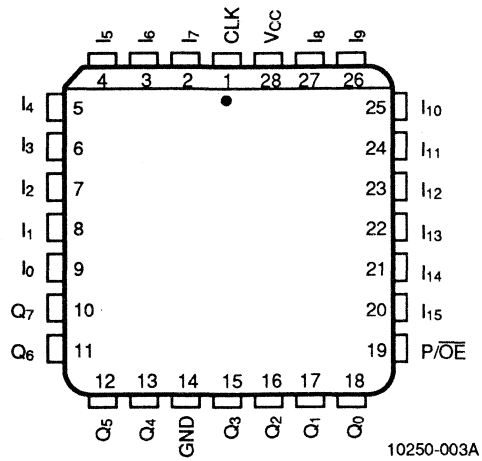
SKINNYDIP



10250-002A

Note: Pin 1 is marked for orientation

PLCC



10250-003A

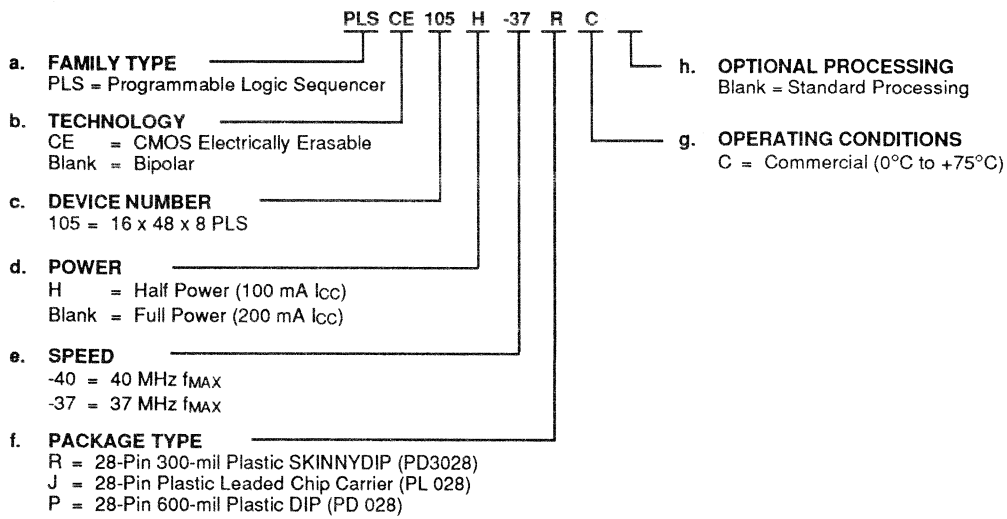
PIN DESIGNATIONS

CLK	Output/state register clock
GND	Ground
I_0-I_{15}	Inputs to AND array
P/$\overline{OE}$	Programmable asynchronous function pin; default is active-high Preset (all registers go HIGH), programmed is active-low Output Enable
Q_0-Q_7	Output register outputs
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Technology**
c. **Device Number**
d. **Power**
e. **Speed**
f. **Package Type**
g. **Operating Conditions**
h. **Optional Processing**



Valid Combinations	
PLSCE105H-37	RC, JC, PC
PLS105-40	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

State Machine Implementation

State machines contain conditional input logic, state memory and output generation logic. The PLS105 device is built around a programmable AND/OR logic array which serves as both conditional input and output generation logic. Forty-eight product or transition terms are found in the AND array. The AND array is driven from several sources: there are sixteen external inputs, six internal feedback signals from the buried state registers, and the complement term.

The OR array drives the output registers, buried state registers, and the complement array term. The PLS105 device offers eight output registers and six buried state registers.

Architectural Details

Part Number	Pins	Inputs	Flip-Flops	Outputs
PLS105	28	16	14	8

State and Output Registers

The state and output registers are both implemented with edge-triggered S-R type flip-flops. If neither input is active, the flip-flop will retain its contents when clocked. This free "hold" state saves product terms. The registers may change only on the LOW-to-HIGH transition of the clock pulse. There are eight output registers and six buried state registers on the device.

Logic Implementation

All transition terms can include True, False, or Don't Care states of the controlling variables. The OR array merges one or more product terms to generate the desired user logic functions for the output and next-state registers. This sharing of OR-terms minimizes the overall logic required to implement complicated control functions.

Complement Array Term

An internal variable (C) known as the complement array term directly implements the "else" logic clause at any state. This often reduces the number of product terms required for a conditional "else" transition . The complement array can also be used for illegal state recovery and designing modulo counters.

Initialization

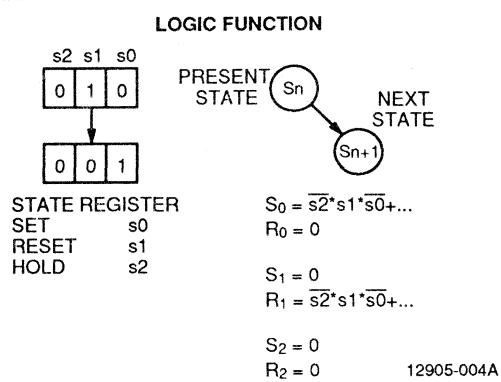
Starting the state machine in a known state is facilitated by power-up preset circuitry which unconditionally loads a "1" into each flip-flop during power-up or by using the asynchronous Preset function. Synchronous transitions to the initial state can be made by having an input be an OR term on all the state register S inputs, and ANDing its complement with all of the R logic terms. Whenever this input is active the machine will synchronously change to the state with all outputs high.

Output Enable

The Preset input can be converted to a three-state Output Enable function by an architecture bit. Expansion to larger control functions can be accommodated by connecting several PLS devices to a control bus and selectively enabling them to each handle a segment of the control algorithm. This user-programmable option is specified as an auxiliary equation in the design file or optionally by use of a keyword.

Typical Operation

The details of device operation may be illustrated by the simple state transition indicated. The state register initially contains 010 and will become 001 after the next clock. For this to occur, state bit 0 must be set, state bit 1 must be reset and state bit 2 must hold its value. The transition term fragments listed produce this result. The S_0 and R_1 product terms detect the bit pattern for the current state (010) and produce a logic one. All other terms evaluate to a zero, producing the transition to state 001.



Typical State Transition

Security Bit

A security bit is provided on the PLS105 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors.

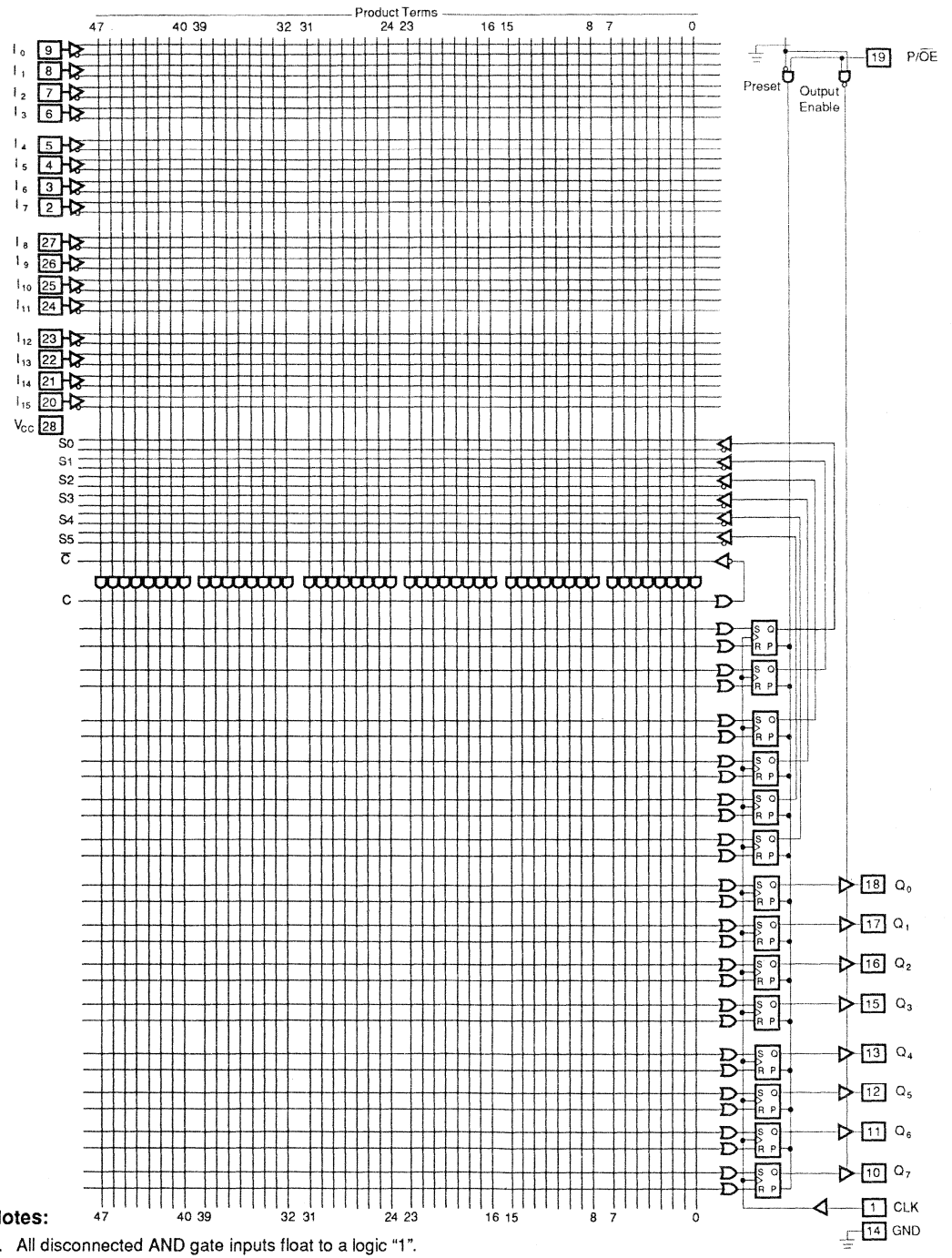
On the PLSCE105, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle. The security bit also prevents preload and observability.

Programming and Erasing

The PLS105 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PLSCE105 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

LOGIC DIAGRAM



Notes:

1. All disconnected AND gate inputs float to a logic "1".
2. All disconnected OR gate inputs float to a logic "0".

10250-004A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 to V_{CC} Max.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		20	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		25	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		20	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		–20	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	CLK, $\overline{OE}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	12	pF
		Others			7	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		15		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array		30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					10	ns
t_{CF}	Clock to Feedback (Note 3)					3	ns
t_{AP}	Asynchronous Preset to Output					15	ns
t_{APW}	Asynchronous Preset Width				10		ns
t_{APR}	Asynchronous Preset Recovery Time				8		ns
t_{WL}	Clock Width	LOW			8		ns
t_{WH}		HIGH			8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	Without Complement Array	$1/(t_S + t_{CO})$	40		MHz
		Internal Feedback		$1/(t_S + t_{CF})$	55.5		MHz
f_{MAXC}		External Feedback	With Complement Array	$1/(t_{SC} + t_{CO})$	25		MHz
		Internal Feedback		$1/(t_{SC} + t_{CF})$	30		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to +7.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		100	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

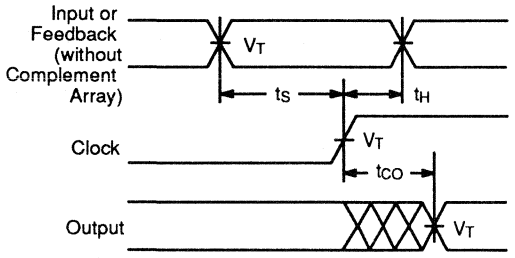
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		17		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array		30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					10	ns
t_{CF}	Clock to Feedback (Note 3)					3	ns
t_{AP}	Asynchronous Preset to Output					15	ns
t_{APW}	Asynchronous Preset Width				10		ns
t_{APR}	Asynchronous Preset Recovery Time				8		ns
t_{WL}	Clock Width	LOW			8		ns
t_{WH}		HIGH			8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	Without Complement Array	$1/(t_S + t_{CO})$	37		MHz
		Internal Feedback		$1/(t_S + t_{CF})$	50		MHz
f_{MAXC}		External Feedback	With Complement Array	$1/(t_{SC} + t_{CO})$	25		MHz
		Internal Feedback		$1/(t_{SC} + t_{CF})$	30		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns

Notes:

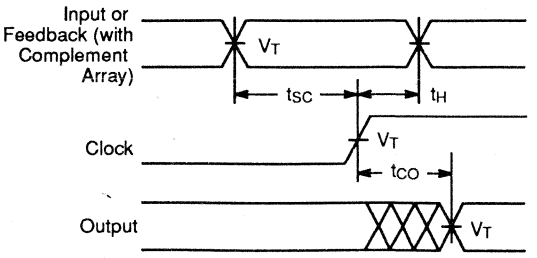
2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



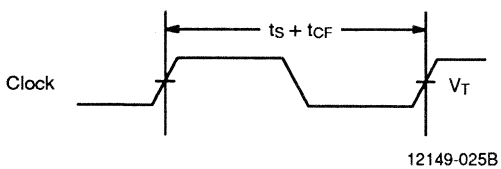
12905-006A

Registered Output (without Complement Array)



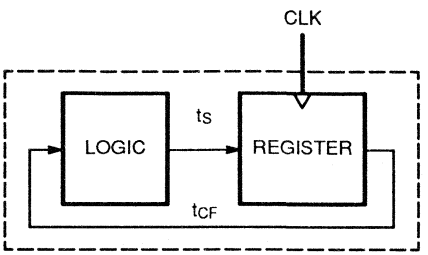
12905-007A

Registered Output (with Complement Array)

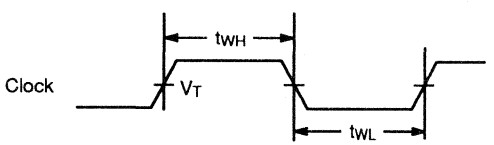


12149-025B

Clock to Feedback (f_{MAX} Internal)
See Path at Right

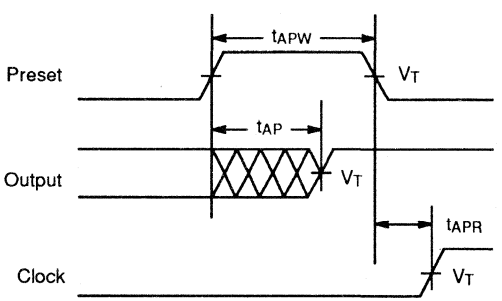


12015-021A



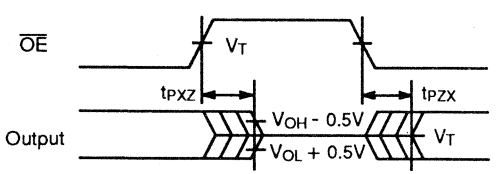
12015-011A

Clock Width



12905-009A

Asynchronous Preset



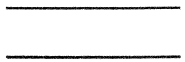
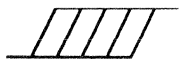
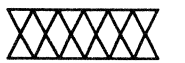
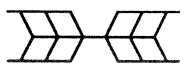
12905-008A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

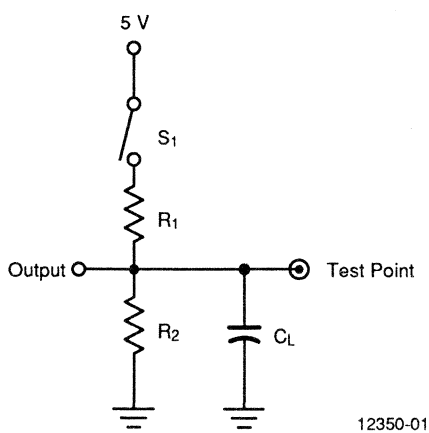
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

3

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} −0.5 V L → Z: V_{OL} +0.5 V

ENDURANCE CHARACTERISTICS

The PLSCE105 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

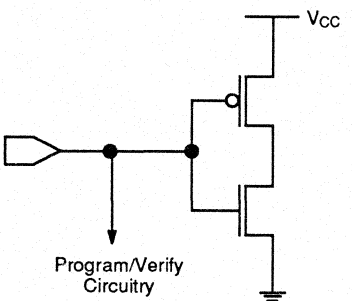
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature (150°C)
		20	Years	Max. Operating Temperature (Military; 125°C)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS

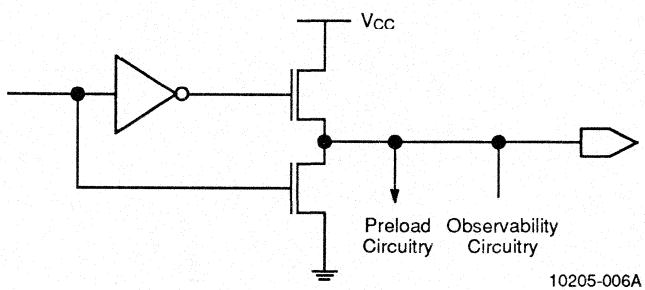
CMOS

Typical Input



10205-012A

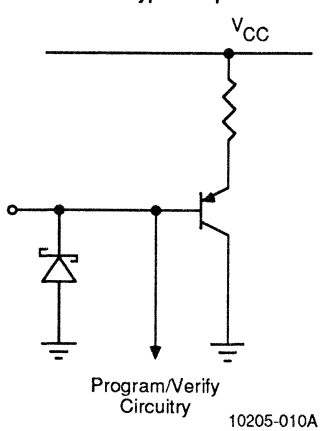
Typical Output



10205-006A

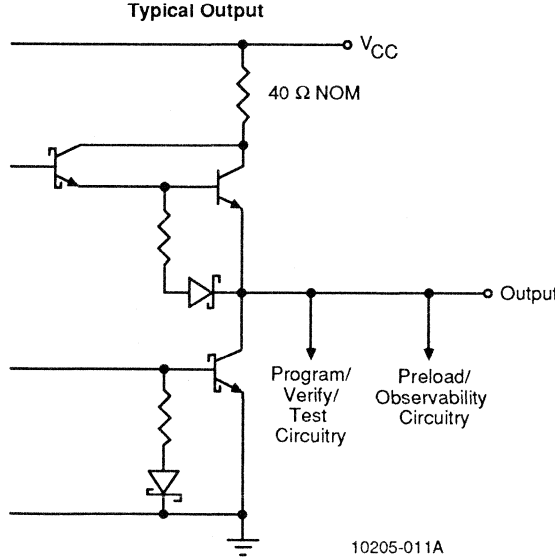
BIPOLAR

Typical Input



10205-010A

Typical Output



10205-011A

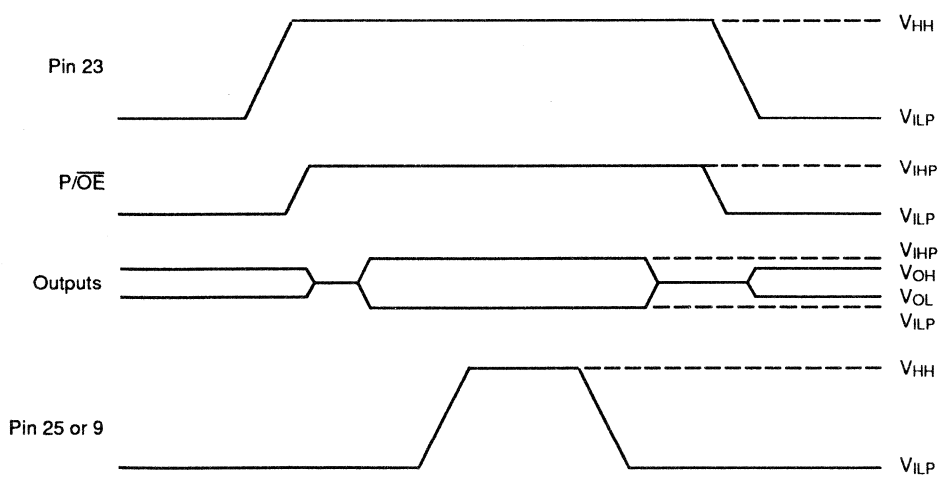
OUTPUT REGISTER PRELOAD (Bipolar Only)

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Raise pin 23 to V_{HH}.
3. Disable output pins by raising P/$\overline{OE}$ to V_{IHP}.
4. Apply V_{IHP}/V_{ILP} as desired to all output pins.
5. Pulse pin 25 or pin 9 from V_{ILP} to V_{HH} and back to V_{ILP}. Pin 25 will preload output registers while pin 9 will preload buried state registers.
6. Remove V_{ILP}/V_{IHP} from output pins.
7. Enable output pins by lowering P/$\overline{OE}$ pin to V_{ILP}.
8. Lower pin 23 to V_{ILP}.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11.5	12	12.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	1			µs
dV_r/dt	V_{HH} Rise Time Slew Rate	10		100	V/µs
dV_f/dt	V_{HH} Fall Time Slew Rate		2.0	3.0	V/µs

Preload Data Q_0–Q_7	Preloaded Register
D_0–D_7	Q_0–Q_7
D_0–D_5,X, X	S_0–S_5



10205-007A

Output Register Preload Waveform

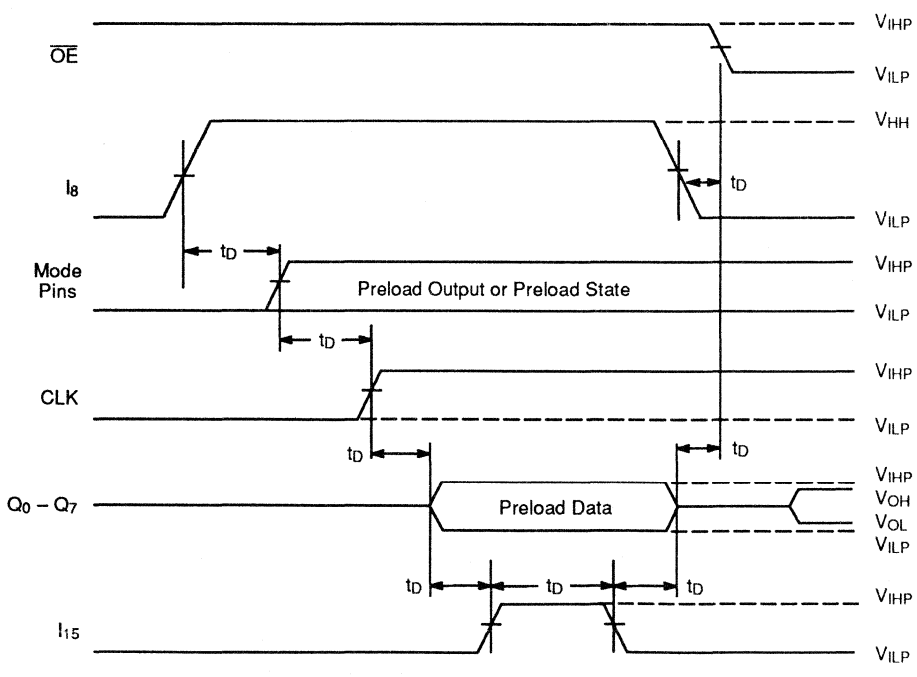
OUTPUT REGISTER PRELOAD (CMOS Only)

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable outputs.
2. With Mode pins LOW raise I_8 to V_{HH}.
3. Use Mode pins to select Preload Output or Preload State.
4. Raise CLK to V_{IHP}.
5. Apply either V_{IHP} or V_{ILP} to all outputs. Use V_{IHP} to preload a LOW in the flip-flop; use V_{ILP} to preload a HIGH in the flop-flop.
6. Pulse I_{15} from V_{ILP} to V_{IHP} to V_{ILP}.
7. Remove preload data from outputs.
8. Lower I_8 to V_{ILP}.
9. Lower $\overline{OE}$ to V_{ILP} to enable the outputs.
10. Verify V_{OL}/V_{OH} at all outputs. To verify state registers, use the observability mode.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	13.25	13.5	13.75	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	4.0	5.0	$V_{CC}+1$	V
t_D	Delay time	1			µs
dV_r/dt	V_{HH} Rise Time Slew Rate	10		100	V/µs
dV_f/dt	V_{HH} Fall Time Slew Rate		2.0	3.0	V/µs

Mode Select Pins				Preload Data	Preloaded Register
I_9	I_{10}	I_{11}	I_{12}	Q_0–Q_7	
0	1	1	0	D_0–D_7	Q_0–Q_7
1	1	1	0	D_0–D_5,X, X	S_0–S_5



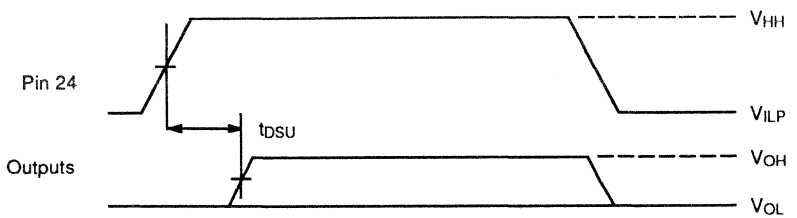
Output Register Preload Waveform

OBSERVABILITY (Bipolar Only)

The observability function allows the state register to be sent to the output pins. This feature aids functional testing of sequential designs by allowing direct observation of the buried state register. The procedure for observability follows.

1. Apply V_{HH} to pin 24.
2. Observe S_0-S_5 on pins Q_0-Q_5.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11.5	12	12.5	V
t_{DSU}	Delay time	250			ns



10205-009A

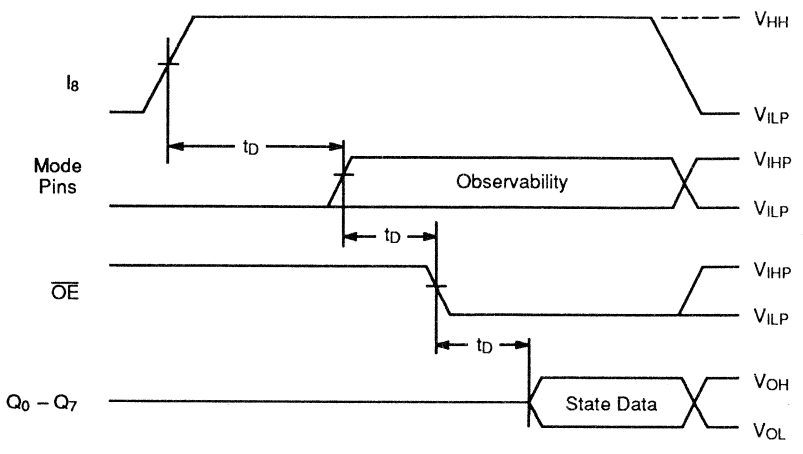
Observability Waveforms

OBSERVABILITY (CMOS Only)

The observability function allows the state register to be sent to the output pins. This feature aids functional testing of sequential designs by allowing direct observation of the buried state register. The procedure for observability follows.

1. Set $\overline{OE}$ to V_{IHP} to disable outputs.
2. With Mode pins LOW raise I_8 to V_{HH}.
3. Use Mode pins to select Observability.
4. Lower $\overline{OE}$ to V_{ILP} to enable the state data to the outputs.
5. Lower I_8 to V_{ILP}.

Mode Select Pins				Output Data
I_9	I_{10}	I_{11}	I_{12}	Q_0–Q_7
0	0	0	1	S_0–S_5, X, X



12905-012A

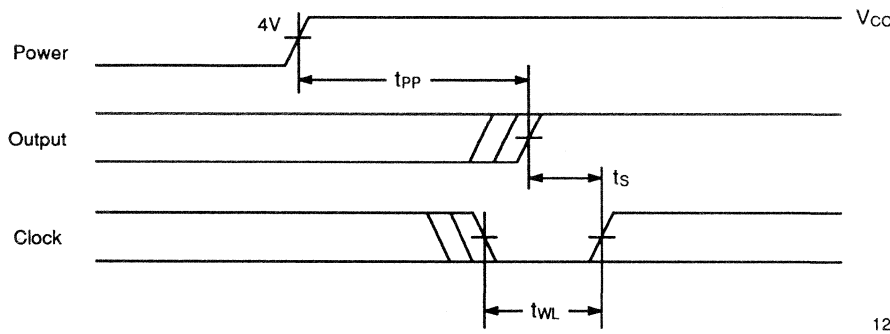
Observability Waveforms

POWER-UP PRESET

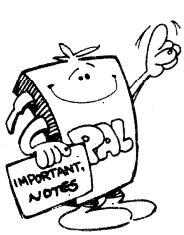
The power-up preset feature ensures that all flip-flops will be preset to HIGH after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up preset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up preset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following preset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PP}	Power-up Preset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Preset Waveform


IMPORTANT
NOTES

PLS167-33, PLSCE167H-33
PLS168-33, PLSCE168H-33

24-Pin TTL/CMOS Programmable Logic Sequencers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Field-programmable replacement for sequential control logic
- Advanced Mealy state machine/sequencer architecture
- Programmable AND/programmable OR array for flexibility
- Full drive: 24 mA I_{OL}, three-state outputs
- Dedicated hardware features to enhance testability
  - Diagnostic Mode access to buried state register
  - Register Preload and Power-up Preset of all flip-flops
- User-programmable pin for asynchronous flip-flop Preset/Output Enable
- Automatic "Hold" state via S-R flip-flops
- Security bit hides proprietary designs from competitors
- Supported by PALASM® software and standard PLD programmers
- Available in 24-pin plastic SKINNYDIP® and 28-pin PLCC packages
- Fabricated with high-performance bipolar and electrically erasable CMOS technology

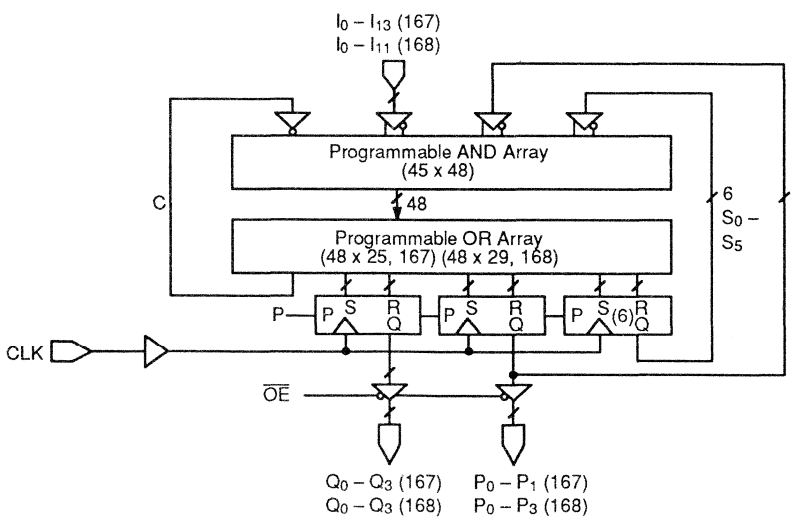
GENERAL DESCRIPTION

The PLS167 and PLS168 are field-programmable replacements for sequential logic. The devices function as Mealy state machines with a registered output. The PLS utilizes the familiar AND/OR PLA logic structure to implement sum-of-product equations. Both arrays are user-programmable to implement transition terms causing changes in the internal state register or output register. The PLS167/8-33 devices are fabricated in Advanced Micro Devices' advanced oxide-isolated bipolar process. The PLSCE167/8H-37 devices are fabricated in a high-speed, EE CMOS process; they offer significant power improvement (I_{CC} of 100 mA) over competing parts.

The PLS devices are fully supported by industry-standard CAD tools, including the PALASM design software package. Device programming is accomplished by using standard PLD programmers.

3

BLOCK DIAGRAM

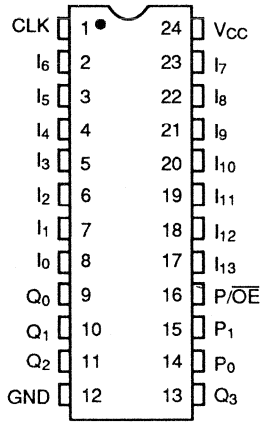


14081-001A

Publication # 14081 Rev. A Amendment /0
Issue Date: January 1990

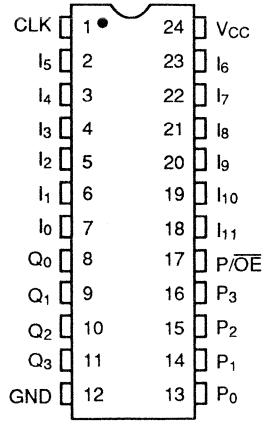
CONNECTION DIAGRAMS

PLS167 SKINNYDIP



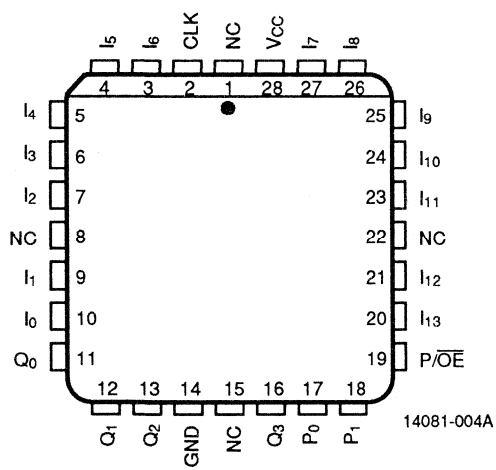
14081-002A

PLS168 SKINNYDIP



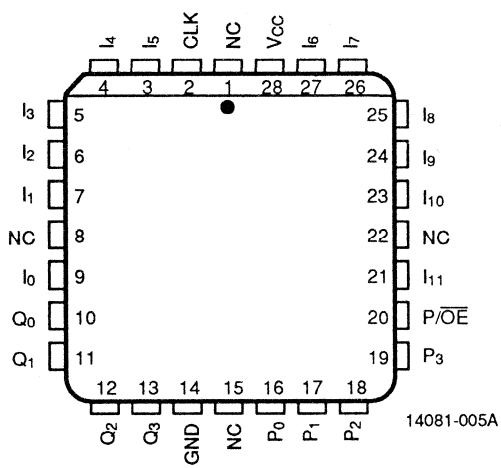
14081-003A

PLCC



14081-004A

PLCC



14081-005A

PIN DESIGNATIONS

CLK	Output/state register clock
GND	Ground
I	Inputs to AND array
P	Programmable output/state register
P/$\overline{OE}$	Programmable asynchronous function pin; default is active-high Preset (all registers go HIGH), programmed is active-low Output Enable
Q	Output register outputs
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products (Bipolar Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Device Number
c. Speed
d. Operating Conditions
e. Package Type
f. Optional Processing

PLS 167 -37 C NS

a. FAMILY TYPE
PLS = Programmable Logic Sequencer

b. DEVICE NUMBER
167 = 14 x 48 x 6 PLS
168 = 12 x 48 x 8 PLS

c. SPEED
-37 = 37 MHz f_{MAX}

f. OPTIONAL PROCESSING
Blank = Standard Processing

e. PACKAGE TYPE
NS = 24-Pin 300-mil Plastic SKINNYDIP (PD3024)
FN = 24-Pin Plastic Leaded Chip Carrier (PL 028)
JS = 24-Pin 300-mil Ceramic SKINNYDIP (CD 3024)

d. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

Valid Combinations	
PLS167-37	CNS, CFN, CJS
PLS168-37	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with MMI logo.

ORDERING INFORMATION
Commercial Products (CMOS Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Device Number
d. Power
e. Speed
f. Package Type
g. Operating Conditions
h. Optional Processing

PLS CE 167 H -33 P C

a. FAMILY TYPE
PLS = Programmable Logic Sequencer

b. TECHNOLOGY
CE = CMOS Electrically Erasable

b. DEVICE NUMBER
167 = 14 x 48 x 6 PLS
168 = 12 x 48 x 8 PLS

d. POWER
H = Half Power (100 mA I_{CC})

e. SPEED
-33 = 33 MHz f_{MAX}

f. PACKAGE TYPE
P = 24-Pin 300-mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
D = 24-Pin 300-mil Ceramic SKINNYDIP (CD3024)

h. OPTIONAL PROCESSING
Blank = Standard Processing

g. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

Valid Combinations	
PLSCE167H-33	PC, JC, DC
PLSCE168H-33	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

State Machine Implementation

State machines contain conditional input logic, state memory and output generation logic. The PLS device is built around a programmable AND/OR logic array which serves as both conditional input and output generation logic. Forty-eight product or transition terms are found in the AND array. The AND array is driven from several sources: there are twelve to fourteen external inputs, six internal feedback signals from the buried state registers, two to four progammable registers, and the complement term.

The OR array drives the output registers, programmable registers, buried state registers, and the complement array term. The PLS device offers six to eight output registers and six buried state registers.

Architectural Details

Part Number	Pins	Inputs	Flip-Flops	Outputs
PLS167	24	14	12	6
PLS168	24	12	14	8

State and Output Registers

The state and output registers are both implemented with edge-triggered S-R type flip-flops. If neither input is active, the flip-flop will retain its contents when clocked. This free "hold" state saves product terms. The registers may change only on the LOW-to-HIGH transition of the clock pulse. There are four output registers, two output/buried registers and six buried state registers on the PLS167 device, and two additional output/buried registers on the PLS168 device.

Logic Implementation

All transition terms can include True, False, or Don't Care states of the controlling variables. The OR array merges one or more product terms to generate the desired user logic functions for the output and next-state registers. This sharing of OR-terms minimizes the overall logic required to implement complicated control functions.

Complement Array Term

An internal variable (C) known as the complement array term directly implements the "else" logic clause at any state. This often reduces the number of product terms required for a conditional "else" transition . The complement array can also be used for illegal state recovery and designing modulo counters.

Initialization

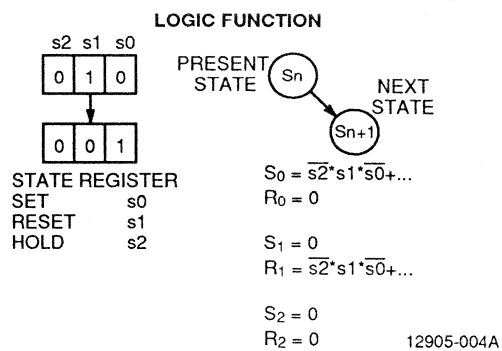
Starting the state machine in a known state is facilitated by power-up preset circuitry which unconditionally loads a "1" into each flip-flop during power-up or by using the asynchronous Preset function. Synchronous transitions to the initial state can be made by having an input be an OR term on all the state register S inputs, and ANDing its complement with all of the R logic terms. Whenever this input is active the machine will synchronously change to the state with all outputs high.

Output Enable

The Preset input can be converted to a three-state Output Enable function by an architecture bit. Expansion to larger control functions can be accommodated by connecting several PLS devices to a control bus and selectively enabling them to each handle a segment of the control algorithm. This user-programmable option is specified as an auxiliary equation in the design file or optionally by use of a keyword.

Typical Operation

The details of device operation may be illustrated by the simple state transition indicated. The state register initially contains 010 and will become 001 after the next clock. For this to occur, state bit 0 must be set, state bit 1 must be reset and state bit 2 must hold its value. The transition term fragments listed produce this result. The S_0 and R_1 product terms detect the bit pattern for the current state (010) and produce a logic one. All other terms evaluate to a zero, producing the transition to state 001.



Typical State Transition

Security Bit

A security bit is provided on the PLS167/8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors.

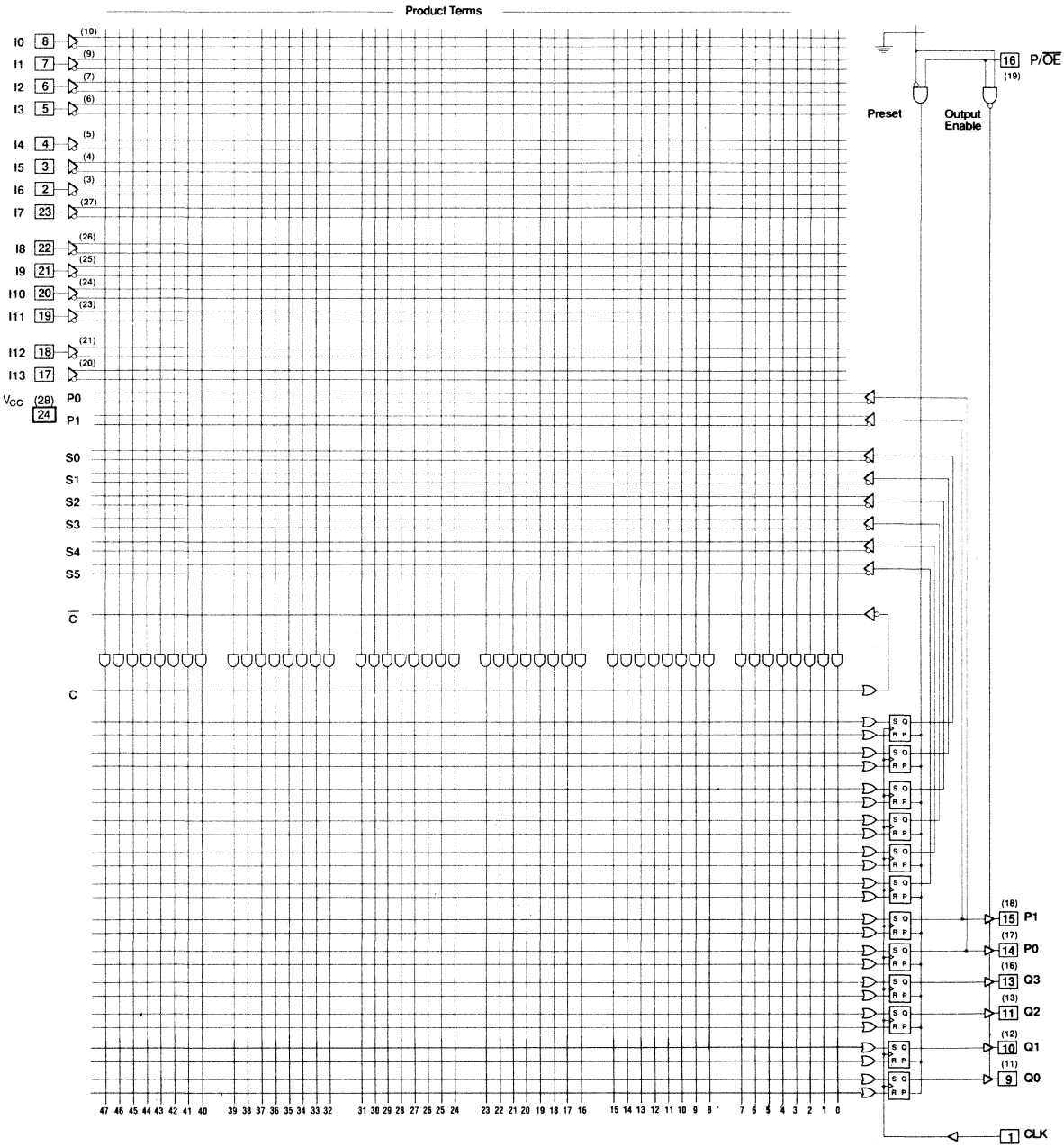
On the PLSCE167/8, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle. The security bit also prevents preload and observability.

Programming and Erasing

The PLS167/8 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PLSCE167/8 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

PLS167 LOGIC DIAGRAM
DIP (PLCC) Pinout

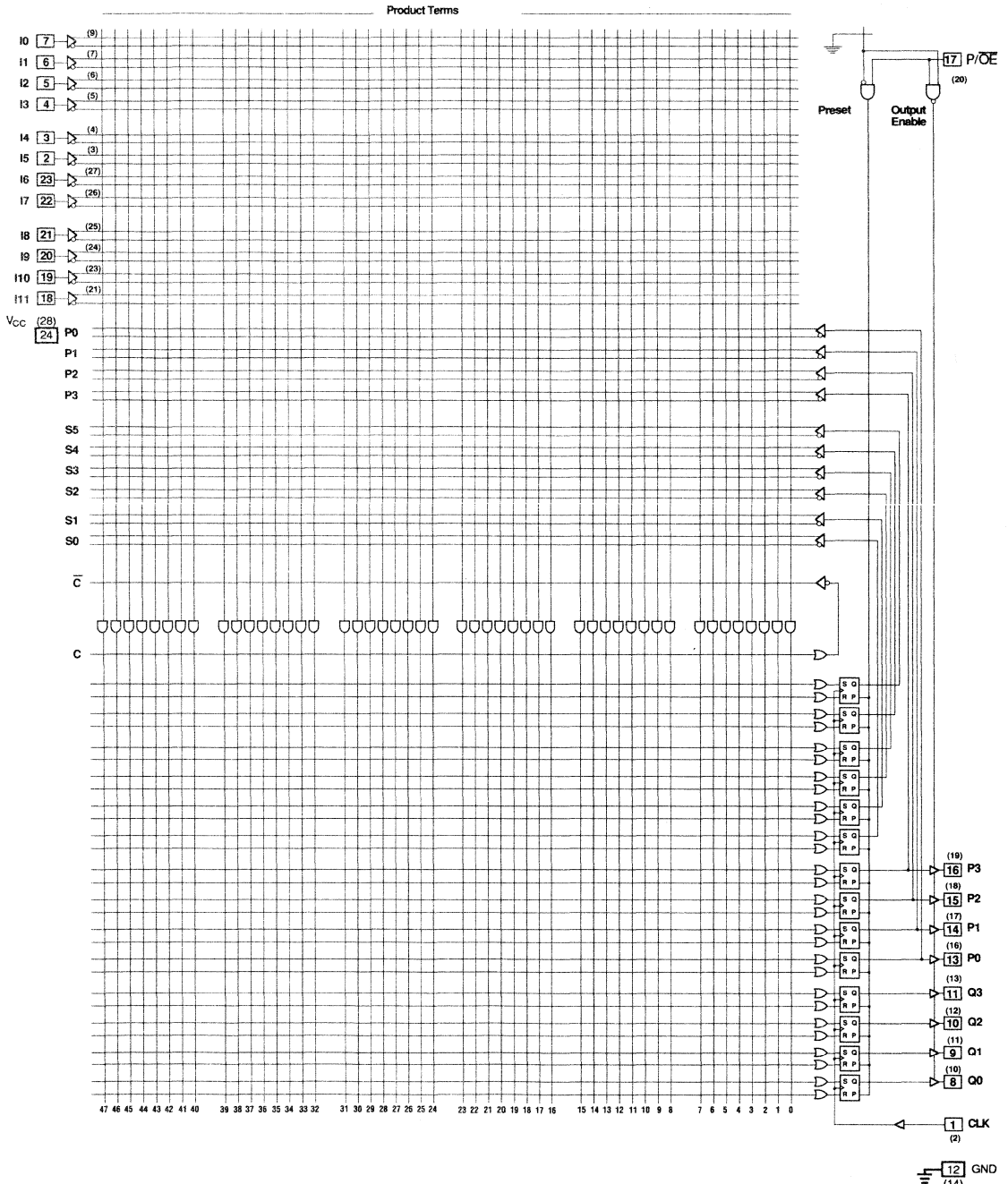


Notes:

1. All disconnected AND gate inputs float to a logic "1."
2. All disconnected OR gate inputs float to a logic "0."

14081-007A

PLS168 LOGIC DIAGRAM
DIP (PLCC) Pinout



Notes:

1. All disconnected AND gate inputs float to a logic "1."
2. All disconnected OR gate inputs float to a logic "0."

14081-007A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to +5.5 V
DC Output Current	+16 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		20	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		25	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		20	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		–20	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		160	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		17		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array		30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					13	ns
t_{AP}	Asynchronous Preset to Output					15	ns
t_{APW}	Asynchronous Preset Width				10		ns
t_{APR}	Asynchronous Preset Recovery Time				8		ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	Without Complement Array	$1/(t_S + t_{CO})$	33		MHz
f_{MAXC}		External Feedback	With Complement Array	$1/(t_{SC} + t_{CO})$	23		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to +7.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		100	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

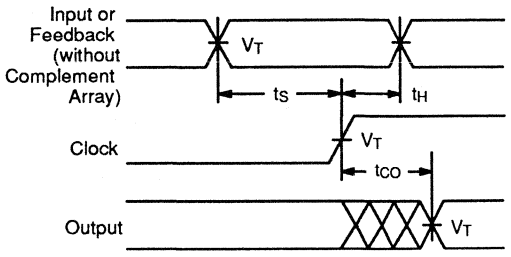
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		17		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array		30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					13	ns
t_{CF}	Clock to Feedback (Note 3)					10	ns
t_{AP}	Asynchronous Preset to Output					15	ns
t_{APW}	Asynchronous Preset Width				10		ns
t_{APR}	Asynchronous Preset Recovery Time				8		ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	Without Complement Array	$1/(t_S + t_{CO})$	33		MHz
		Internal Feedback		$1/(t_S + t_{CF})$	37		MHz
f_{MAXC}		External Feedback	With Complement Array	$1/(t_{SC} + t_{CO})$	23		MHz
		Internal Feedback		$1/(t_{SC} + t_{CF})$	25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns

Notes:

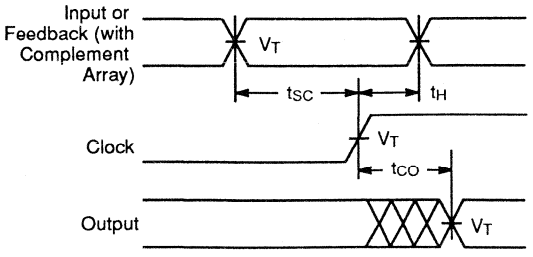
2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



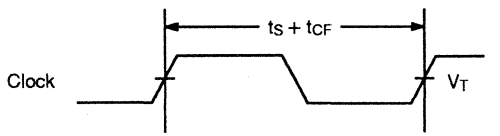
12905-006A

Registered Output (without Complement Array)



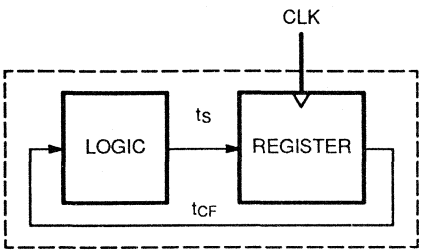
12905-007A

Registered Output (with Complement Array)

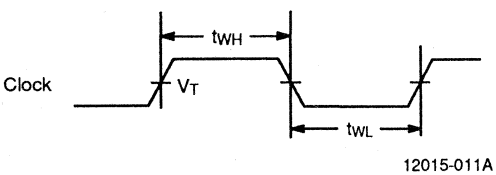


12149-025B

Clock to Feedback (f_{MAX} Internal) See Path at Right

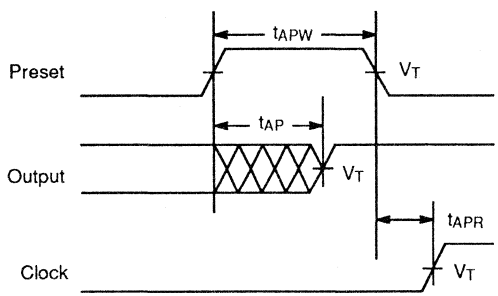


12015-021A



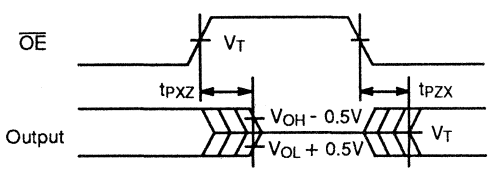
12015-011A

Clock Width



12905-009A

Asynchronous Preset



12905-008A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

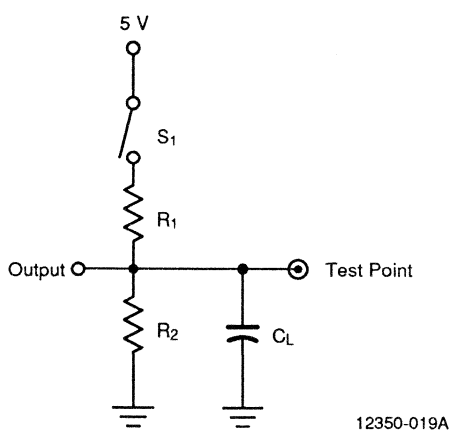
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

3

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} −0.5 V L → Z: V_{OL} +0.5 V

ENDURANCE CHARACTERISTICS

The PLSCE167/8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

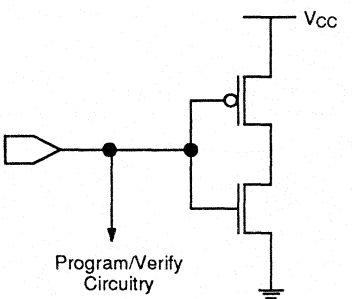
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (125°C)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS

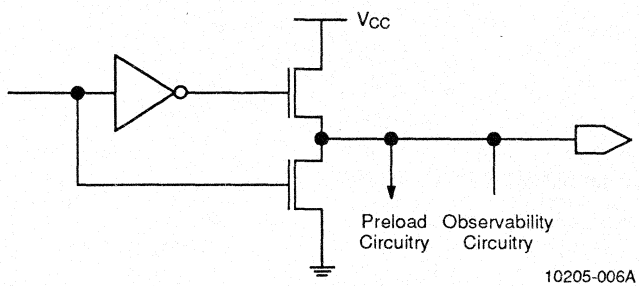
CMOS

Typical Input



10205-012A

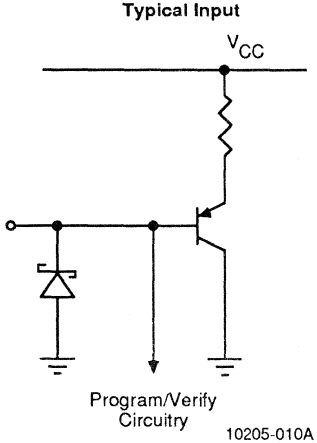
Typical Output



10205-006A

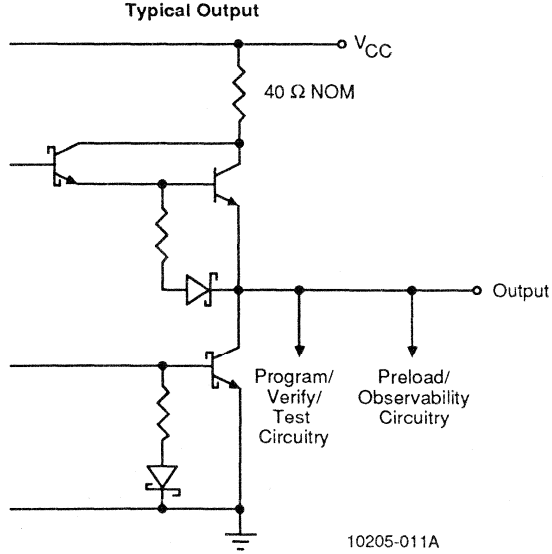
BIPOLAR

Typical Input



10205-010A

Typical Output



10205-011A

OUTPUT REGISTER PRELOAD (Bipolar Only)

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Raise pin 19 to V_{HH}.
3. Disable output pins by raising P/$\overline{OE}$ pin to V_{IHP}.
4. Apply V_{IHP}/V_{ILP} as desired to all output pins.
5. Pulse pin 21 or pin 8/7 from V_{ILP} to V_{HH} and back to V_{ILP}. Pin 21 will preload output registers while pin 8/7(167/168) will preload buried state registers.
6. Remove V_{ILP}/V_{IHP} from output pins.
7. Enable output pins by lowering P/$\overline{OE}$ pin to V_{ILP}.
8. Lower pin 19 to V_{ILP}.

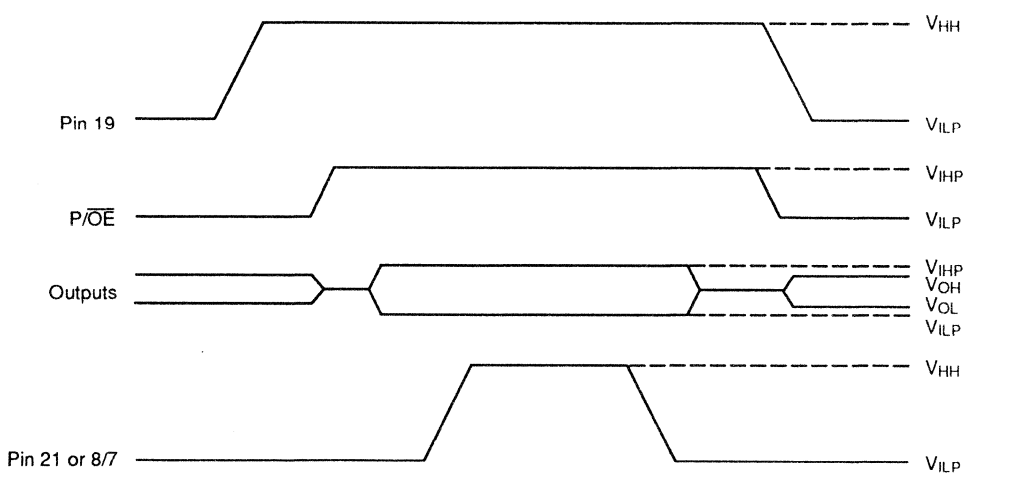
Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11.5	12	12.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	1			µs
dV_r/dt	V_{HH} Rise Time Slew Rate	10		100	V/µs
dV_f/dt	V_{HH} Fall Time Slew Rate		2.0	3.0	V/µs

PLS167

Preload Data	Pulse	Preloaded Register
Q_0–Q_3, P_0–P_1		
D_0–D_5	Pin 21	Q_0–Q_3, P_0–P_1
D_0–D_5	Pin 8	S_0–S_5

PLS168

Preload Data	Pulse	Preloaded Register
Q_0–Q_3, P_0–P_3		
D_0–D_7	Pin 21	Q_0–Q_3, P_0–P_3
X, X, D_2–D_7	Pin 7	S_0–S_5



Output Register Preload Waveform

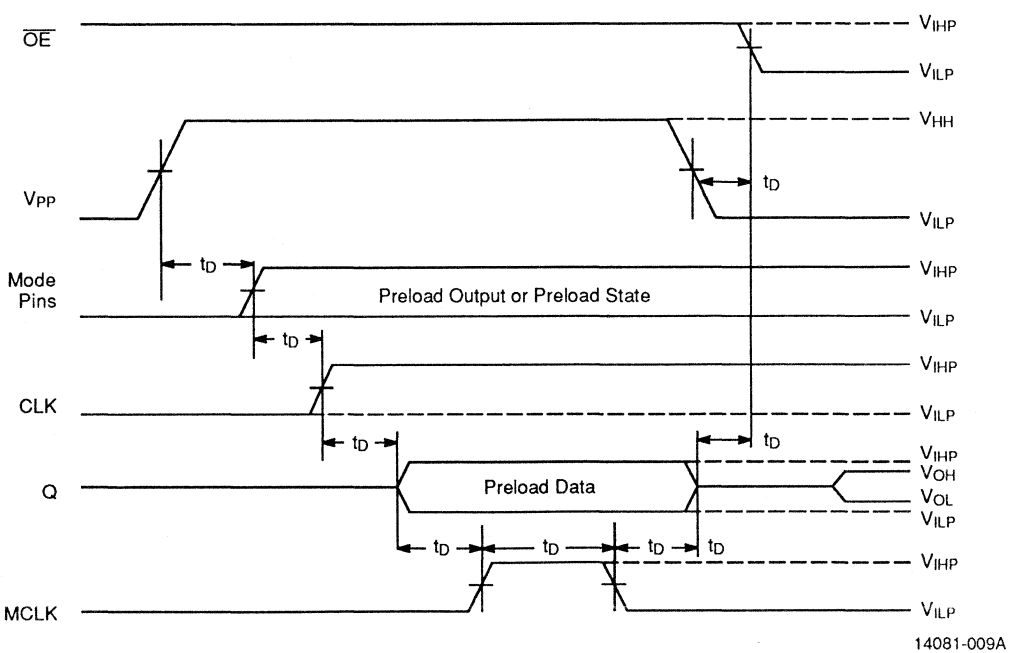
OUTPUT REGISTER PRELOAD (CMOS Only)

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable outputs.
2. With Mode pins LOW raise V_{PP} to V_{HH}.
3. Use Mode pins to select Preload Output or Preload State.
4. Raise CLK to V_{IHP}.
5. Apply either V_{IHP} or V_{ILP} to all outputs. Use V_{IHP} to preload a LOW in the flip-flop; use V_{ILP} to preload a HIGH in the flop-flop.
6. Pulse MCLK from V_{ILP} to V_{IHP} to V_{ILP}.
7. Remove preload data from outputs.
8. Lower V_{PP} to V_{ILP}.
9. Lower $\overline{OE}$ to V_{ILP} to enable the outputs.
10. Verify V_{OL}/V_{OH} at all outputs. To verify state registers, use the observability mode.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	13.25	13.5	13.75	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	4.0	5.0	$V_{CC}+1$	V
t_D	Delay time	1			µs
dV_r/dt	V_{HH} Rise Time Slew Rate	10		100	V/µs
dV_f/dt	V_{HH} Fall Time Slew Rate		2.0	3.0	V/µs

Mode Select Pins			
MD_0	MD_1	MD_2	MD_3
0	1	1	0
1	1	1	0



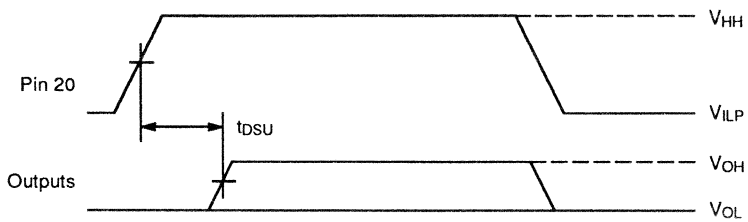
Output Register Preload Waveform

OBSERVABILITY (Bipolar Only)

The observability function allows the state register to be sent to the output pins. This feature aids functional testing of sequential designs by allowing direct observation of the buried state register. The procedure for observability follows.

1. Apply V_{HH} to pin 20.
2. Observe S_0–S_5 on pins Q_0–Q_3, P_0–P_1 (167) or Q_2–Q_3, P_0–P_3 (168).

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11.5	12	12.5	V
t_{DSU}	Delay time	250			ns



14081-010A

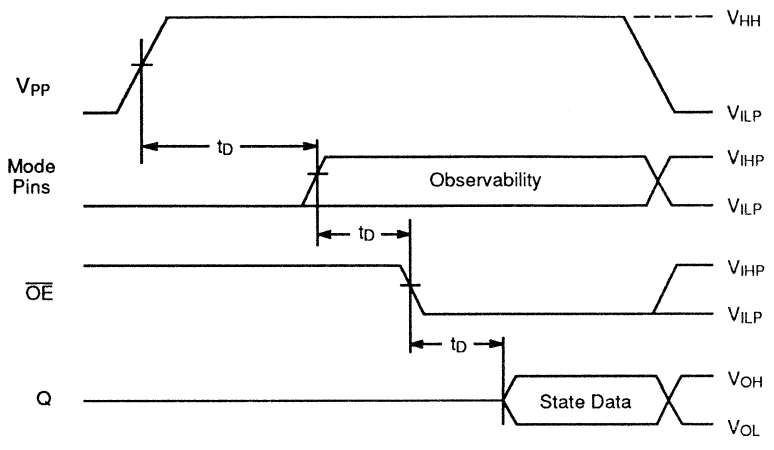
Observability Waveforms

OBSERVABILITY (CMOS Only)

The observability function allows the state register to be sent to the output pins. This feature aids functional testing of sequential designs by allowing direct observation of the buried state register. The procedure for observability follows.

1. Set $\overline{OE}$ to V_{IHP} to disable outputs.
2. With Mode pins LOW raise V_{PP} to V_{HH}.
3. Use Mode pins to select Observability.
4. Lower $\overline{OE}$ to V_{ILP} to enable the state data to the outputs.
5. Lower V_{PP} to V_{ILP}.

Mode Select Pins			
MD_0	MD_1	MD_2	MD_3
0	0	0	1



14081-011A

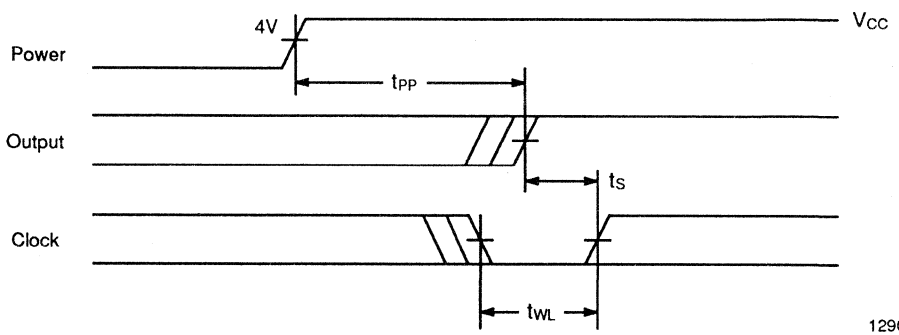
Observability Waveforms

POWER-UP PRESET

The power-up preset feature ensures that all flip-flops will be preset to HIGH after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up preset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up preset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following preset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PP}	Power-up Preset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Preset Waveform

PLS30S16-40

28-Pin Universal Programmable Logic Sequencer

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Field-programmable replacement for sequential logic**
  - Eases design and speeds time to market
- **Advanced Mealy state machine architecture**
  - Programmable AND and OR arrays for increased logic capability
  - S-R flip-flops provide automatic hold state
- **64 product terms and 12 state registers allow many states**
- **Up to 12 registered outputs or up to 8 combinatorial outputs**
- **17 inputs including four with synchronizing D-type flip-flops**
- **Two clock inputs and two complement arrays for dual state machines in one device**
- **Enhanced testability**
  - Observability of all buried registers
  - Register Preload of all flip-flops
  - On-chip test array for 100% testability
- **Supported by PALASM® software and standard PLD programmers**
- **Available in 28-pin plastic SKINNYDIP® and PLCC packages**
- **High performance at 40 MHz f_{MAX}**

GENERAL DESCRIPTION

The PLS30S16 is an advanced 28-pin field-programmable logic sequencer (PLS). It is a flexible superset of other 28-pin PLS devices with additional logic and additional flexibility. The device functions as a Mealy state machine with either registered or combinatorial outputs. The PLS30S16 utilizes the familiar AND/OR PLA logic structure (17x71x12) to implement Boolean sum-of-product equations.

Up to 17 external inputs drive the AND array, four of which may be registered. Both AND and OR logic arrays are programmable, eliminating redundant terms and restrictions on terms per output. The AND array creates transition terms and the OR array merges terms for state transitions and output logic. Two complement array logic terms are provided to create multiple-pass logic functions. These terms are commonly used to generate the "else" branches for undecoded default transitions.

The PLS30S16 has 16 S-R flip-flops, 12 of which drive the AND array as state bits. Four of these flip-flops are part of dual-feedback I/O macrocells; four other macrocells function as either registered or combinatorial outputs. The other two banks of four flip-flops act as dedicated buried register state bits and registered outputs. The clock function is individually selectable for the four banks of flip-flops. Up to 12 outputs can be configured, all of which have three-state buffers controlled by product terms.

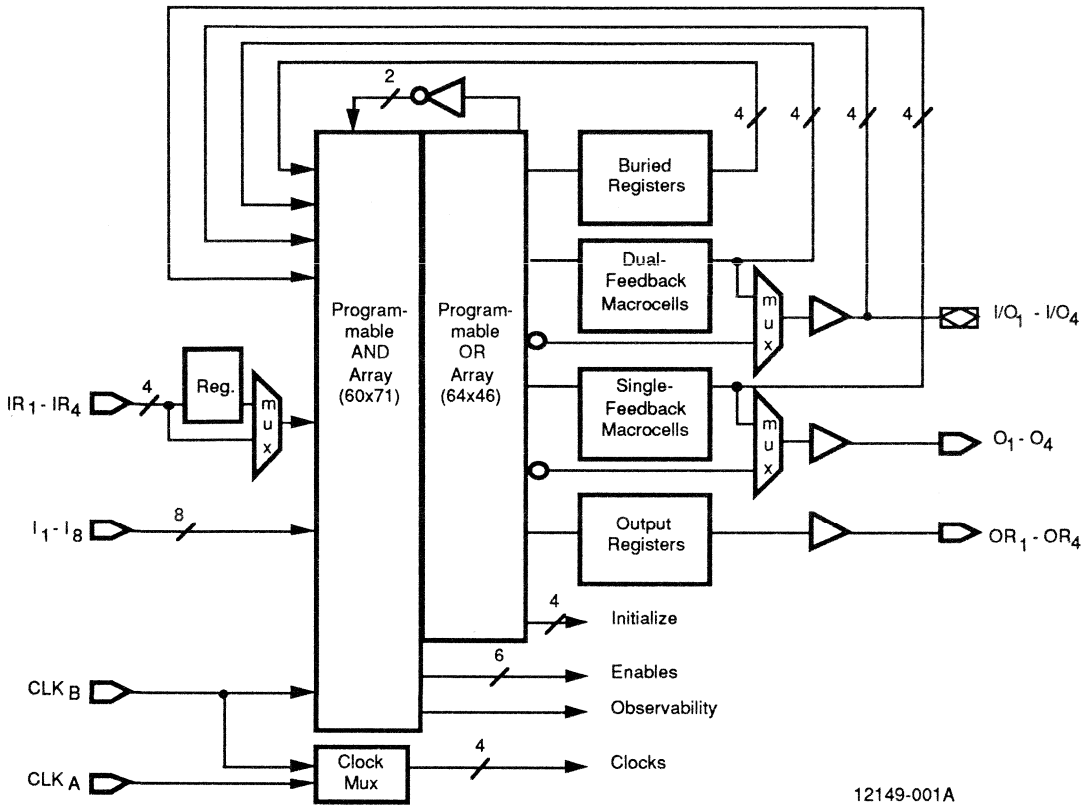
The PLS30S16 utilizes AMD's high-speed bipolar process for the best performance. The entire PLS family is fully supported by PALASM design software, enabling verification of the design and conversion to the JEDEC standard programming format. The device is supported by industry-standard programming and development tools.

AMD PLS FAMILY

Part Number	Pins	Inputs	Product Terms	State Registers	Output Registers	f_{MAX}
PLS30S16	28	12-17	64	4-12	4-12	40
PLS105	28	16	48	6	8	40
PLS167	24	14	48	6-8	4-6	33
PLS168	24	12	48	6-10	4-8	33

Publication # 12149 Rev. A Amendment /0
Issue Date: January 1990

BLOCK DIAGRAM

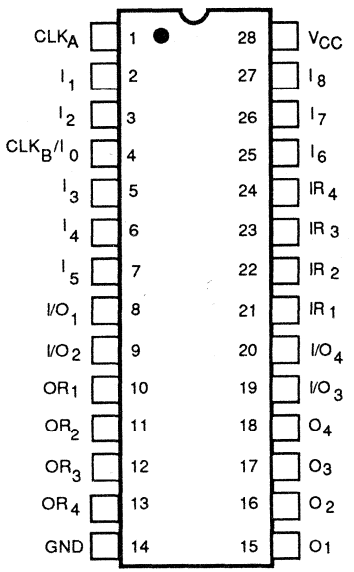


Internal Signals

QI/O_1–QI/O_4	Registered feedback associated with I/O_1–I/O_4
QO_1–QO_4	Registered feedback associated with O_1–O_4
Q_1–Q_4	Buried registers
CLK_0	Clock for IR_1–IR_4
CLK_1	Clock for QI/O_1–QI/O_4
CLK_2	Clock for OR_1–OR_4 and Q_1–Q_4
C_0–C_1	Complement array sum terms
OBS	Observability product term
OE_1–OE_4	Output enable product terms for I/O_1–I/O_4
OE_O	Output enable product term for O_1–O_4
OE_R	Output enable product term for OR_1–OR_4

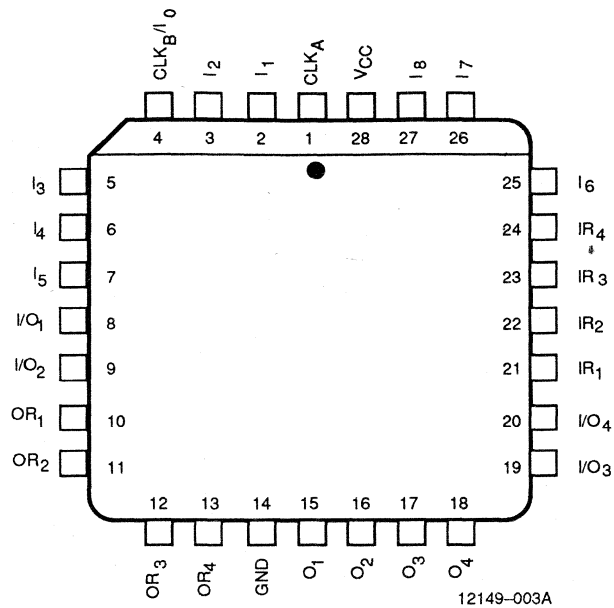
CONNECTION DIAGRAMS
Top View

SKINNYDIP®



12149–002A

PLCC



12149–003A

Note: Pin 1 is marked for orientation

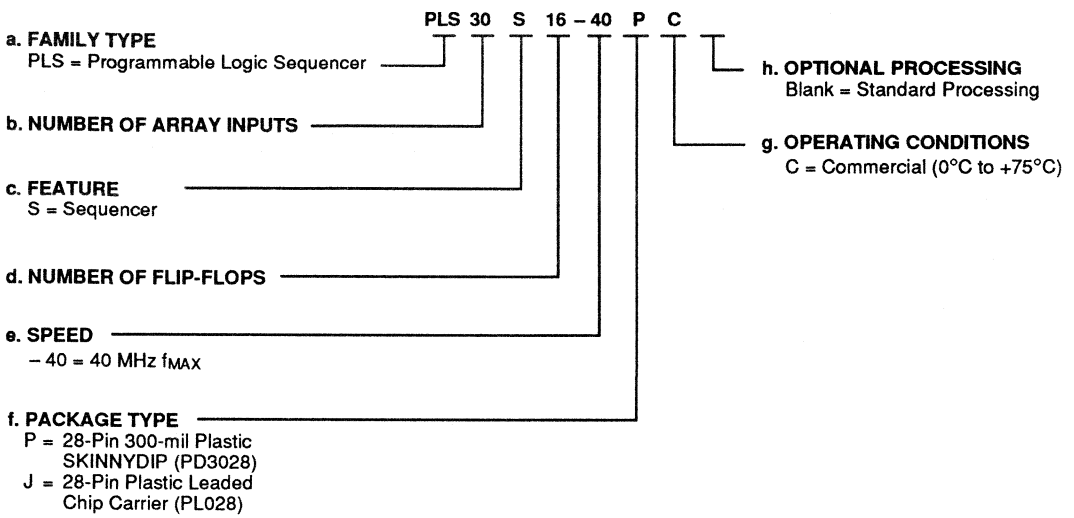
PIN DESIGNATIONS

I_1 - I_8	Inputs
IR_1-IR_4	Registered inputs with bypass
I/O_1-I/O_4	Registered or combinatorial I/O with dual feedback
O_1-O_4	Registered or combinatorial outputs
OR_1-OR_4	Registered outputs
CLK_A	Clock input; clock for O_1-O_4
CLK_B/I_0	Clock and/or array input
V_{CC}	Supply Voltage
GND	Ground

ORDERING INFORMATION
Commercial Products

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Feature
d. Number of Flip-flops
e. Speed
f. Package Type
g. Operating Conditions
h. Optional Processing



Valid Combinations	
PLS30S16-40	PC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

State Machine Implementation

State machines contain conditional input logic, state memory and output generation logic. The PLS30S16 is built around a programmable AND/OR logic array which serves as both conditional input and output generation logic. 64 product or transition terms are found in the AND array. It is driven from several sources: 17 external inputs, 12 internal feedbacks from the state registers, and 2 complement terms.

All transition terms can include True, False, or Don't Care conditions of the controlling variables. The OR array merges one or more product terms to generate the desired logic functions for the output and state registers. This sharing of OR terms minimizes the overall logic required to implement complicated control functions. The two internal variables $C_0 - C_1$ are known as the complement array terms, and can directly implement a default branch (the "else" branch) from any state. Two complement arrays allow the integration of two independent state machines.

Inputs

The device inputs include the eight dedicated inputs I_1–I_8, optionally registered inputs IR_1–IR_4, CLK_B, and I/O pins I/O_1–I/O_4. All signals are complemented on-chip, allowing either true or complement versions in equations. If any input pin is not used, it should be tied to GND or V_{CC}.

Inputs IR_1–IR_4 have synchronizing D-type flip-flops to capture transient signals or eliminate potential register setup time violations. The flip-flop is a simple D-type that is loaded on the rising edge of CLK_0 (Figure 1). CLK_0 can be either polarity of either clock input, allowing the input register to be clocked on the opposite phase of the output register clock, or independently of the output register. Each flip-flop can be individually bypassed by programming the multiplexer fuse (SI).

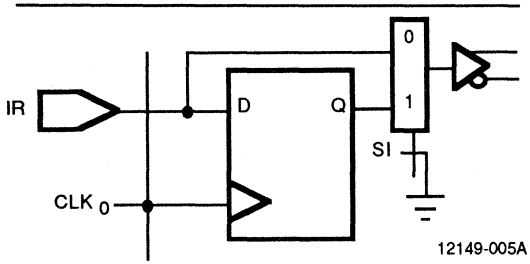


Figure 1a. Input Register

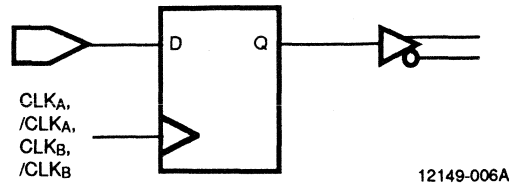


Figure 1b. Input Register Configuration; Registered Input (SI = 1)

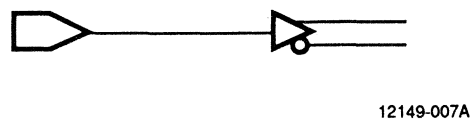


Figure 1c. Input Register Configuration; Combinatorial Input (SI = 0)

CLK_B can be used as a standard array input if not needed as a clock input. If CLK_B is to be used both as a logic input and as a clock, great care should be taken to avoid setup time violations.

S-R Flip-flops

The 16 state and output registers are implemented with rising-edge triggered, clocked S-R type flip-flops (Figure 2). The flip-flop goes HIGH after the clock edge if the S (Set) input is HIGH, and LOW if the R (Reset) input is HIGH. If neither input is HIGH, the flip-flop will retain its contents when clocked. This free "hold" state saves product terms. S and R may not be HIGH at the same time. The registers may change only on the LOW-to-HIGH transition of the clock input, which depends on the selection of the clock source.

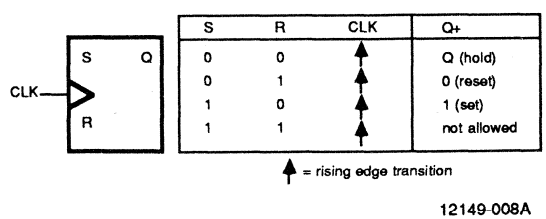


Figure 2. S-R Flip-flop Logic

Typical Operation

The details of device operation may be illustrated by the simple state transition indicated in Figure 3. The state register initially contains 010 and will become 001 after the next clock. In order for this to occur, state bit Q0 must be set, state bit Q1 must be reset and state bit Q2 must hold its value. For the S-R type flip-flops, the equation fragments listed (in PALASM syntax) produce this result. The Q0.S and Q1.R product terms detect the bit pattern for the current state (010) and produce a logic one, setting Q0 and resetting Q1. All other terms evaluate to a zero, producing the transition to state 001.

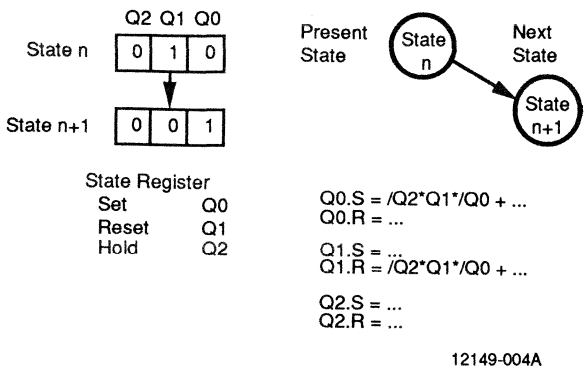


Figure 3. Typical State Transition

Buried Registers

Q_1–Q_4 are the four dedicated buried registers (Figure 4). They can be used as state bits, storing the current state and using feedback to the AND array to help determine the next state. All four flip-flops are clocked by CLK_2, which can be either CLK_A or CLK_B according to the Clock Mux.

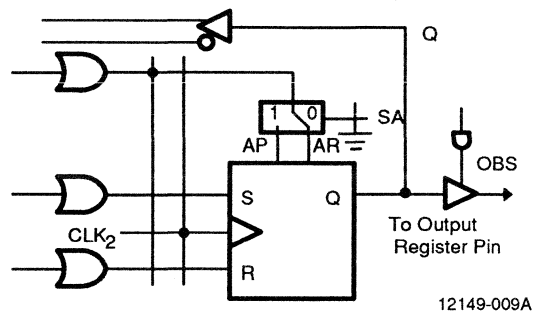


Figure 4. Buried Register

The buried registers Q_1–Q_4 can be preloaded to any value (see "Register Preload"). Data to be preloaded is placed on pins I/O_1–I/O_4, pin 2 is raised to a supervoltage, and CLK_B is raised. The value in the registers can be examined by Observability (see "Register Observability"). Observability mode is entered either by a supervoltage on pin 21 or assertion of the Observability product term. The data in the buried registers is then sent to output pins OR_1–OR_4.

The initialization logic shown, controlled by fuse SA, is discussed later for all registers.

3

Dual-Feedback Macrocells

I/O_1–I/O_4 are the four dual-feedback macrocells (Figure 5). Register bypass is controlled by fuse SO for each macrocell. Feedback from both the flip-flop and the pin allows the same macrocell to function as both a buried state register and a combinatorial I/O or dedicated input.

Note that the combinatorial path is fed by a separate NOR gate, allowing completely independent combinatorial and buried register functions. The buried register signals are named QI/O_1–QI/O_4. The flip-flops are clocked by CLK_1, which can be either CLK_A or CLK_B according to the Clock Mux.

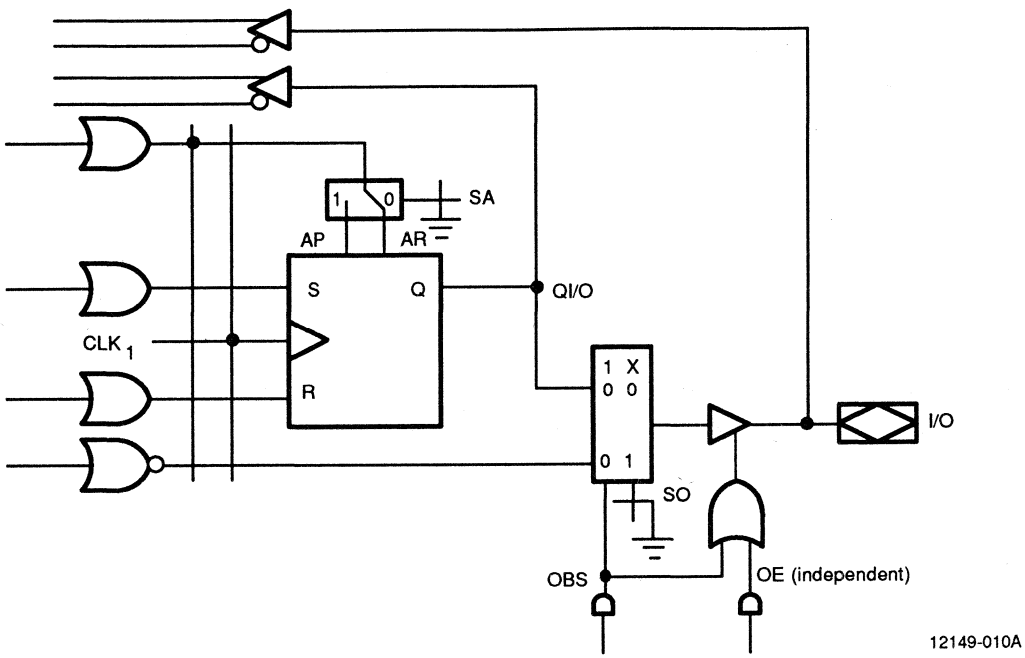
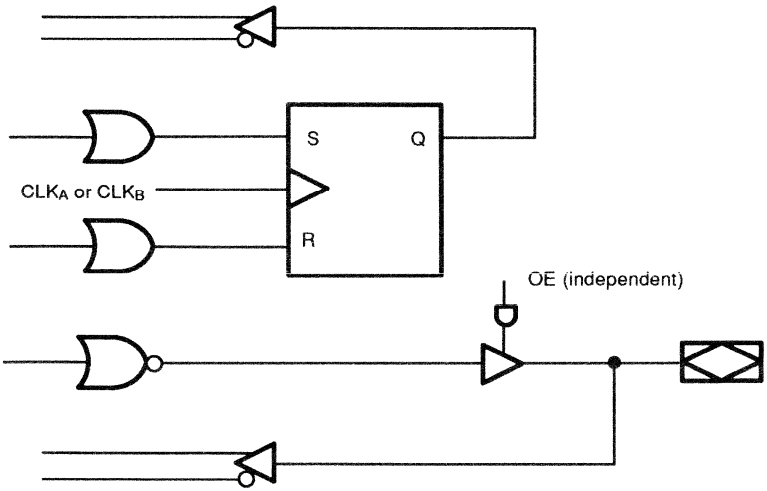
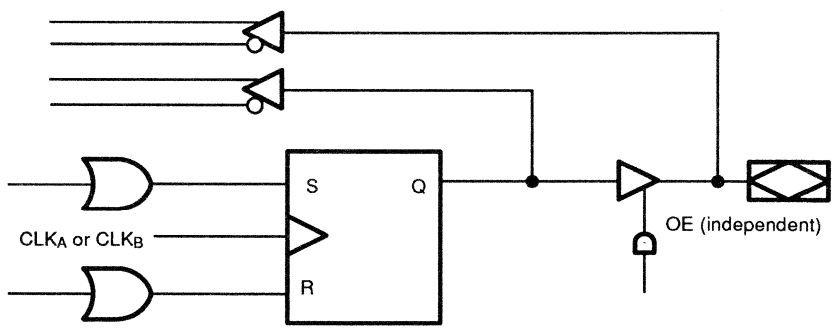


Figure 5a. Dual-Feedback Macrocell



12149-011A

Figure 5b. Dual-Feedback Macrocell Configuration; Buried Register and Combinatorial I/O



12149-012A

Figure 5c. Dual-Feedback Macrocell Configuration; Registered I/O

Each dual-feedback macrocell output has independent output enable control; the outputs I/O_1–I/O_4 are controlled by enable terms OE_1–OE_4, respectively. With the output disabled, the pin can be used as an additional dedicated input. Dynamic enable control allows the pin to be connected to a bus.

The four flip-flops can be preloaded from the associated pins by raising pin 2 and clocking CLK_A (see "Register Preload"). The state of the flip-flops can be observed on the pins in Observability mode, even if buried (see "Register Observability").

Single-Feedback Macrocells

Pins O_1–O_4 provide four additional state registers with either registered or combinatorial outputs (Figure 6). The combinatorial path is independent of the registered path, allowing separate equations for the state bits and the combinatorial outputs. The flip-flops are clocked by the CLK_A input. Register bypass is controlled by fuse SO for each macrocell.

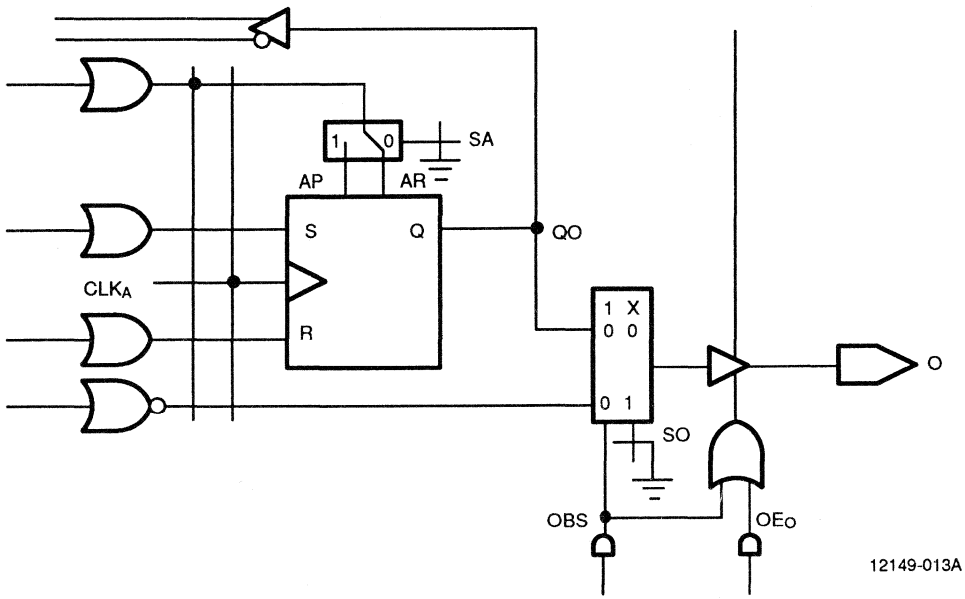


Figure 6a. Single-Feedback Macrocell

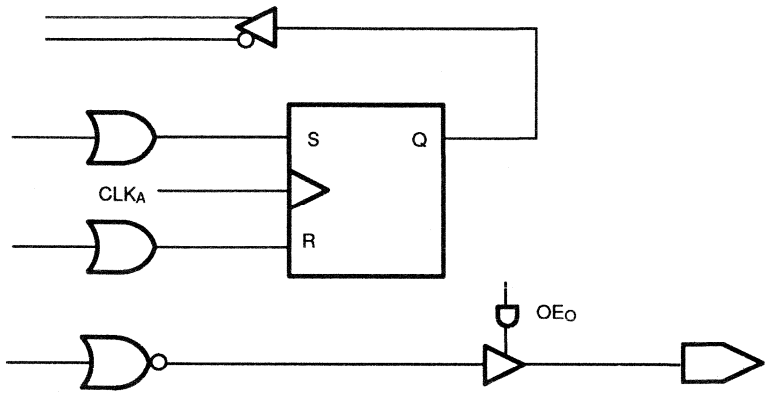


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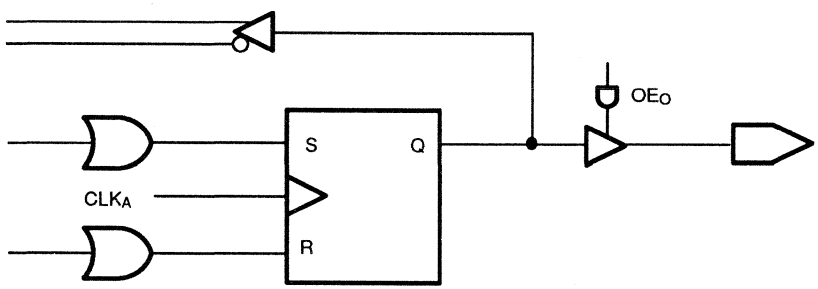
Figure 6b. Single-Feedback Macrocell Configuration; Buried Register and Combinatorial Output



12149-015A

Figure 6c. Single-Feedback Macrocell Configuration; Registered Output with Feedback

All four outputs are controlled by a common output enable term, OE_o. The enable allows connection to a bus.

The associated buried register signals QO_1–QO_4 can be preloaded or observed similarly to Q_1–Q_4 (see "Register Preload").

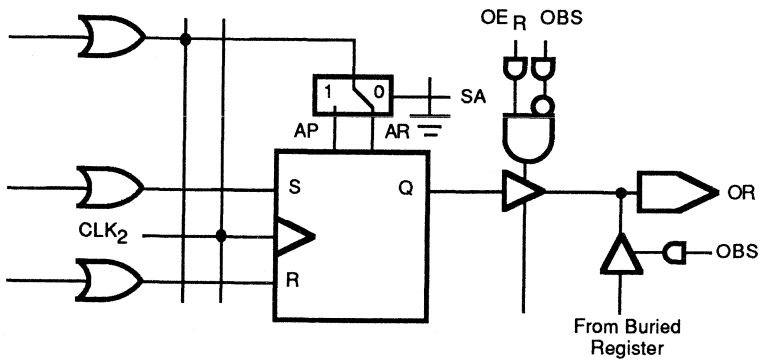


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Figure 7. Output Register

Output Registers

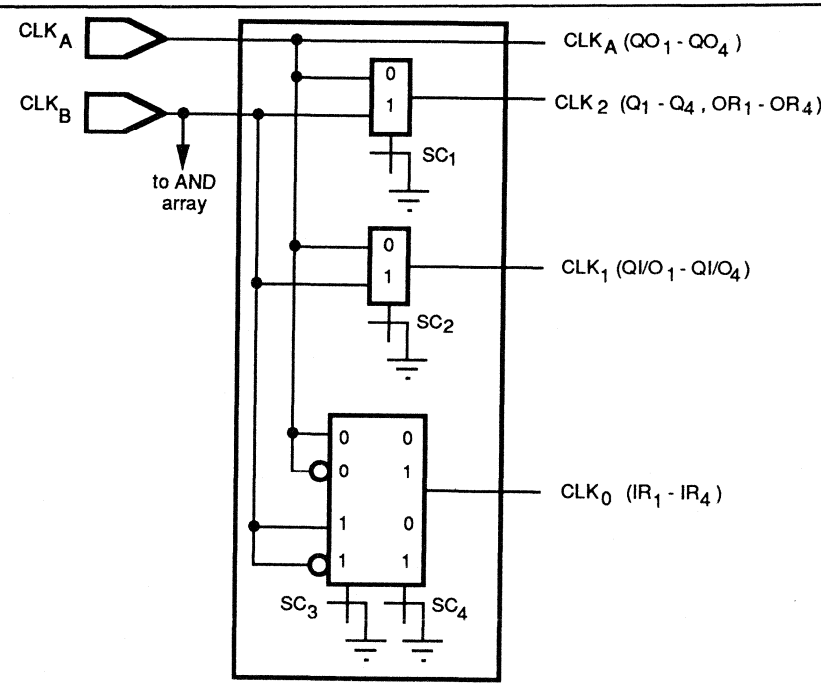
Pins OR_1–OR_4 are dedicated registered outputs (Figure 7). These four flip-flops are clocked on the rising edge of CLK_2, which can be either CLK_A or CLK_B.

The registered outputs are enabled by product term OE_R, allowing connection to a bus.

The register can be preloaded by placing the data on the pins, raising pin 2, and clocking CLK_B (see "Register Preload"). Observability is not necessary since the registers cannot be buried. During observability mode, the outputs are replaced with the buried register values Q_1–Q_4.

Clock Multiplexer

The clock multiplexer takes the two clock inputs CLK_A and CLK_B and creates four separate clocks for the five banks of flip-flops (Figure 8). CLK_0 can be either polarity of CLK_A or CLK_B, and is used to clock the input register. CLK_1 can be the rising edge of either clock input, and is used to clock the dual-feedback macrocell register (QI/O_1–QI/O_4). CLK_2 also can be either CLK_A or CLK_B and is used to clock both the buried register Q_1–Q_4 and the output register OR_1–OR_4. CLK_A is directly used to clock the single-feedback macrocell register QO_1–QO_4. The source for each clock signal is independently controlled by the fuses in the clock mux, SC_1–SC_4 (Table 1).



12149-017A

Figure 8. Clock Multiplexer

Table 1. Clock Mux Logic

SC_1	SC_2	SC_3	SC_4	CLK_0 (IR_1–IR_4)	CLK_1 (QI/O_1–QI/O_4)	CLK_2 (OR_1–OR_4, Q_1–Q_4)
0	0	X	X	CLK_A		
0	1	X	X	/CLK_A		
1	0	X	X	CLK_B		
1	1	X	X	/CLK_B		
X	X	0	X		CLK_A	
X	X	1	X		CLK_B	
X	X	X	0			CLK_A
X	X	X	1			CLK_B

The two clock inputs and clock multiplexer allow two state machines in one device. CLK_A can be used to clock one state machine consisting of at least QO_1–QO_4 while the other state machine can consist of any of the other register groups. The two clock inputs also allow the input registers to be clocked independently of the output/buried registers if CLK_0 is made a function of CLK_B, and CLK_1 and CLK_2 are tied to CLK_A. The user-selectable polarity option on CLK_0 allows the input registers to be clocked on the opposite edge of the same clock input for the output/state registers.

Output Enable

All outputs of the device have three-state buffers. The I/O_1–I/O_4 pins have individual OE product terms, OE_1–OE_4, allowing the user to individually select the required number of outputs and inputs. The O_1–O_4 registered or combinatorial outputs have a single OE product term for the bank, OE_O. Registered outputs OR_1–OR_4 are bank enabled by product term OE_R.

Expansion to larger control functions can be accommodated by connecting several PLS devices to a control bus and selectively enabling them to each handle a segment of the control algorithm. Since the product terms are 0 when unprogrammed, all twelve outputs will be disabled in the unprogrammed state.

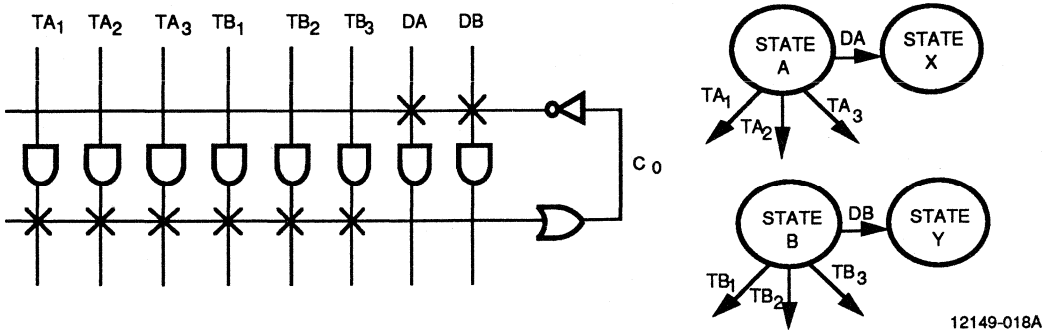


Figure 9. Complement Array - Implementing Default Transitions

Complement Array Terms

The two complement array terms (C_0–C_1) are simply inverted feedback signals from the OR array to the AND array. The complement array can be used to conserve product terms, especially by implementing default transitions.

For local default transitions, or "else" branches, the input to the complement array term is connected to all of the potential transition product terms (TA_1–TA_3) from the given state (A) (Figure 9). When none of these terms is TRUE or HIGH, the C_0 or C_1 signal will be LOW and the inverted feedback will be HIGH. This feedback signal can be connected to a product term that implements the default transition (DA). Since the default product term can also be connected to the state bits that define the present state, the complement array term can be reused for every default transition. As a universal default term, the complement array term can be used as an illegal state recovery term. With two complement arrays, it is easier to define two state machines in one device.

Logic Optimization

The flexibility of the programmable OR array allows two primary advantages over the architecture found in PAL® devices. First, no duplication of product terms is required, since the same product term can be part of multiple output equations. In effect, all 64 product terms are available for all equations. In addition, programmable polarity is not needed, since any equation can be DeMorganized to its opposite polarity. Note that registered outputs are active high with respect to the sum term, and combinatorial outputs are active low with respect to the sum term.

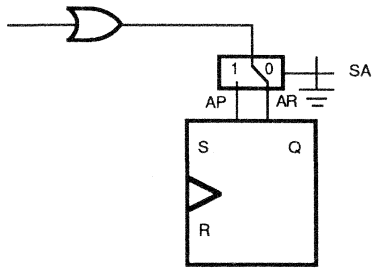


Figure 10a. Initialization

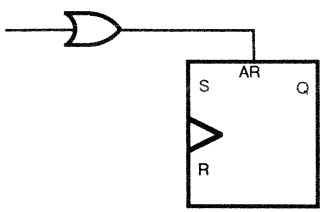


Figure 10b. Initialization; Asynchronous Reset (SA = 0)

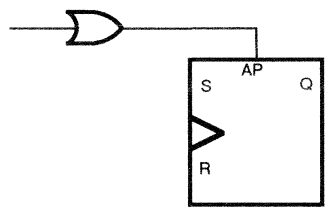


Figure 10c. Initialization; Asynchronous Preset (SA = 1)

12149-019A

3

Initialization

Starting the state machine in a known state is facilitated by circuitry which unconditionally loads a value into each flip-flop using the asynchronous initialization function, provided by a sum term for each nibble of registers. Individual fuses for each flip-flop (SA) dictate this initial value, either LOW or HIGH (Figure 10). The initialization control can be thought of as a 1:2 demultiplexer that selects Asynchronous Reset (AR) in the unprogrammed state (SA = 0), and Asynchronous Preset (AP) when SA is programmed (SA = 1) (Table 2).

Table 2. Initialization Logic

SA	OR TERM	Q
X	0	Q
0	1	0
1	1	1

Synchronous transitions to the initial state can be made by a suitably programmed product term connected to the flip-flops' S or R inputs, as dictated by the state mapping. Whenever this input is active the machine will synchronously transition to the initial state, on the active edge of the appropriate clock signals.

The initialization terms should not be dependent on the I/O pins, since these signals change during preload and observability.

Test Features

Testing of the PLS30S16 is enhanced by the dedicated hardware features of register preload and observability. Register preload allows use of an arbitrary test vector set to fully exercise all state transitions and guard against unreachable states and dead-lock loops. Observability provides visibility of the internal state register outputs when strobed by a supervoltage control signal or enabled by the observability product term.

The added features allow complete functional testing; AMD fully guarantees all AC specifications and timing margins.

Register Preload

All registers on the PLS30S16 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function provides for loading of macrocell registers QO_1–QO_4 and QI/O_1–QI/O_4 using CLK_A, and input registers IR_1–IR_4 and output registers OR_1–OR_4 and the buried state registers Q_1–Q_4 using CLK_B. Data is placed on the pins associated with the register (buried

state registers are loaded using the pins associated with I/O_1–I/O_4), and the appropriate pin is clocked.

Preload mode is entered by placing a supervoltage signal on pin 2 (see "Register Preload"). All outputs immediately enter a high-impedance state. Data to be preloaded should be established on the appropriate pins and either CLK_A or CLK_B pulsed. Following this, data is removed (high-impedance state) and the preload supervoltage removed.

Device Observability

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The PLS30S16 offers an observability feature that allows the user to send the hidden buried register values to observable output pins.

The PLS30S16 observability can be activated either by a supervoltage level applied to pin 21 or by the OBS product term. The contents of buried registers QO_1–QO_4, QI/O_1–QI/O_4 and Q_1–Q_4 are placed on the output pins O_1–O_4, I/O_1–I/O_4, and OR_1–OR_4, respectively (see "Register Observability").

For macrocells that are configured as combinatorial, the observability product term suppresses the selection of the combinatorial output by asserting the macrocell output mux into registered output mode. The observability product term allows the observation of the associated registers by overriding the output enable term and enabling the output buffer.

Note that when the register contents are directed to the pins I/O_1–I/O_4, the signals on the pins fed back to the array can change value. If this happens to satisfy the logic terms associated with device initialization, the contents of some flip-flops may change state. The user is cautioned against using initialization terms involving I/O_1–I/O_4 when device observability is desired.

Security Fuse

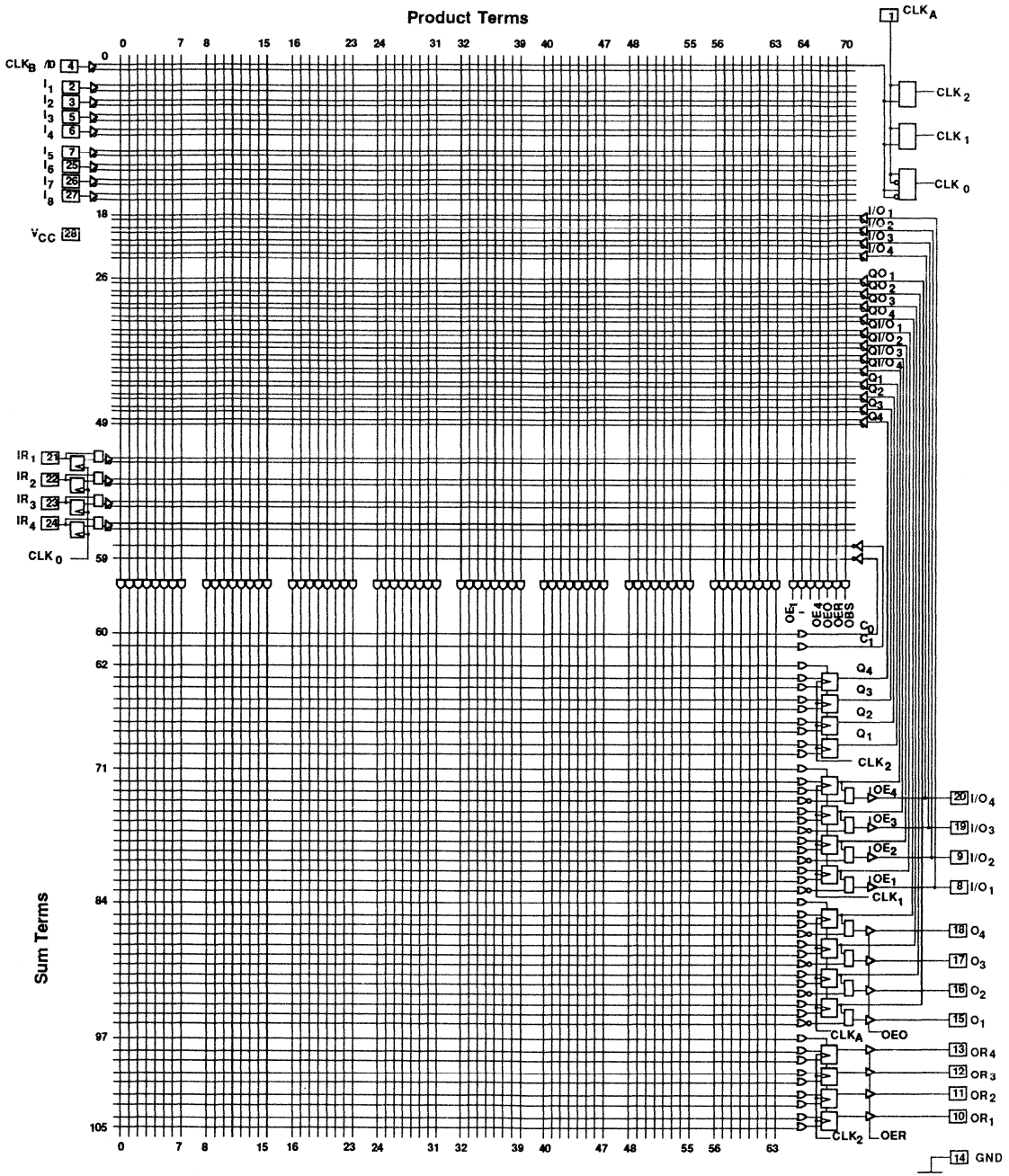
One security fuse in the PLS30S16 is provided to hide proprietary designs from examination by competitors. The security fuse, when programmed, blocks reading of the fuse array, preloading of the registers, and both supervoltage and product-term controlled observability of buried registers. The security fuse is verified by verifying the array as if every fuse were programmed. This security feature gives the user a proprietary circuit which is very difficult to copy.

Technology

The PLS30S16 utilizes AMD's oxide-isolated IMOX™ process for the highest speed. The fuses are composed of proven Platinum-Silicide (PtSi) for high programming yields and high reliability. On-chip test fuses and test circuitry allow factory testing of programmability and all DC and switching characteristics.

Fuses are connected in the unprogrammed state and selectively disconnected during programming. AND gates with all inputs connected are permanently LOW while OR gates with all inputs connected are permanently HIGH. A disconnected fuse floats to a logic one in the AND array and a zero in the OR array. AND gates with all inputs disconnected are permanently HIGH while OR gates with all inputs disconnected are permanently LOW.

LOGIC DIAGRAM



NOTES: 1. All AND gate inputs with a programmed fuse float to a logic "1"
2. All OR gate inputs with a programmed fuse float to a logic "0"

12149-020A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	-0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off–State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		100	µA
I_{OZL}	Off–State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short–Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.		225	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short–circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

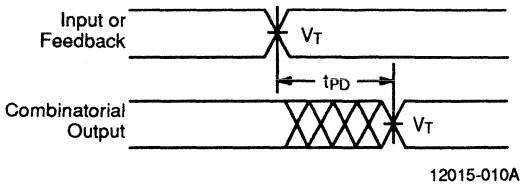
Note:
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output					20	ns
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		15		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array (Note 3)		30		ns
t_{SI}	Setup Time from Input to Clock (Input Register)				3		ns
t_H	Hold Time				0		ns
t_{HI}	Hold Time (Input Register)				2		ns
t_{CO}	Clock to Output					10	ns
t_{CF}	Clock to Feedback (Note 4)					5	ns
t_{CI}	Clock to Input (Input Register)					5	ns
t_I	Asynchronous Initialize to Registered Output					25	ns
t_{IW}	Asynchronous Initialize Width				20		ns
t_{IR}	Asynchronous Initialize Recovery Time				20		ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	Without Complement Array	$1/(t_s + t_{co})$	40		MHz
		Internal Feedback		$1/(t_s + t_{cf})$	50		MHz
f_{MAXC}		External Feedback	With Complement Array	$1/(t_{sc} + t_{co})$	25		MHz
		Internal Feedback		$1/(t_{sc} + t_{cf})$	28.5		MHz
t_{EA}	Input to Output Enable					20	ns
t_{ER}	Input to Output Disable					20	ns

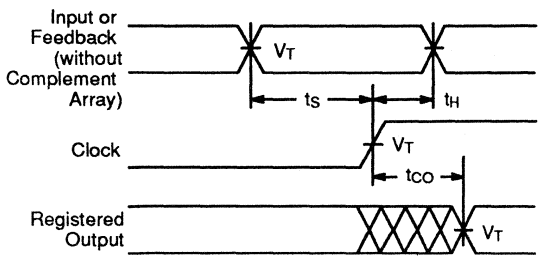
Notes:
2. See Switching Test Circuit for test conditions.
3. Add 15 ns to any path for complement array.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



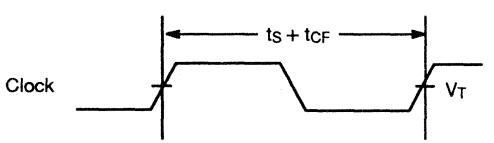
12015-010A

Combinatorial Output



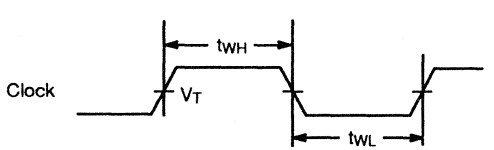
12015-012A

Registered Output without Complement Array



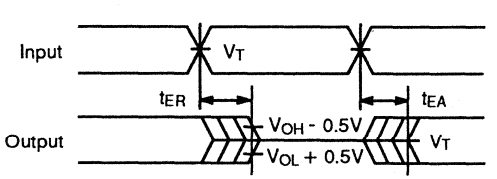
12149-025A

Clock to Feedback (f_{MAX} Internal) See Path at Right



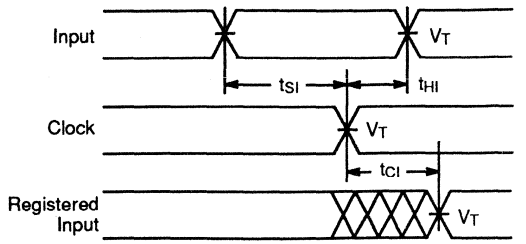
12015-011A

Clock Width



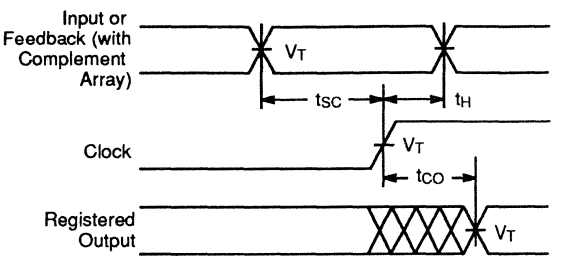
12015-013A

Input to Output Disable/Enable



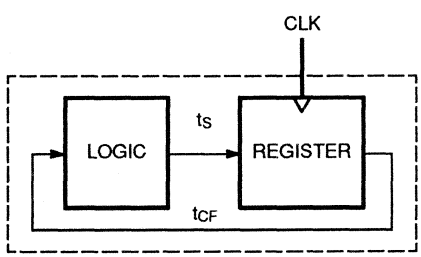
12149-024A

Registered Input

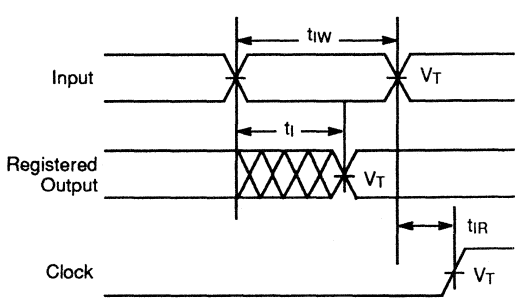


12149-023A

Registered Output (with Complement Array)



12015-021A



12149-028A

Asynchronous Initialization

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

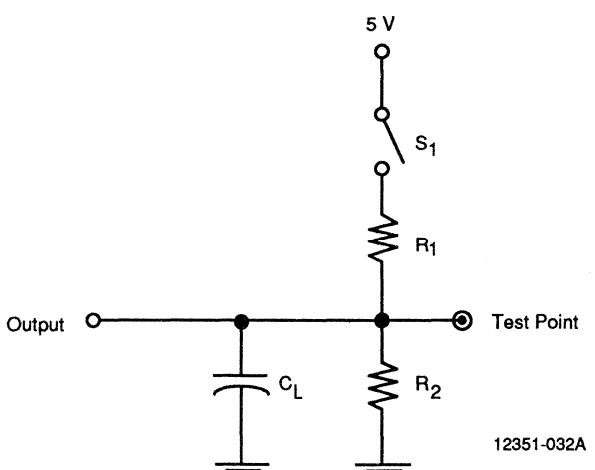
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

3

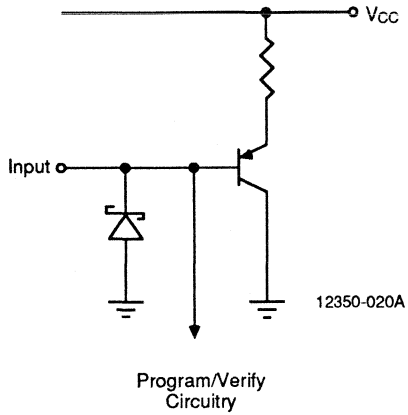
SWITCHING TEST CIRCUIT



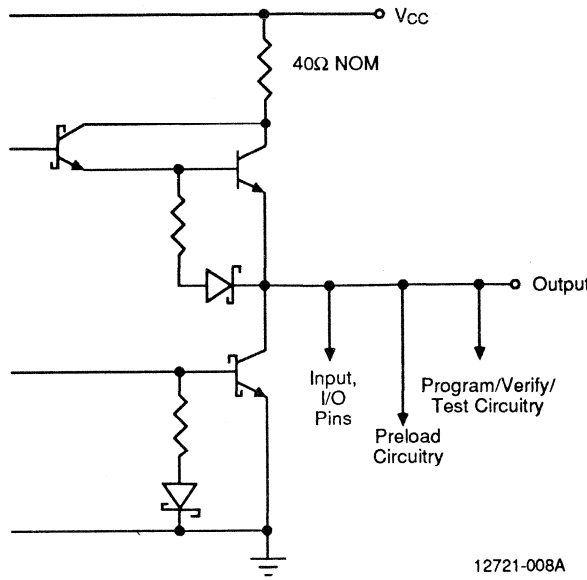
Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output



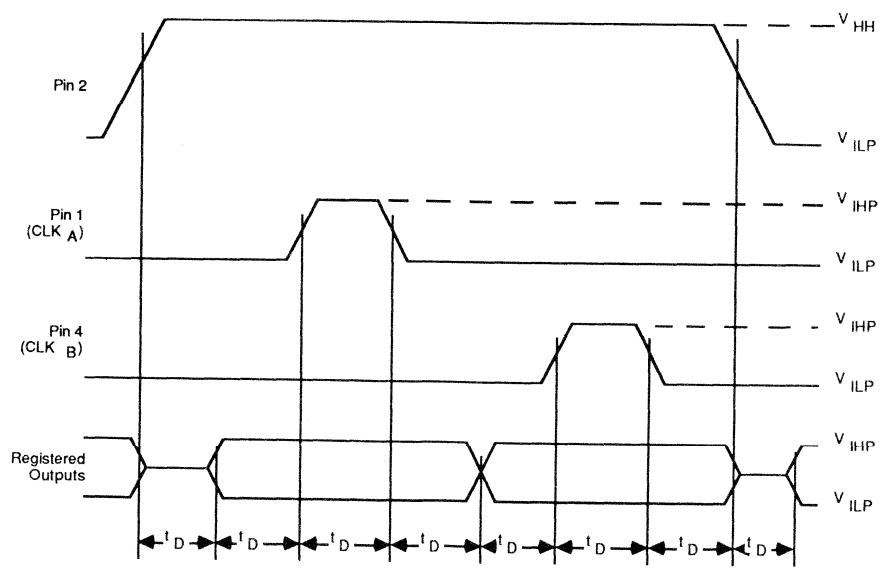
REGISTER PRELOAD

The Preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Raise pin 2 to V_{HH} (11 V) to disable outputs.
3. Apply the desired value (V_{ILP}/V_{IHP}) to outputs. Note that a preloaded HIGH will set the flip-flop HIGH.
4. Pulse the appropriate pin (pin 1 or 4) from V_{ILP} to V_{IHP} to V_{ILP}.
5. Repeat steps 3 and 4 for second set of flip-flops.
6. Remove V_{ILP}/V_{IHP} from all outputs.
7. Lower pin 2 to V_{ILP}.
8. Enable outputs per programmed pattern.
9. Verify for V_{OL}/V_{OH} at all output pins.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	10	11	12	V
V_{ILP}	Low-level input voltage	0	0.3	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Supply voltage during preload	4.5	5.0	5.5	V
t_D	Delay time	0.1	1	15	ms

Register to Preload	Data Input	CLKA	CLKB
QI/O_1–QI/O_4	I/O_1–I/O_4	⎍	L
QO_1–QO_4	O_1–O_4	⎍	L
OR_1–OR_4	OR_1–OR_4	L	⎍
Q_1–Q_4	I/O_1–I/O_4	L	⎍
IR_1–IR_4	IR_1–IR_4	L	⎍



12149-032A

Preload Waveform

REGISTER OBSERVABILITY

The Observability function allows the registers to be viewed at the output pins. This feature aids functional testing of sequential designs by allowing direct observation of register states.

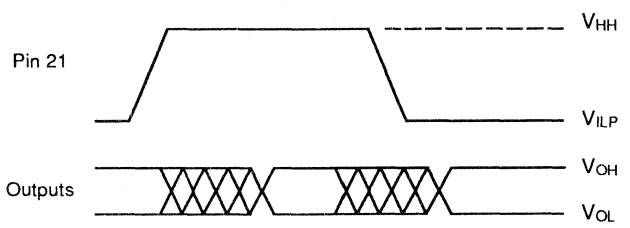
During observability, pins 1 and 4 (the clock pins) should remain LOW. If either pin goes HIGH, the registers will be clocked and the previous data may be lost. As long as these pins remain LOW and asynchronous initialization is not asserted, the data in the registers will not change during Observability. Note that when register data is sent to pins I/O_1–I/O_4, the data will also affect the pin feedback. Care must be taken that this does not assert asynchronous initialization.

The procedure for observability follows.

1. Raise pin 21 to V_{HH} (11 V), or assert Observability term OBS per programmed pattern.
2. Register values will be sent to appropriate outputs.
3. Lower pin 21 or remove OBS term.

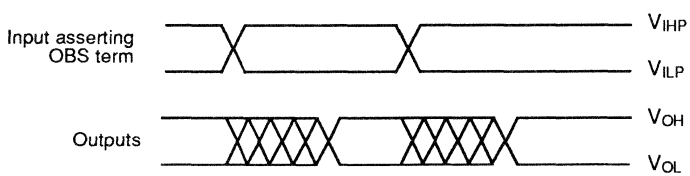
Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	10	11	12	V
V_{ILP}	Low-level input voltage	0	0.3	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V

Register to Observe	Data Output
QI/O_1–QI/O_4	I/O_1–I/O_4
QO_1–QO_4	O_1–O_4
Q_1–Q_4	OR_1–OR_4



12149-033A

Supervoltage Observability



12149-034A

Product Term Observability

Am29CPL151H-25/33

CMOS 64-Word Field-Programmable Controller (FPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements complex state machines**
- **High-speed, low-power CMOS EPROM technology**
- **Functionally equivalent to the bipolar Am29PL141**
- **Seven conditional inputs (each can be registered as a programmable option), 16 outputs**
- **Up to 33-MHz maximum frequency**
- **64-word by 32-bit CMOS EPROM**
- **Space-saving 28-pin OTP plastic SKINNYDIP® and PLCC packages and windowed ceramic SKINNYDIP package**
- **29 instructions**
  - Conditional branching, conditional looping, conditional subroutine call, multiway branch

GENERAL DESCRIPTION

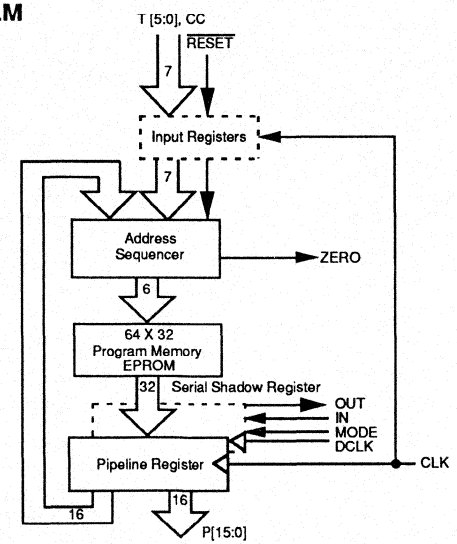
The Am29CPL151 is a CMOS, single-chip Field Programmable Controller (FPC). It allows implementation of complex state machines and controllers by programming the appropriate sequence of instructions. Jumps, loops, and subroutine calls, conditionally executed based on the test inputs, provide the designer with powerful control flow primitives.

Intelligent control may be distributed throughout the system by using FPCs to control various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic, and bus control units. An address sequencer, the heart of the FPC, provides the address to an internal 64-word by 32-bit EPROM.

The Am29CPL151 is functionally equivalent to the Am29PL141 but is manufactured in CMOS technology and offers a space-saving 300-mil SKINNYDIP package. A pin-compatible larger FPC is offered as the Am29CPL154 with a deeper 512 x 36 memory and added flexibility.

This UV-erasable and reprogrammable device utilizes proven floating-gate CMOS EPROM technology to ensure high reliability, easy programming, and better than 99.9% programming yields. The Am29CPL151 is offered in both windowed and One-Time Programmable (OTP) packages. OTP plastic SKINNYDIP and PLCC devices are ideal for volume production.

SIMPLIFIED BLOCK DIAGRAM

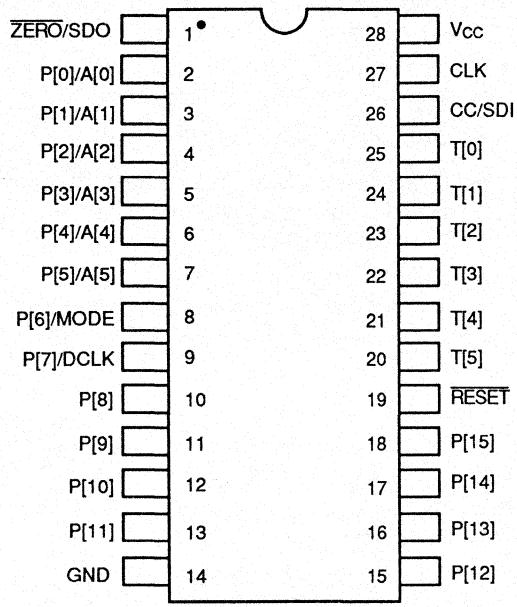


10135-001B

Publication # 10135 Rev. D Amendment /0
Issue Date: November 1989

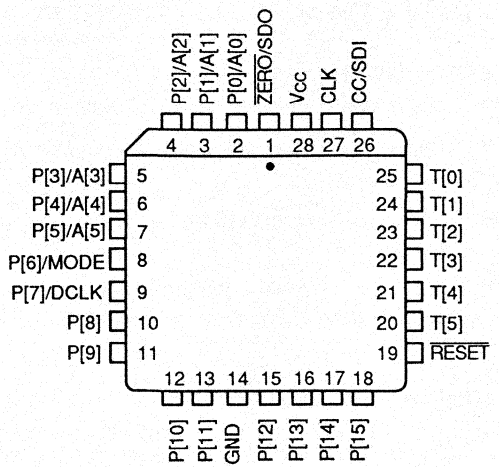
CONNECTION DIAGRAMS
Top View

SKINNYDIP



10135-002B

PLCC/LCC

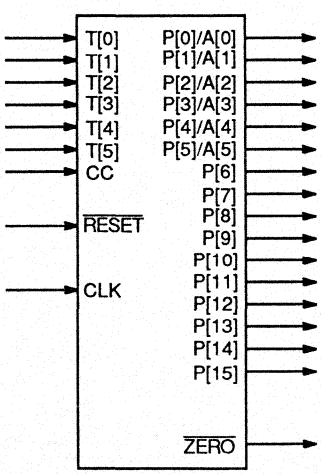


10135-003B

Note:
Pin 1 is marked for orientation.

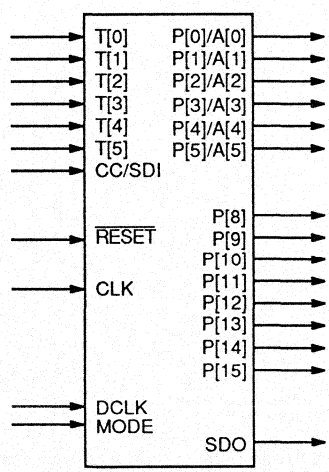
LOGIC SYMBOLS

Normal Configuration



10135-004A

SSR® Diagnostics Configuration

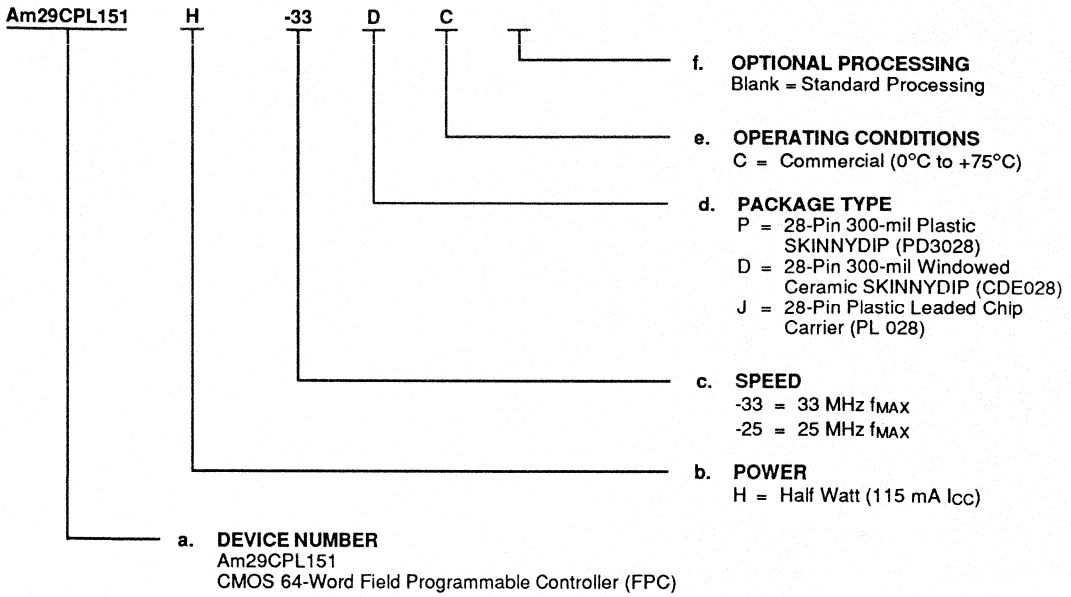


10135-005A

ORDERING INFORMATION
Commercial Products

AMD products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Package Type
e. Operating Conditions
f. Optional Processing



Valid Combinations	
Am29CPL151H-33	PC, DC, JC
Am29CPL151H-25	

Valid Combinations

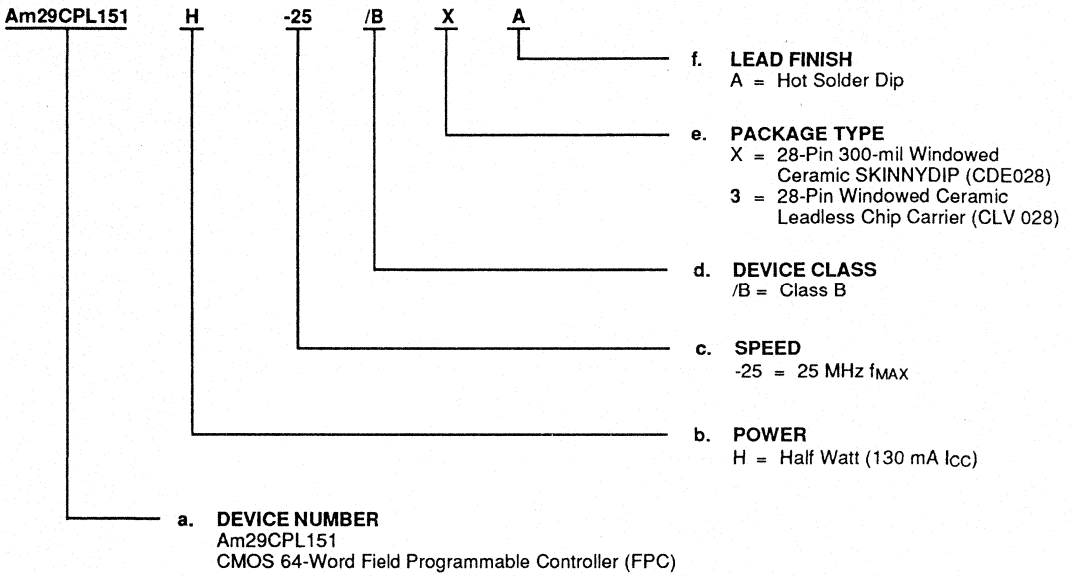
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
Am29CPL151H-25	/BXA, /B3A

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

CC [SDI]

Optionally Registered Condition Code Test Input

When the TEST (P[24:22]) field of the executing instruction is set to 6 (binary 110), CC is selected to be the conditional input. In SSR diagnostic configuration, CC is also the Serial Data Input (SDI). An EPROM bit associated with this input may be programmed to make this input a registered input. The default state of this input is unregistered.

CLK

Clock Input

The rising edge of the clock latches the program counter, count register (CREG), subroutine register (SREG), pipeline register, and EQ flag. The rising edge of the clock also latches the test input registers, CC register, and the $\overline{\text{RESET}}$ register if their respective configuration bits are set to enable internal synchronizing registers.

P[15:8]

Outputs

The upper eight general-purpose control outputs are enabled by the OE signal from the pipeline register. When OE is HIGH, P[15:8] are enabled, and when LOW, P[15:8] are disabled.

P[7:6], P[5:0]/A[5:0] [DCLK, MODE]

Outputs

The lower eight general-purpose control outputs are permanently enabled. In the SSR diagnostic configuration, P[7] becomes the diagnostic clock input DCLK and P[6] becomes the diagnostic control input MODE. In expand mode (when the EXP bit is programmed) bits P[5:0] become the Program Memory address outputs A[5:0].

$\overline{\text{RESET}}$

Optionally Registered $\overline{\text{Reset}}$ Input; Active LOW

When the reset input is LOW, the output of the PC MUX is forced to the uppermost program address (63). On the next rising edge of the clock, this address (63) is loaded into the program counter; the instruction at location 63 is loaded into the pipeline register, and the EQ flag is cleared. A programmable configuration bit allows the option of making this a registered input. If $\overline{\text{RESET}}$ is internally registered, the first rising edge of the clock latches it. On the next rising edge of the clock, the EQ flip-flop is cleared and the contents of memory location 63 are loaded into the pipeline register. The default state of this input is unregistered.

T[5:0]

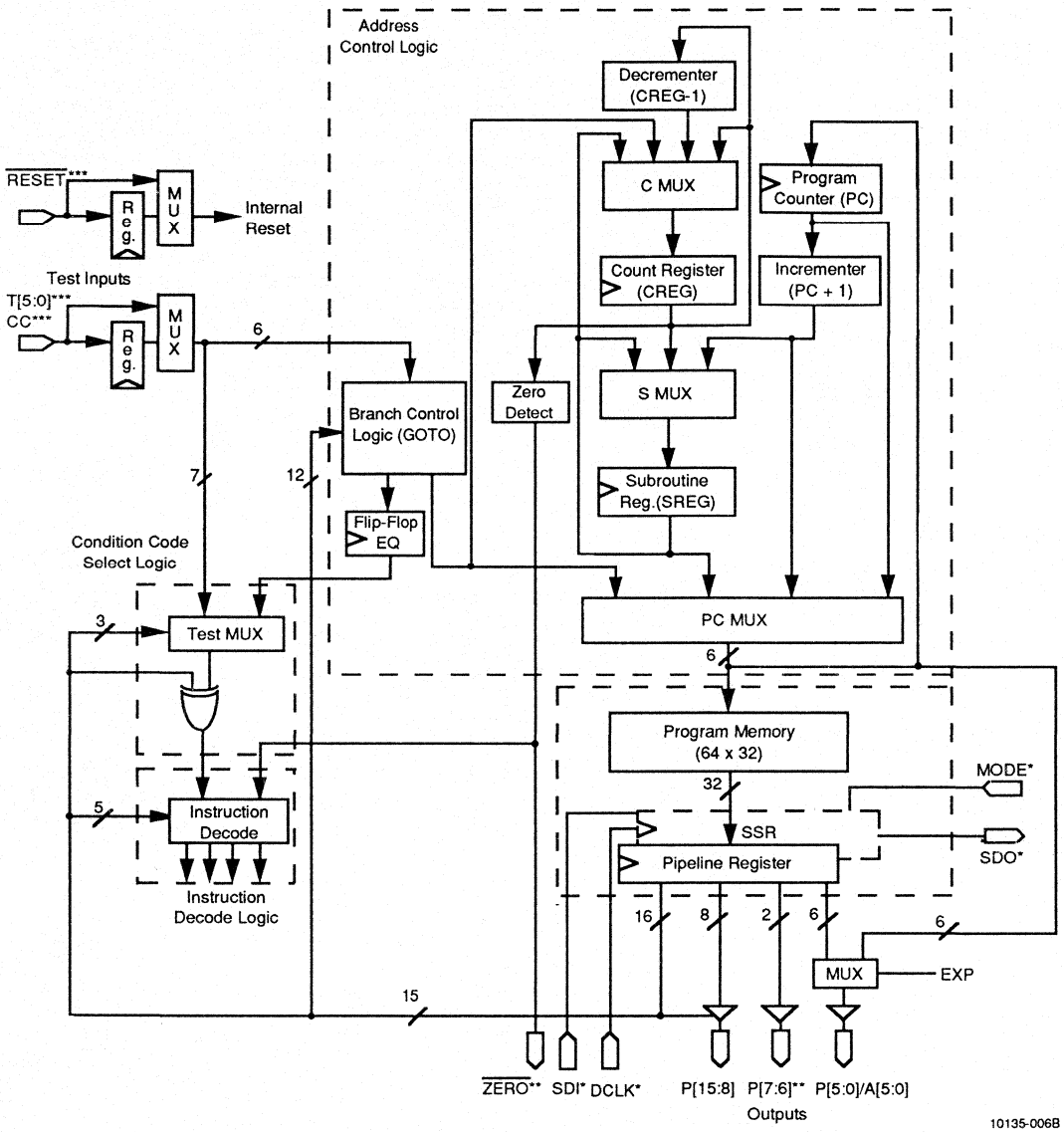
Optionally Registered Test Inputs

In conditional instructions, the TEST inputs can be used as individual condition codes selected by the TEST field in the pipeline register. The T[5:0] inputs can also be used as a branch address when performing a program branch or as a count value to be loaded into the CREG. Each of these inputs has an EPROM bit associated with it. This bit may be programmed such that the corresponding input becomes a registered input. The default state of these inputs is unregistered.

$\overline{\text{ZERO}}$ [SDO]

Zero Output; Active LOW

A LOW state on the $\overline{\text{ZERO}}$ output indicates that the CREG value is zero. In the SSR diagnostic configuration, $\overline{\text{ZERO}}$ becomes the Serial Data Output (SDO). This change is only on the output pin; internally, the zero-detect function is unchanged.



* These pins available only in SSR mode.
** These pins available only in normal mode.
*** Each of the T[5:0], $\overline{\text{RESET}}$, and CC inputs can be individually registered or left unregistered as a programmable option.

10135-006B

Figure 1. Am29CPL151 Detailed Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1, the detailed block diagram of the Am29CPL151, shows logic blocks and interconnecting buses that permit parallel performance of different operations in a single instruction. The FPC consists of four main logic blocks: the program memory, address control logic, condition code selection logic, and instruction decode. A fifth optional block is the Serial Shadow Register (SSR).

The program memory contains the user-defined instruction flow and output sequence. The address control logic addresses the program memory. This control logic supports high-level instruction functions including conditional branches, subroutine calls and returns, loops, and multiway branches. The condition code selection logic selects the condition code input to be tested when a conditional instruction is executed. The polarity of the selected condition code input is controlled by the POL bit in the microword. The instruction decode generates the control signals necessary to perform the instruction specified by the instruction part (P[31:16]) of the microword. The SSR enables in-system testing to isolate problems down to the IC level.

Program Memory

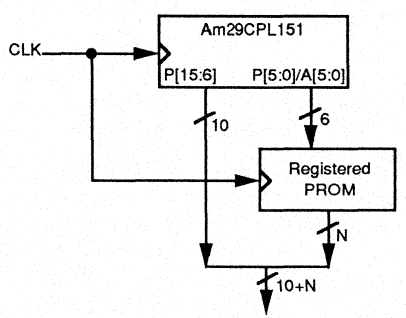
The FPC program memory is a 64-word by 32-bit EPROM with a 32-bit pipeline register at its output. The upper 16 bits (P[31:16]) of the pipeline register are internal to the FPC and form the instruction to control address sequencing. The format for instructions is: a one-bit synchronous Output Enable OE, a five-bit OPCODE, a one-bit test polarity select POL, a three-bit TEST condition select field, and a six-bit immediate DATA field. The DATA field is used to provide branch addresses, test input masks, and counter values.

The lower 16 bits (P[15:0]) of the pipeline register are brought out as user-defined, general-purpose control outputs. The upper eight control outputs (P[15:8]) are disabled when OE is programmed as a LOW. The lower eight control bits (P[7:0]) are always enabled. Outputs P[5:0] will contain the next instruction address when the optional EXP EPROM cell is programmed.

Controlling External PROM

By programming the EXP bit, PC MUX is output over pins P[5:0]/A[5:0]. This feature can be used to extend the width of the output control word when external registered memories are used. In the diagram below, the Am29CPL151 controls external registered PROMs to provide an output control word (10 + N) bits wide (where N is the bit width of the PROMs).

3



10135-038B

Figure 2. Controlling External PROM

Address Control Logic

The address control logic consists of five smaller logic blocks. These are:

PC MUX –Program counter multiplexer

P CNTR –Program counter (PC) and incrementer (PC + 1)

SUBREG –Subroutine register (SREG) with subroutine mux (S MUX)

CNTR –Count register (CREG) with counter mux (C MUX), decrementer (CREG–1), and zero detect

GOTO –Specialized branch control logic

The PC MUX is a six-bit, four-to-one multiplexer. It selects either the PC, PC + 1, SREG, or GOTO output as the next microaddress input to the Program Memory and to the PC. The PC thus always contains the address of the instruction in the pipeline register. During a Reset, the PC MUX output is forced to all ones, selecting location 63 from Program Memory.

The P CNTR block consists of a six-bit register (PC) driving a six-bit combinatorial incrementer (PC + 1). Either the present or the incremented values of PC can address the Program Memory. The incremented value of PC can be saved as a subroutine return address. The present PC value can address the Program Memory when waiting for a condition to become valid. PC + 1 addresses the Program Memory for sequential program flow, for unconditional instructions, and as a default for conditional instructions.

The SUBREG block consists of a six-bit, three-to-one multiplexer (S MUX) driving a six-bit register (SREG). The three possible SREG inputs are PC + 1, CREG, and SREG. SREG normally operates as a one-deep stack to save subroutine return addresses. PC + 1 is the input source when performing subroutine calls, and PC MUX is the output destination when performing return from subroutine.

The CNTR block consists of a six-bit, four-to-one multiplexer (C MUX), driving a six-bit register (CREG); a six-bit combinatorial decrementer (CREG-1); and a zero-detection circuit. The CNTR logic block is typically used for timing functions and iterative loop counting.

The SUBREG and CNTR can be considered as one logic block because of their unique interaction. Both have the other as an additional input source and output destination. The CREG can therefore be an additional stack location when not used for counting, and the SREG can be a nested-count location when not used as a stack location. Thus the SREG and CREG can operate in three different modes:

1. As a separate one-deep stack and counter
2. As a two-deep stack
3. As a two-deep nested counter

The GOTO logic block serves three functions:

1. It provides a six-bit count value from the DATA field in the pipeline register (P[21:16]) or from the TEST inputs T[5:0] masked by the DATA field P[21:16]. This is represented by T*M.
2. It provides a branch address from the DATA field in the pipeline register P[21:16] or from the TEST inputs T[5:0] masked by the DATA field P[21:16]. This is represented by T*M.
3. It compares T[5:0] masked by the MASK field P[21:16], called T*M, to the CONSTANT field from the pipeline register P[27:22]. If a match occurs, the EQ flip-flop is set. EQ remains unchanged if there is no match. Constant field bits that correspond to masked test bits must be zero.

The EQ flag can be tested by the condition code selection logic. Multiple tests of any group of T inputs in a manner analogous to sum-of-products can be performed since a no-match comparison does not reset the EQ flag. Any conditional branch on EQ will reset the EQ flag. Conditional returns on EQ will not change the EQ flag. $\overline{\text{RESET}}$ input LOW will reset the EQ flag.

Note: A zero in the MASK field blocks the corresponding bit in the TEST field; a one activates the corresponding bit.

The constant field bits that correspond to masked test field bits must be zero. A zero is substituted for masked test field bits. The "POL" bit is a "don't care" when using test inputs to load registers.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Condition Code Selection Logic

The condition code selection logic consists of an eight-to-one multiplexer. The eight test condition inputs are the device inputs CC, T[5:0], and the EQ flag. The TEST field P[24:22] selects one of the eight conditions to test.

The polarity bit POL in the instruction allows the user to test for either a pass or fail condition. Refer to table1 for details.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

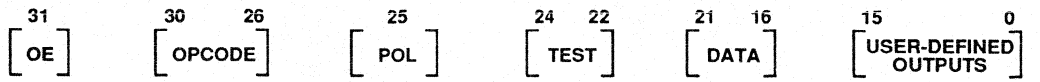
Instruction Decode

The instruction decoder is a PLA that generates the control for 29 different instructions. The decoder inputs include the OPCODE field P[30:26], the zero detection output from the CNTR, and the selected test condition code from the condition code selection logic.

Operational Modes

The Am29CPL151 operates as a six-bit microcontroller in normal mode, and there are several configuration bits that can be programmed to modify this normal operation. The EXP bit allows the six program address lines from the PC MUX to be output on the lower six bits of the output pins (P[5:0]) so that a user can expand the width of the control lines by using external registered memories. The SSR bit allows on-chip diagnostic capabilities for in-system testing. The remaining bits serve to individually select whether the input pins will be unsynchronized or not. The default setting of these bits (unprogrammed,1) will cause each pin to be unsynchronized, and so programming a given bit (to 0) will cause that corresponding input to become internally synchronized.

Am29CPL151 General Instruction Format



10135-007B

WHERE:
OE = Synchronous Output Enable for P[15:8].
OPCODE = A five-bit opcode field for selecting one of the 28 single-data-field instructions.
POL = A one-bit test condition polarity select (refer to table 1).
TEST = A three-bit test condition select.

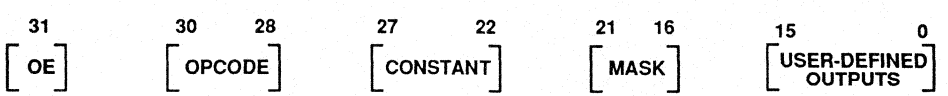
TEST[24:22]	UNDER TEST
000	T [0]
001	T [1]
010	T [2]
011	T [3]
100	T [4]
101	T [5]
110	CC
111	EQ

DATA = A six-bit conditional branch address, test input mask, or counter value field designated as PL in instruction mnemonics.

Table 1

Input Condition Being Tested	POL	Test Result
0	0	Fail
0	1	Pass
1	0	Pass
1	1	Fail

Am29CPL151 Comparison Instruction Format



10135-008B

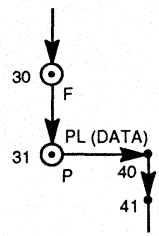
WHERE:
OE = Synchronous Output Enable for P[15:8].
OPCODE = Compare instruction (binary 100).
CONSTANT = A six-bit constant for equal-to comparison with T*M.
MASK = A six-bit mask field for masking the incoming T[5:0] inputs.

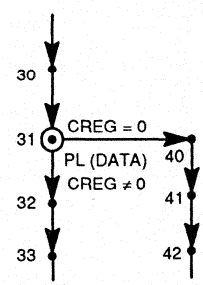
Am29CPL151 INSTRUCTION SET DEFINITION

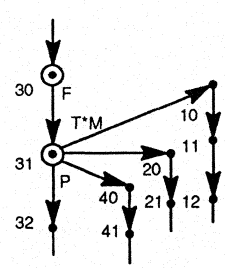
• = Other instruction
⊙ = Instruction being described
○ = Register in part

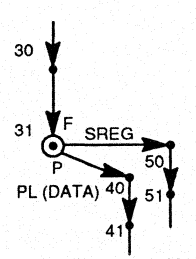
P = Test Pass
F = Test Fail
X,Y are arbitrary values in the CREG or SREG

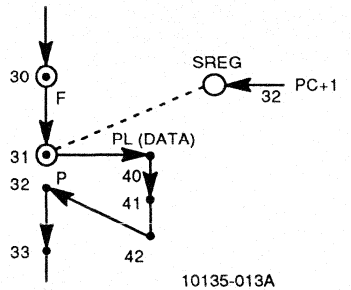
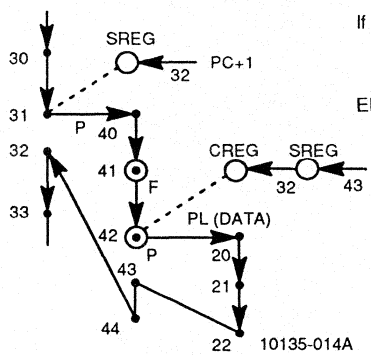
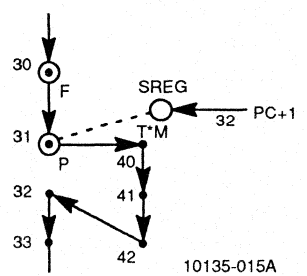
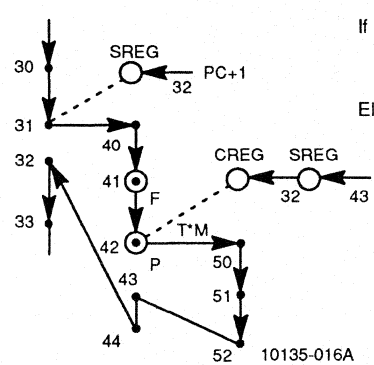
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

19	GOTOPL	**IF (cond) THEN GOTO PL (data)**
		Conditional branch to the address in the PL (DATA field). The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-009A
				If (cond = true) Then
				PC = PL(data)
				Else
				PC = PC + 1

0B	GOTOPLZ	**IF (CREG = 0) THEN GOTO PL (data)**
		Conditional branch to the address in the PL (DATA field) when CREG is equal to zero. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and the CREG is equal to zero.
			
			10135-010A
				If (CREG = 0) Then
				PC = PL(data)
				Else
				PC = PC + 1

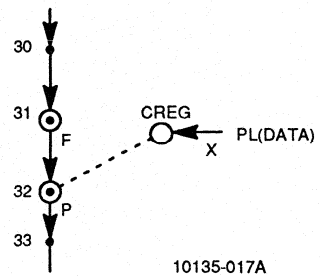
0F	GOTOTM	**IF (cond) THEN GOTO TM (data)**
		Conditional branch to the address defined by the T*M (T[5:0] under bitwise mask from the DATA field). This instruction is intended for multiway branches. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-011A
				If (cond = true) Then
				PC = T*M
				Else
				PC = PC + 1

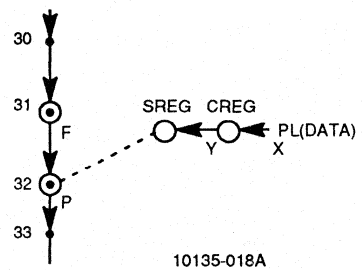
18	FORK	**IF (cond) THEN GOTO PL (data) ELSE GOTO (SREG)**
		Conditional branch to the address in the PL (DATA field) or the SREG. A branch to PL is taken if the condition is true and a branch to SREG if false. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-012A
				If (cond = true) Then
				PC = PL(data)
				Else
				PC = SREG

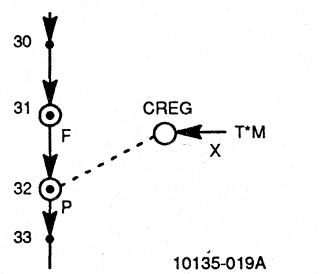
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
1C	CALPL	**IF (cond) THEN CALL PL (data)** Conditional jump to subroutine at the address in the PL (DATA field). The PC + 1 is pushed into the SREG as the return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-013A	If (cond = true) Then SREG = PC + 1 PC = PL(data) Else PC = PC + 1
1D	CALPLN	**IF (cond) THEN CALL PL (data), NESTED** Conditional jump to subroutine at the address in the PL (DATA field) nested. The SREG and CREG are treated as a two-deep stack, the PC + 1 is pushed into the SREG as the return address, and the previous SREG value is transferred into the CREG as a nested return address. The EQ flag will be reset of the test field selects it and the condition passes.	 10135-014A	If (cond = true) Then CREG = SREG SREG = PC + 1 PC = PL(data) Else PC = PC + 1
1E	CALTM	**IF (cond) THEN CALL TM (data)** Conditional jump to subroutine at the address specified by the T*M (T[5:0] under bitwise mask from the DATA field). The PC + 1 is pushed into the SREG as the return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-015A	If (cond = true) Then SREG = PC + 1 PC = T*M Else PC = PC + 1
1F	CALTMN	**IF (cond) THEN CALL TM (data), NESTED** Conditional jump to subroutine at the address specified by the T*M (T[5:0] under bitwise mask from the DATA field) nested. The PC + 1 is pushed into the SREG as the return address, and the previous SREG value is transferred into the CREG as a nested return address. The EQ flag will be reset of the test field selects it and the condition passes.	 10135-016A	If (cond = true) Then CREG = SREG SREG = PC + 1 PC = T*M Else PC = PC + 1

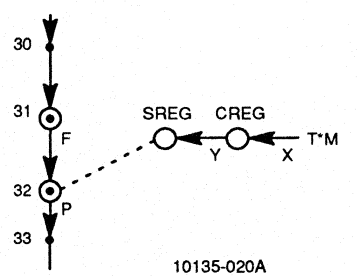
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

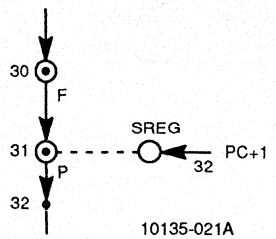
04	LDPL	**IF (cond) THEN LOAD PL (data)**
		Conditional load the CREG from the PL (DATA field).
			
			10135-017A
				If (cond = true) Then
				CREG = PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

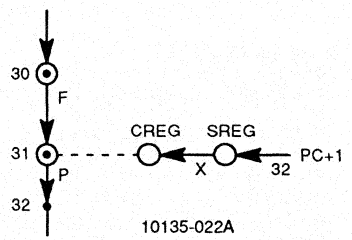
05	LDPLN	**IF (cond) THEN LOAD PL (data), NESTED**
		Conditional load the CREG from the PL (DATA field) nested. The CREG and SREG are treated as a two-deep nested count register, the previous CREG value is pushed into the SREG as a nested count, and the CREG is loaded from PL.
			
			10135-018A
				If (cond = true) Then
				SREG = CREG
				CREG = PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

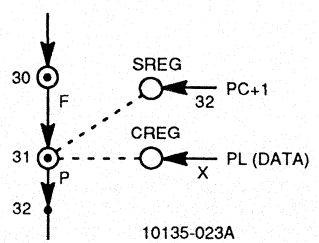
06	LDTM	**IF (cond) THEN LOAD TM (data)**
		Conditional load the CREG from the T*M (T[5:0] inputs under bit-wise mask from the DATA field).
			
			10135-019A
				If (cond = true) Then
				CREG = T*M
				PC = PC + 1
				Else
				PC = PC + 1

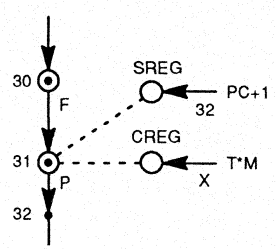
07	LDTMN	**IF (cond) THEN LOAD TM (data) NESTED** Conditional load the CREG from the T*M (T[5:0] inputs under bit-wise mask from the DATA field) nested. The SREG and CREG are treated as a two-deep nested count register, the previous CREG value is transferred into the SREG, and the CREG is loaded from T*M.	 10135-020A	If (cond = true) Then SREG = CREG CREG = T*M PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

15	PSH	**IF (cond) THEN PUSH**
		Conditional push the PC + 1 into the SREG.
			
			10135-021A
				If (cond = true) Then
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

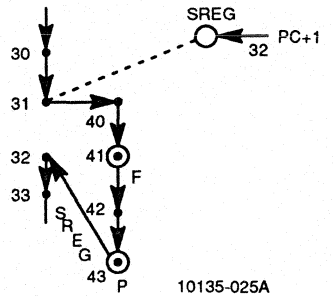
17	PSHN	**IF (cond) THEN PUSH, NESTED**
		Conditional push the PC + 1 into the SREG nested. This microinstruction treats the SREG and CREG as a two-deep stack, PC + 1 is pushed into SREG, and the previous value in SREG is transferred into the CREG.
			
			10135-022A
				If (cond = true) Then
				CREG = SREG
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

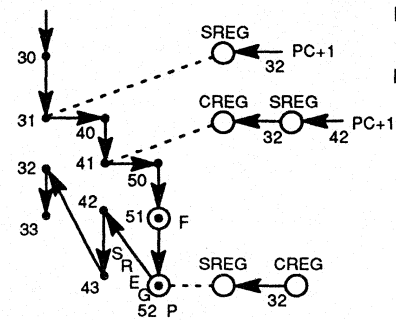
14	PSHPL	**IF (cond) THEN PUSH, LOAD PL (data)**
		Conditional push the PC + 1 into the SREG and load the CREG from the PL (DATA field).
			
			10135-023A
				If (cond = true) Then
				CREG = PL(data)
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

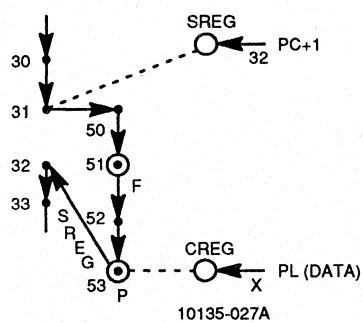
16	PSHTM	**IF (cond) THEN PUSH, LOAD TM (data)**
		Conditional push the PC + 1 into the SREG and load the CREG from the T*M (T[5:0] under bitwise mask from the DATA field).
			
			10135-024A
				If (cond = true) Then
				CREG = T*M
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

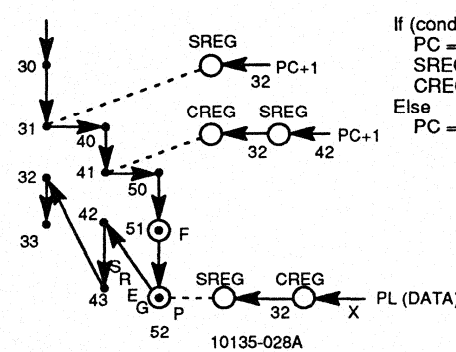
Am29CPL151 INSTRUCTION SET DEFINITION (Continued)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

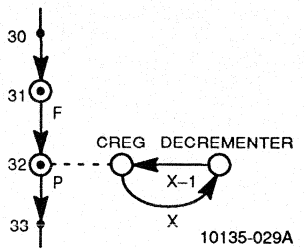
02	RET	**IF (cond) THEN RET**
		Conditional return from subroutine. The SREG provides the return from subroutine address.
			
			10135-025A
				If (cond = true) Then
				PC = SREG
				Else
				PC = PC + 1

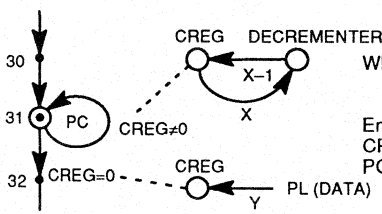
03	RETN	**IF (cond) THEN RET, NESTED**
		Conditional return from nested subroutine. This instruction treats the SREG and CREG as a two-deep stack providing the SREG value as a return address, and the CREG value as a nested return address that is transferred into the SREG.
			
			10135-026A
				If (cond = true) Then
				PC = SREG
				SREG = CREG
				Else
				PC = PC + 1

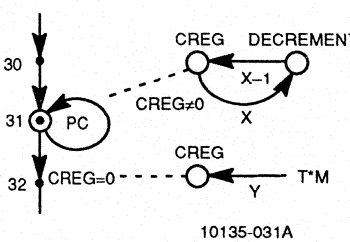
00	RETPL	**IF (cond) THEN RET, LOAD PL (data)**
		Conditional return from subroutine and load the CREG from the PL (DATA field). The SREG provides the return from subroutine address.
			
			10135-027A
				If (cond = true) Then
				CREG = PL(data)
				PC = SREG
				Else
				PC = PC + 1

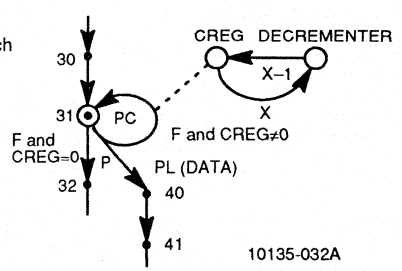
01	RETPLN	**IF (cond) THEN RET NESTED, LOAD PL (data)**
		Conditional return from nested subroutine and load the CREG from the PL (DATA field). This instruction treats the SREG and CREG as a two-deep stack providing the SREG value as a return address, and the CREG value as a nested return address that is transferred into the SREG.
			
			10135-028A
				If (cond = true) Then
				PC = SREG
				SREG = CREG
				CREG = PL(data)
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

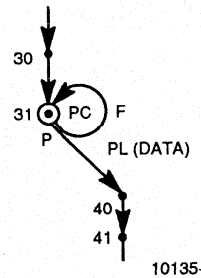
09	DEC	**IF (cond) THEN DEC**
		Conditional decrement of the CREG.
				If (cond = true) Then
				CREG = CREG –1
				PC = PC + 1
				Else
				PC = PC + 1

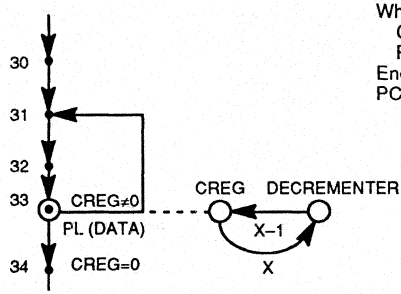
0C	DECPL	**WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the PL (DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be re-loaded from PL. This instruction does not depend on the pass/fail condition.
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = PL(data)
				PC = PC + 1

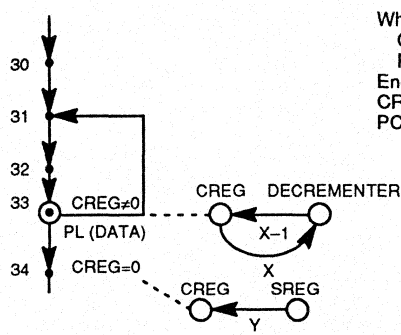
0E	DECTM	**WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the T*M (T[5:0] under bitwise mask from the DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while the CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from T*M. This instruction does not depend on the pass/fail condition.
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = T*M
				PC = PC + 1

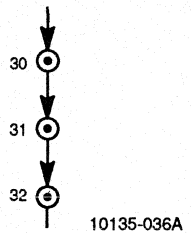
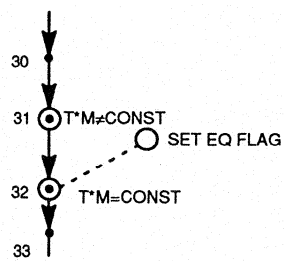
1B	DECGOPL	**If (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT**
		Conditional Hold/Count. The current instruction will be refetched and the CREG decremented until the condition under test becomes true or the counter is equal to zero. If the condition becomes true, a branch to the address in the PL (DATA field) is executed. If the counter becomes zero without the condition becoming true, a CONTINUE is executed. The EQ flag will be reset if the test field selects it and the condition passes.
				While (cond = false)
				If (CREG < > 0)
				CREG = CREG –1
				PC = PC
				Else
				PC = PC + 1
				End While
				PC = PL (data)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

1A	WAIT	**IF (cond) THEN GOTO PL (data) ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When true, a branch to the address in the PL (DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-033A
				If (cond = true) Then
				' PC = PL (data)
				Else
				PC = PC

08	LPPL	**WHILE (CREG < > 0) LOOP TO PL (data)**
		Conditional loop to the address in the PL (DATA field). This instruction is intended to be placed at the bottom of an iterative loop. If the CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the loop) is executed. If the CREG is equal to zero, looping is complete and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10135-034A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PL (data)
				End While
				PC = PC + 1

0A	LPPLN	**WHILE (CREG < > 0) LOOP TO PL (data) ELSE NEST**
		Conditional loop to the address in the PL (DATA field) nested. The SREG and CREG are treated as a two-deep nested count register, and the instruction is intended to be placed at the bottom of an "inner-nested" iterative loop. If the CREG is not equal to zero, the CREG is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the inner loop) is executed. If the CREG is equal to zero, the inner loop is complete, and the count value for the outer loop is transferred from the SREG into the CREG. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10135-035A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PL(data)
				End While
				CREG = SREG
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
0D	CONT	**CONTINUE** The next sequential instruction is fetched unconditionally.	 10135-036A	PC = PC + 1
10–13 (100XX binary)	CMP	**CMP TM (mask) TO PL (constant)** This instruction performs bitwise Exclusive-OR of T*M (T[5:0] under bitwise mask from the MASK field) with CONSTANT (P[27:22]). If T*M equals CONSTANT, the EQ flag is set to one, which may be branched on in a following instruction. If not equal, the EQ flag is unaffected. This allows sequences of compares, in a manner analogous to sum-to-products, to be performed which can be followed by a single conditional branch if one or more of the comparisons are true. Note: The EQ flag is set to zero on reset or when EQ is selected as the test condition in a branch. Conditional returns on EQ leave the flag unchanged. Constant field bits that correspond to masked test field bits must be zero. This instruction does not depend on the pass/fail condition.	 10135-037A	Compare T*M and CONSTANT EQ = ((T [5:0] .AND. MASK) .XNOR. CONSTANT) .OR. EQ PC = PC + 1

3

INSTRUCTIONS BASED ON TEST CONDITIONS

Op-code	Mnemonic	Assembler Statement	Condition Pass				Condition Fail				Notes
			PC MUX	SREG	CREG	EQ FLAG	PC MUX	SREG	CREG	EQ FLAG	
00	RETPL	IF (cond) THEN RET, LOAD PL (data)	SREG	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
01	RETPLN	IF (cond) THEN RET NESTED, LOAD PL (data)	SREG	Load CREG	Load PL	NC	PC + 1	Hold	Hold	NC	
02	RET	IF (cond) THEN RET	SREG	Hold	Hold	NC	PC + 1	Hold	Hold	NC	
03	RETN	IF (cond) THEN RET, NESTED	SREG	Load CREG	Hold	NC	PC + 1	Hold	Hold	NC	
04	LDPL	IF (cond) THEN LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
05	LDPLN	IF (cond) THEN LOAD PL (data), NESTED	PC + 1	Load CREG	Load PL	NC	PC + 1	Hold	Hold	NC	
06	LDTM	IF (cond) THEN LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC + 1	Hold	Hold	NC	
07	LDTMN	IF (cond) THEN LOAD TM (data), NESTED	PC + 1	Load CREG	Load TM	NC	PC + 1	Hold	Hold	NC	
09	DEC	IF (cond) THEN DEC	PC + 1	Hold	DEC	NC	PC + 1	Hold	Hold	NC	
0F	GOTOTM	IF (cond) THEN GOTO TM (data)	TM	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	1
14	PSHPL	IF (cond) THEN PUSH, LOAD PL (data)	PC + 1	PC + 1	Load PL	NC	PC + 1	Hold	Hold	NC	
15	PSH	IF (cond) THEN PUSH	PC + 1	PC + 1	Hold	NC	PC + 1	Hold	Hold	NC	
16	PSHTM	IF (cond) THEN PUSH, LOAD TM (data)	PC + 1	PC + 1	Load TM	NC	PC + 1	Hold	Hold	NC	
17	PSHN	IF (cond) THEN PUSH, NESTED	PC + 1	PC + 1	Load SREG	NC	PC + 1	Hold	Hold	NC	
18	FORK	IF (cond) THEN GOTO PL (data) ELSE GOTO (SREG)	PL	Hold	Hold	Reset	SREG	Hold	Hold	NC	1
19	GOTOPL	IF (cond) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	1
1A	WAIT	IF (cond) THEN GOTO PL (data) ELSE WAIT	PL	Hold	Hold	Reset	PC	Hold	Hold	NC	1
1C	CALPL	IF (cond) THEN CALL PL (data)	PL	PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	1
1D	CALPLN	IF (cond) THEN CALL PL (data), NESTED	PL	PC + 1	Load SREG	Reset	PC + 1	Hold	Hold	NC	1
1E	CALTM	IF (cond) THEN CALL TM (data)	TM	PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	1
1F	CALTMN	IF (cond) THEN CALL TM (data), NESTED	TM	PC + 1	Load SREG	Reset	PC + 1	Hold	Hold	NC	1

Key:
- PC = Program Counter
- SREG = Stack Register
- CREG = Counter Register
- PL = Pipeline (data) Field
- TM (data) = Test Inputs Masked by DATA Field
- TM (mask) = Test Inputs Masked by MASK Field
- DEC = Decrement
- NC = No Change

Notes:

1. If COND = EQ and condition PASSES, reset EQ flag.
2. If COND = EQ and CREG ≠ 0, reset EQ flag.
3. If COND = EQ and CREG = 0, reset EQ flag.
4. Set EQ flag if CONST field = T*M.

INSTRUCTIONS DEPENDENT ON CREG

			CREG = 0				CREG ≠ 0				
Op-code	Mnemonic	Assembler Statement	PC MUX	SREG	CREG	EQ FLAG	PC MUX	SREG	CREG	EQ FLAG	Notes
08	LPPL	WHILE (CREG < > 0) LOOP TO PL (data)	PC + 1	Hold	Hold	NC	PL	Hold	DEC	Reset	2
0A	LPPLN	WHILE (CREG < > 0) LOOP TO PL (data), ELSE NEST	PC + 1	Hold	Load SREG	NC	PL	Hold	DEC	Reset	2
0B	GOTOPLZ	IF (CREG = 0) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
0C	DECPL	WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC	Hold	DEC	NC	
0E	DECTM	WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC	Hold	DEC	NC	

INSTRUCTIONS DEPENDENT ON TEST CONDITION AND CREG VALUE

					Condition Pass			Condition Fail				
Op-code	Mnemonic	Assembler Statement	CREG Content	PC MUX	SREG	CREG	EQ FLAG	PC MUX	SREG	CREG	EQ FLAG	Notes
1B	DECGOPL	IF (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT	≠ 0	PL	Hold	Hold	Reset	PC	Hold	DEC	NC	1
			= 0	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	

UNCONDITIONAL INSTRUCTIONS

Opcode	Mnemonic	Assembler Statement	PC MUX	SREG	CREG	EQ FLAG	Notes
0D	CONT	CONTINUE	PC + 1	Hold	Hold	NC	
10-13 (Binary 100XX)	CMP	CMP TM (mask) TO PL (constant)	PC + 1	Hold	Hold	Set	4

Key: PC = Program Counter
SREG = Stack Register
CREG = Counter Register
PL = Pipeline (data) Field
TM (data) = Test Inputs Masked by DATA Field
TM (mask) = Test Inputs Masked by MASK Field
DEC = Decrement
NC = No Change

Notes:

1. If COND = EQ and condition PASSES, reset EQ flag.
2. If COND = EQ and CREG ≠ 0, reset EQ flag.
3. If COND = EQ and CREG = 0, reset EQ flag.
4. Set EQ flag if CONST field = T*M.

Am29CPL151 SSR Diagnostics Option

As a programmable option, the Am29CPL151 FPC may be configured to contain Serial Shadow Register (SSR) diagnostics capability. SSR diagnostics is a simple, straightforward method of in-system testing to isolate problems down to the IC level.

The SSR diagnostics configuration activates a 32-bit-wide D-type register called a "shadow" register, on the pipeline register inputs. The shadow register can be serially loaded from the SDI pin, parallel loaded from the pipeline register, or held. The pipeline register can be loaded from the Program Memory in normal mode or from the shadow register during diagnostics. A redefinition of four device pins is required to control the different diagnostics functions. CC also functions as the Serial Data Input (SDI), $\overline{ZERO}$ becomes the Serial Data Output (SDO), P[7] becomes the diagnostic clock (DCLK), and P[6] becomes the diagnostic mode control (MODE). The various diagnostic and normal modes are shown in table 2.

Serially loading a test instruction into the shadow register and parallel loading the shadow register contents into the pipeline register forces execution of the test instruction. The test result can then be clocked into the pipeline register as in normal operation mode, parallel loaded into the shadow register, and serially shifted out for system diagnostics.

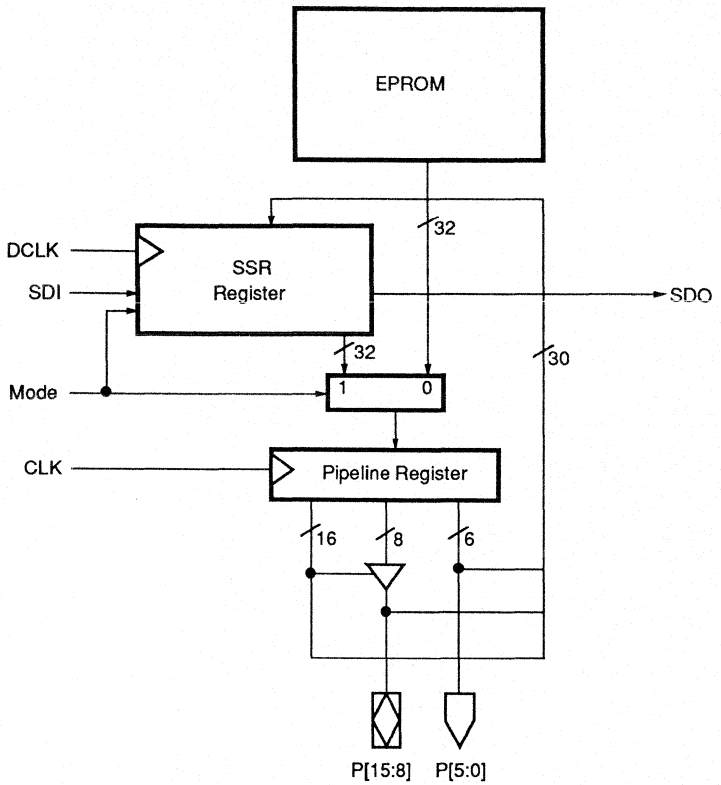
Table 2

Inputs				Outputs			Operation
SDI	MODE	DCLK	CLK	SDO	Shadow Register	Pipeline Register	
X	L	↑	H, L, ↓	S_0	$S_{i-1} \leftarrow S_i$ $S_{31} \leftarrow$ SDI	Hold	Serial Right-Shift Shadow Register
CC (Note 1)	L	H, L, ↓	↑	S_0	Hold	$P_i \leftarrow EPROM_i$	Normal Operation; Load Pipeline Register from EPROM
L	H	↑	H, L, ↓	L	$S_i \leftarrow P_i$	Hold	Load Shadow Register from Pipeline Register (Note 2)
X	H	H, L, ↓	↑	SDI	Hold	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	H, L, ↓	H	Hold	Hold	Hold Shadow Register

Notes:

1. During normal operation, this pin behaves as the CC input.
2. S7, S6 are undefined. S[15:8] load from the source driving pins P[15:8]. If P[31] in the microword is a ONE, S[15:8] are loaded from the pipeline register. If P[31] in the microword is a ZERO, S[15:8] are loaded from an external source.

Key:
- H = HIGH
- L = LOW
- X = Don't Care
- ↑ = LOW-to-HIGH transition
- ↓ = HIGH-to-LOW transition



10135-052A

Figure 3. SSR Diagnostics Logic

Erasure

In order to fully erase all memory locations, it is necessary to expose the memory array to a standard ultraviolet light source having a wavelength of 2537 angstroms. The minimum recommended dose (UV intensity x exposure time) is 15 Wsec/cm^2. For a UV lamp with a 12 mW/cm^2 power rating, the exposure time would be about 30 minutes. The device should be located one inch from the source in a direct line.

It should be noted that erasure will begin with exposure to light having wavelengths less than 4000 angstroms. To prevent exposure to sunlight or fluorescent lighting, an opaque label should be affixed over the window after programming.

OTP (One-Time Programmable) Am29CPL151 devices are available in plastic and are ideal for volume production. They can be inventoried unprogrammed and used with current software revisions; there is no window to be covered to prevent light from changing data.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		105	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		115	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 4.5 V to 5.5 V	25	pF
		Others		T_A = –55°C to +125°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 2)

No.	Parameter Symbol	Parameter Description		H-33 Min.	H-33 Max.	H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			12		14	ns
2		CLK to A[5:0]			28		36	ns
3		CLK to $\overline{ZERO}$			21		29	ns
4	t_S	T[3:0] to CLK, Registered		8		8		ns
5		T[5:4] to CLK, Registered		10		10		ns
6		T[5:0] to CLK, Asynchronous (Note 3)		30		40		ns
7		CC to CLK, Registered		8		8		ns
8		CC to CLK, Asynchronous (Note 3)		30		40		ns
9		$\overline{RESET}$ to CLK, Registered		12		12		ns
10		$\overline{RESET}$ to CLK, Asynchronous (Note 3)		26		40		ns
11	t_H	CLK to T[5:0]		0		0		ns
12	(Note 4)	CLK to CC		0		0		ns
13		CLK to $\overline{RESET}$		0		0		ns
14	t_{PZX}	CLK to P[15:8] Enable			30		40	ns
15	t_{PXZ}	CLK to P[15:8] Disable			30		40	ns
16	t_{WL}	CLK Width	LOW	12		16		ns
17	t_{WH}		HIGH	12		16		ns
18	t_P	CLK Period (Note 3)		30		40		ns
19	f_{MAX}	Maximum Frequency ($1/t_P$)		33		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (CC, T[5:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[5:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[5:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD

   CC to CLK setup time:
   CC (a) + (b) – (c) = CC to CLK setup time

   T[5:0] to CLK setup time:
   T[5:0] (a) + (b) – (c) = T[5:0] to CLK setup time

   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time
4. These hold time parameters are tested on a sample basis.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-33 Min.	H-33 Max.	H-25 Min.	H-25 Max.	Unit
SSR Configuration								
20	t_{PD}	Mode to SDO			20		30	ns
21		SDI to SDO			20		30	ns
22	t_{CO}	DCLK to SDO			28		36	ns
23	t_S	Mode to CLK		11		15		ns
24		Mode to DCLK		11		15		ns
25		SDI to DCLK		11		15		ns
26		P[15:8] to DCLK		11		15		ns
27	t_H	CLK to Mode		6		6		ns
28	(Note 1)	DCLK to Mode		0		0		ns
29		DCLK to SDI		0		0		ns
30		DCLK to P[15:8]		0		0		ns
31	t_{WL}	DCLK Width	LOW	15		20		ns
32	t_{WH}		HIGH	15		20		ns
33	t_P	DCLK Period		30		40		ns

Notes:

1. These hold time parameters are tested on a sample basis.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.3 V to V_{CC} + 0.3 V
DC Output or I/O Pin Voltage	–0.3 V to V_{CC} + 0.3 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices

Ambient Temperature (T_A) Operating in Free Air	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = 25°C, 125°C, and –55°C.

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		120	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		130	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 4.5 V to 5.5 V	25	pF
		Others		T_A = –55°C to +125°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			20	ns
2		CLK to A[5:0]			40	ns
3		CLK to $\overline{ZERO}$			30	ns
4	t_S	T[3:0] to CLK, Registered		10		ns
5		T[5:4] to CLK, Registered		12		ns
6		T[5:0] to CLK, Asynchronous (Note 3)		40		ns
7		CC to CLK, Registered		10		ns
8		CC to CLK, Asynchronous (Note3)		40		ns
9		$\overline{RESET}$ to CLK, Registered		16		ns
10		$\overline{RESET}$ to CLK, Asynchronous (Note 3)		40		ns
11	t_H	CLK toT[5:0]		0		ns
12	(Note 4)	CLK to CC		0		ns
13		CLK to $\overline{RESET}$		0		ns
14	t_{PZX}	CLK to P[15:8] Enable			40	ns
15	t_{PXZ}	CLK to P[15:8] Disable			35	ns
16	t_{WL}	CLK Width	LOW	15		ns
17	t_{WH}		HIGH	15		ns
18	t_P	CLK Period (Note 3)		40		ns
19	f_{MAX}	Maximum Frequency ($1/t_P$)		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (CC, T[5:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[5:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[5:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) - Measurement (c)
   CLK PERIOD:
   CLK (a) + (b) - (c) = CLK PERIOD
   T[5:0] to CLK setup time:
   T[5:0] (a) + (b) - (c) = T[5:0] to CLK setup time
   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) - (c) = $\overline{RESET}$ to CLK setup time
   CC to CLK setup time:
   CC (a) + (b) - (c) = CC to CLK setup time
4. These hold time parameters are tested on a sample basis.

SWITCHING CHARACTERISTICS over MILITARY operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
SSR Configuration						
20	t_{PD}	Mode to SDO			30	ns
21		SDI to SDO			30	ns
22	t_{CO}	DCLK to SDO			30	ns
23	t_S	Mode to CLK		25		ns
24		Mode to DCLK		25		ns
25		SDI to DCLK		25		ns
26		P[15:8] to DCLK		25		ns
27	t_H (Note 1)	CLK to Mode		6		ns
28		DCLK to Mode		0		ns
29		DCLK to SDI		0		ns
30		DCLK to P[15:8]		0		ns
31	t_{WL}	DCLK Width	LOW	25		ns
32	t_{WH}		HIGH	25		ns
33	t_P	DCLK Period		60		ns

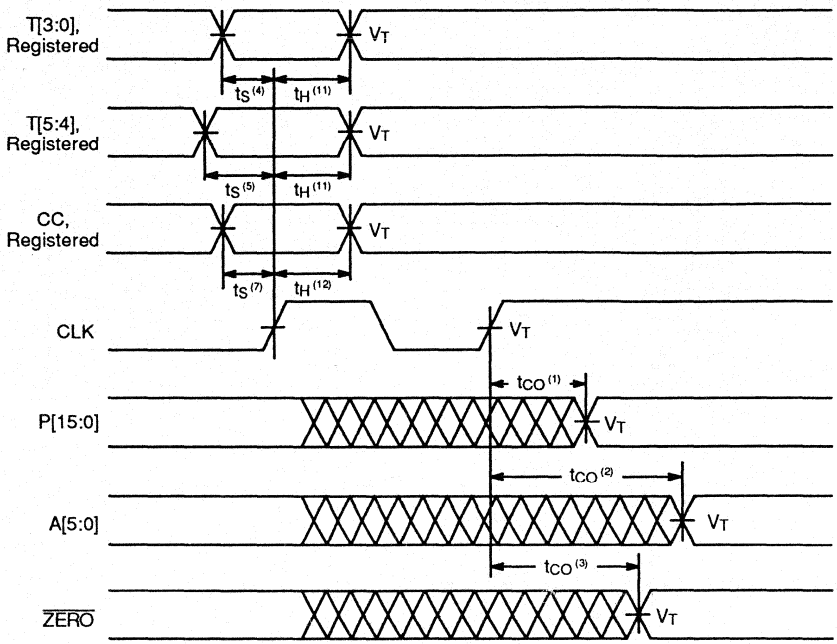
Notes:

1. These hold time parameters are tested on a sample basis.

3

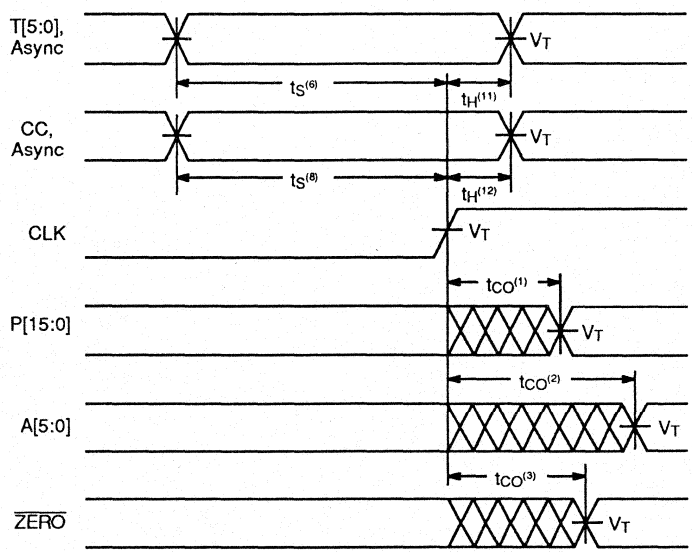
SWITCHING WAVEFORMS

Normal Configuration



10135-055A

Registered Test Inputs

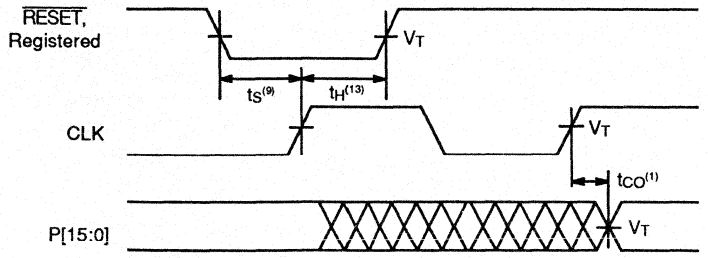


10135-056A

Asynchronous Test Inputs

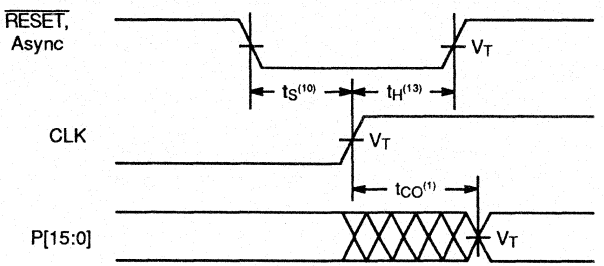
SWITCHING WAVEFORMS (Continued)

Normal Configuration



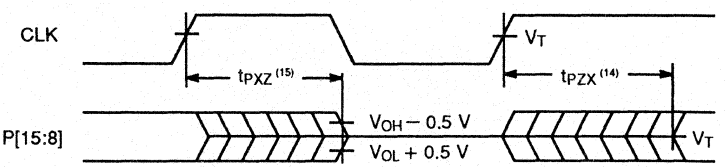
10135-057A

Registered $\overline{\text{RESET}}$



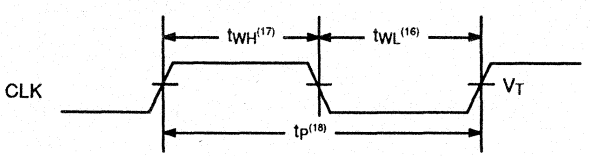
10135-058A

Asynchronous $\overline{\text{RESET}}$



10135-059A

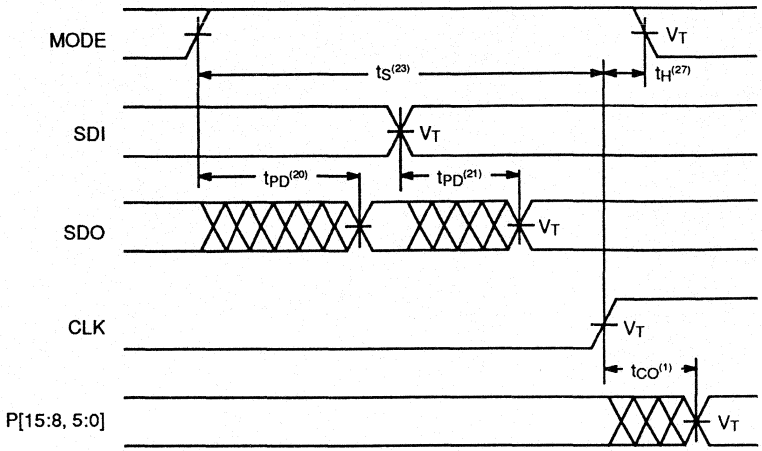
CLK to Output Disable/Enable



10135-060A

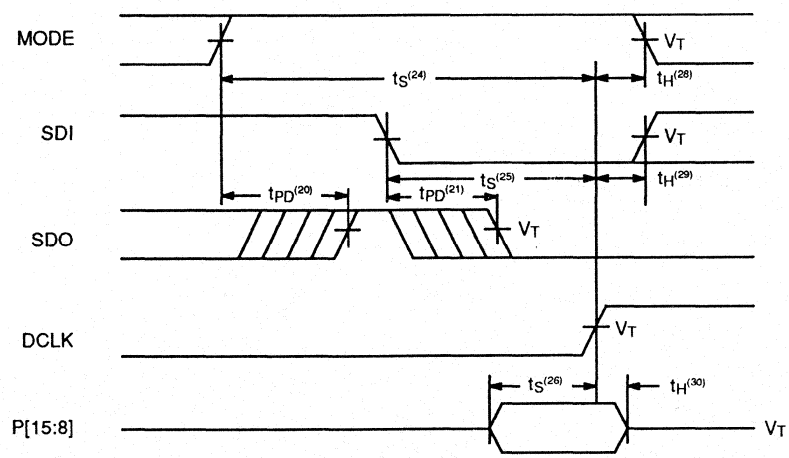
Clock Width/Period

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10135-061A

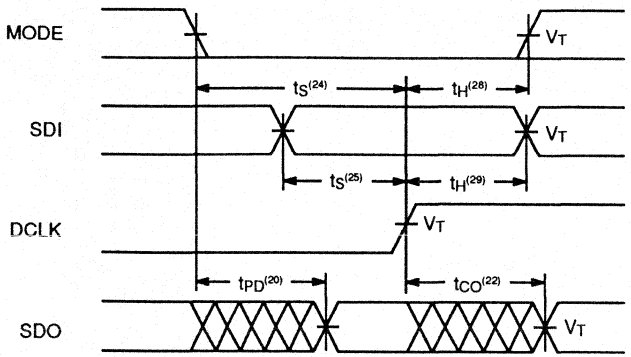
Load Pipeline Register from Shadow Register



10135-062A

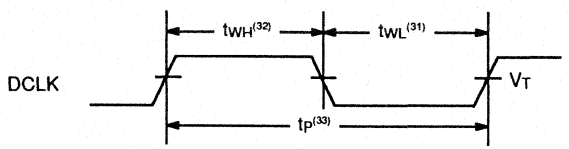
Load Shadow Register from Pipeline Register and/or Pins

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10135-063A

Shift Shadow Register



10135-064A

DCLK Width/Period

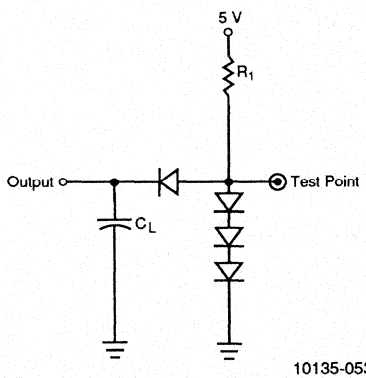
3

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

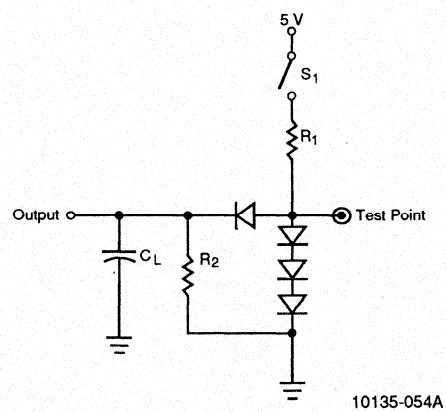
KS000010-PAL

SWITCHING TEST CIRCUIT



10135-053A

Three-State Outputs



10135-054A

Two-State Outputs

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	667 Ω	5 kΩ	667 Ω	5 kΩ	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Note:

Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω: t_r ≤ 2.5 ns.

TEST PHILOSOPHY AND METHODS

The following eight points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

7. Threshold Testing

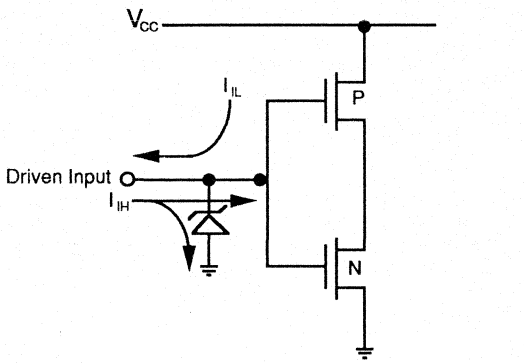
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.

8. AC Testing

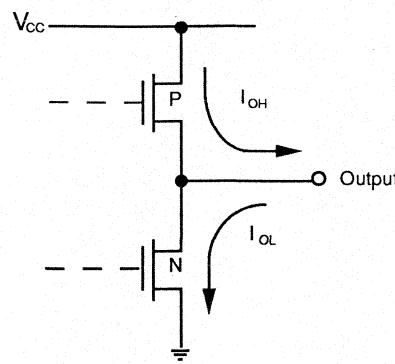
   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



10135-050A

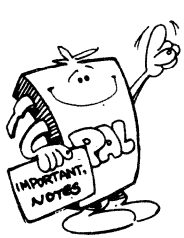


10135-051A

Thermal Impedance Values (θ_{JA}), Typical

28-Pin Plastic SKINNYDIP (PD3028)	50°C/W
28-Pin Windowed Ceramic SKINNYDIP (CDE028)	40°C/W
28-Pin Plastic Leaded Chip Carrier (PL 028)	55°C/W
28-Pin Windowed Ceramic Leadless Chip Carrier (CLV028)	55°C/W

3



Preliminary | COM'L: -25/30 MIL: -25

Am29CPL154H-25/30

CMOS 512-Word Field-Programmable Controller (FPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements complex state machines**
- **High-speed, low-power CMOS EPROM technology**
- **Functional upgrade from the Am29CPL151**
- **Eight conditional inputs (each can be registered as a programmable option), 16 outputs**
- **Up to 30-MHz maximum frequency**
- **512-word by 36-bit CMOS EPROM**
- **Space-saving 28-pin OTP plastic SKINNYDIP® and PLCC packages and windowed ceramic SKINNYDIP package**
- **28 instructions**
  - Conditional branching, conditional looping, conditional subroutine call, multiway branch

GENERAL DESCRIPTION

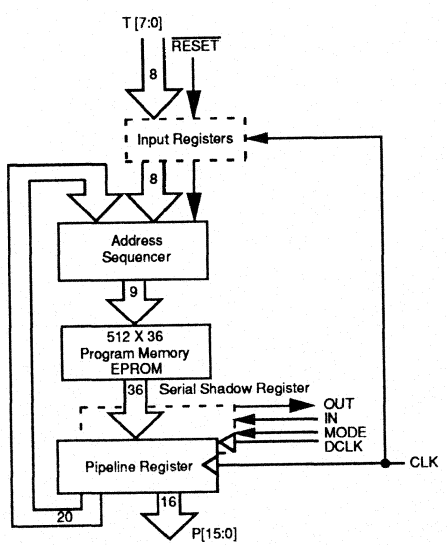
The Am29CPL154 is a CMOS, single-chip Field Programmable Controller (FPC). It allows implementation of complex state machines and controllers by programming the appropriate sequence of instructions. Jumps, loops, and subroutine calls, conditionally executed based on the test inputs, provide the designer with powerful control flow primitives.

Intelligent control may be distributed throughout the system by using FPCs to control various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic, and bus control units. An address sequencer, the heart of the FPC, provides the address to an internal 512-word by 36-bit EPROM.

The Am29CPL154 is manufactured in CMOS technology and offers a space-saving 300-mil SKINNYDIP package. A pin-compatible smaller FPC is offered as the Am29CPL151 with a 64 x 32 memory.

This UV-erasable and reprogrammable device utilizes proven floating-gate CMOS EPROM technology to ensure high reliability, easy programming, and better than 99.9% programming yields. The Am29CPL154 is offered in both windowed and One-Time Programmable (OTP) packages. OTP plastic SKINNYDIP and PLCC devices are ideal for volume production.

SIMPLIFIED BLOCK DIAGRAM



10136-001A

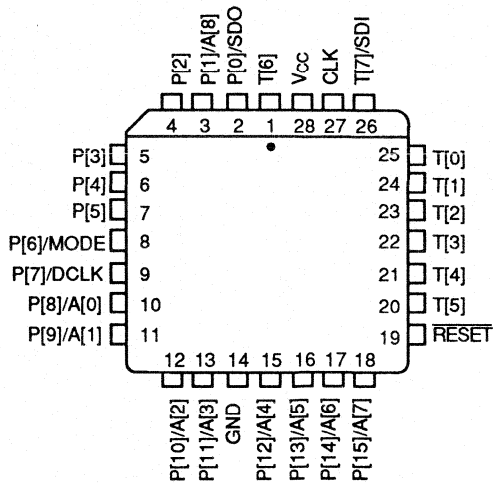
Publication # 10136 Rev. C Amendment /0
Issue Date: January 1989

CONNECTION DIAGRAMS
Top View

SKINNYDIP

10136-002A

PLCC/LCC

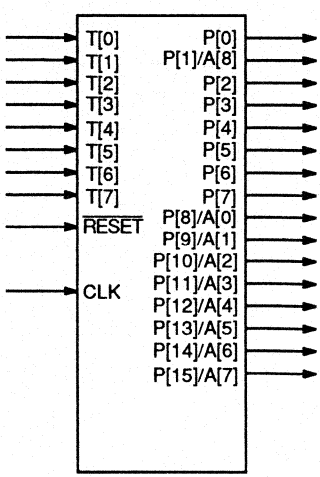


10136-003A

Note:
Pin 1 is marked for orientation.

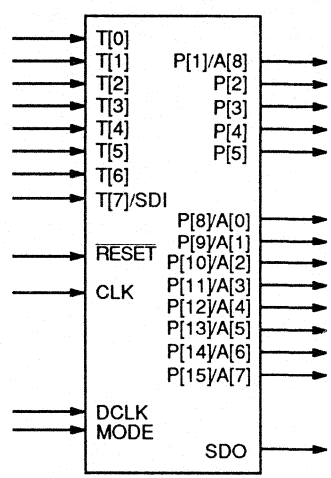
LOGIC SYMBOLS

Normal Configuration



10136-004A

SSR® Diagnostics Configuration

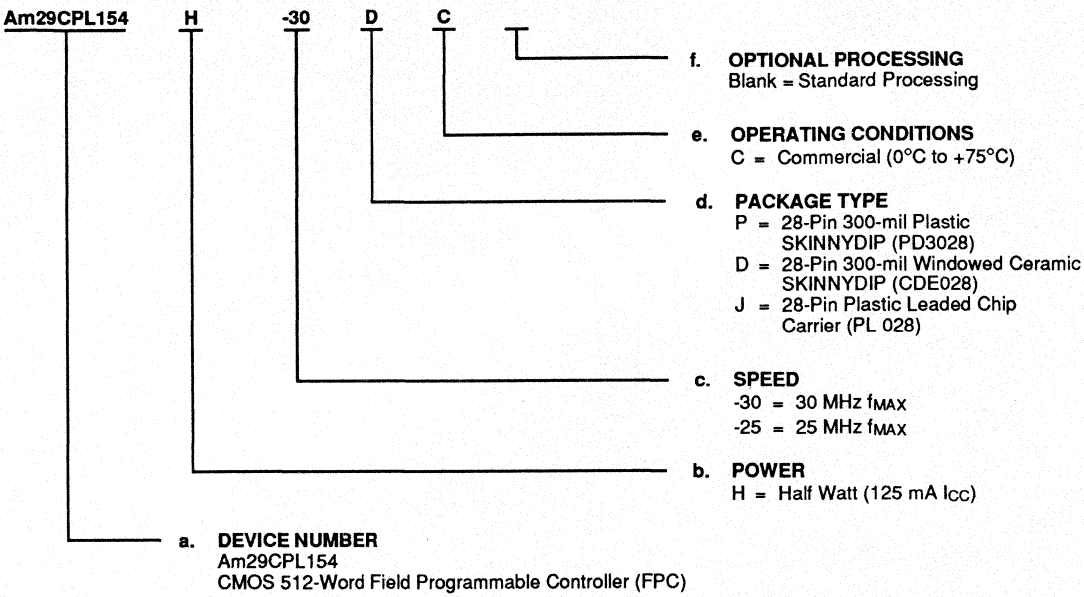


10136-005A

ORDERING INFORMATION
Commercial Products

AMD products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Package Type
e. Operating Conditions
f. Optional Processing



Valid Combinations	
Am29CPL154H-30	PC, DC, JC
Am29CPL154H-25	

Valid Combinations

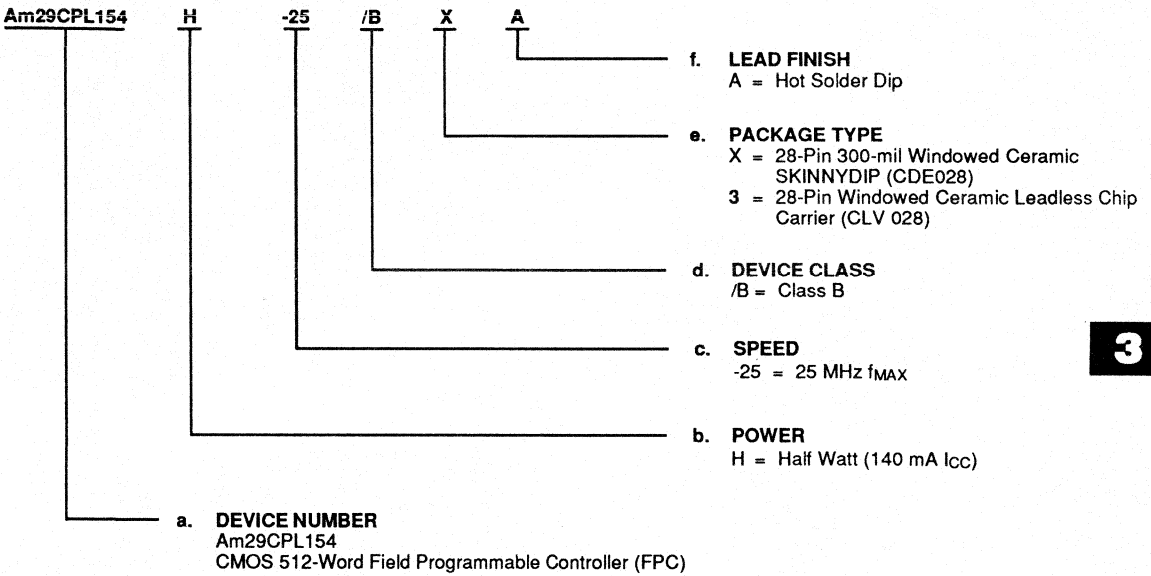
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power
c. Speed
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
Am29CPL154H-25	/BXA, /B3A

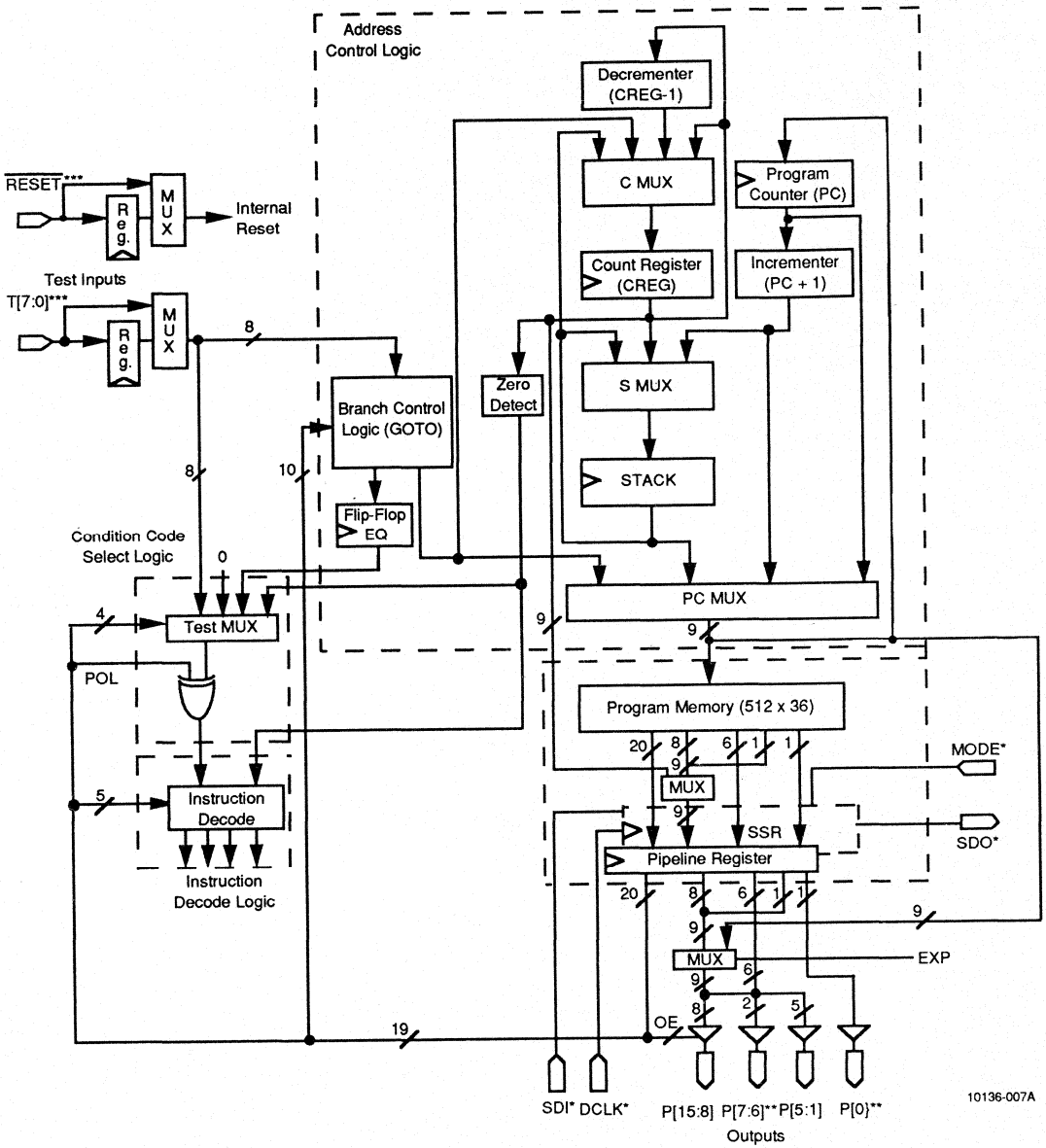
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.



* These pins available only in SSR mode.
** These pins available only in normal mode.
*** Each of the T[7:0] and $\overline{\text{RESET}}$ inputs can be individually registered or left unregistered as a programmable option.

10136-007A

Figure 1. Am29CPL154 Detailed Block Diagram

PIN DESCRIPTION

CLK

Clock Input

The rising edge of the clock latches the program counter, count register (CREG), subroutine register (SREG), pipeline register, and EQ flag. The rising edge of the clock also latches the test input registers and the $\overline{\text{RESET}}$ register if their respective configuration bits are set to enable internal synchronizing registers.

P[15:8]/A[7:0]

Outputs

The upper eight general-purpose control outputs are enabled by the OE signal from the pipeline register. When OE is HIGH, P[15:8] are enabled and when LOW, P[15:8] are disabled.

A controller Expansion (EXP) cell can be programmed to set pins P[1] and P[15:8] to output the program address A[8] and A[7:0] from the PC MUX. These can be used to address external registered memories to provide more control outputs.

The contents of the internal count register (CREG) can also be routed to the control output pins P[1] and P[15:8], using the OUTPUT instruction. Thus, the control outputs can be changed dynamically.

P[7:0] [DCLK, MODE, SDO]

Outputs

The lower eight general-purpose control outputs are permanently enabled. In the SSR diagnostic configuration, P[7] becomes the diagnostic clock input DCLK, P[6] becomes the diagnostic control input MODE, and P[0] becomes the serial Data Output [SDO].

$\overline{\text{RESET}}$

Optionally Registered $\overline{\text{Reset}}$ Input; Active LOW

When the reset input is LOW, the output of the PC MUX is forced to the uppermost program address (511). On the next rising edge of the clock, this address (511) is loaded into the program counter; the instruction at location 511 is loaded into the pipeline register, and the EQ flag is cleared. A programmable configuration bit allows the option of making this a registered input. If $\overline{\text{RESET}}$ is internally registered, the first rising edge of the clock latches it. On the next rising edge of the clock, the EQ flip-flop is cleared and the contents of memory location 511 are loaded into the pipeline register. The default state of this input is registered.

T[7:0] [SDI]

Optionally Registered Test Inputs

In conditional instructions, the TEST inputs can be used as individual condition codes selected by the TEST field in the pipeline register. The T[7:0] inputs can also be used as a branch address when performing a program branch or as a count value to be loaded into the CREG. When this is done, a ninth bit from the microword is added as the MSB of the test inputs to yield a nine-bit value. Each of these inputs has an EPROM bit associated with it. This bit may be programmed such that the corresponding input becomes an unregistered input. The default state of these inputs is registered. In SSR diagnostics mode, T[7] becomes the Serial Data Input (SDI).

FUNCTIONAL DESCRIPTION

Figure 1, the detailed block diagram of the Am29CPL154, shows logic blocks and interconnecting buses that permit parallel performance of different operations in a single instruction. The FPC consists of four main logic blocks: the program memory, address control logic, condition code selection logic, and instruction decode. A fifth optional block is the Serial Shadow Register (SSR).

The program memory contains the user-defined instruction flow and output sequence. The address control logic addresses the program memory. This control logic supports high-level instruction functions including conditional branches, subroutine calls and returns, loops, and multiway branches. The condition code selection logic selects the condition code input to be tested when a conditional instruction is executed. The polarity of the selected condition code input is controlled by the POL bit in the microword. The instruction decode generates the control signals necessary to perform the instruction specified by the instruction part (P[35:16]) of the microword. The SSR enables in-system testing to isolate problems down to the IC level.

Program Memory

The FPC program memory is a 512-word by 36-bit EPROM with a 36-bit pipeline register at its output. The upper 20 bits (P[35:16]) of the pipeline register are internal to the FPC and form the instruction to control address sequencing. The format for instructions is: a one-bit synchronous Output Enable OE, a five-bit OPCODE, a one-bit test polarity select POL, a four-bit TEST condition select field, and a nine-bit immediate DATA field. The DATA field is used to provide branch addresses, test input masks, and counter values.

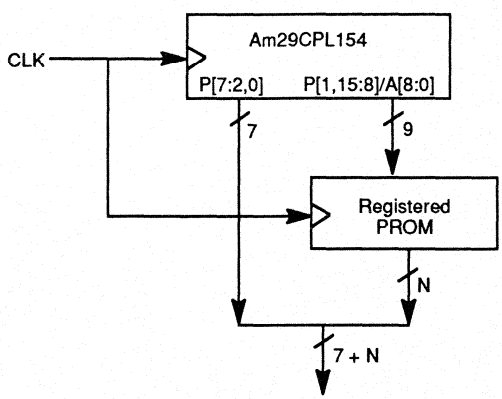
The lower 16 bits (P[15:0]) of the pipeline register are brought out as user-defined, general-purpose control outputs. The upper eight control outputs (P[15:8]) are disabled when OE is programmed as a LOW. The lower eight control bits (P[7:0]) are always enabled.

Outputs P[1] and P[15:8] will contain the next instruction address when the optional bit EXP is set. The contents of the count register are also available at P[1] and P[15:18] by using the OUTPUT instruction regardless of whether the EXP bit is set.

Controlling External PROM

By programming the EXP bit, PC MUX is output over pins P[1,15:8]/A[8:0]. This feature can be used to extend the width of the output control word when external registered memories are used. In the diagram below, the Am29CPL154 controls external registered PROMs to provide an output control word (7 + N) bits wide (where N is the bit width of the PROMs).

When the OUTPUT instruction is executed, the CREG contents are output over pins P[1], P[15:8]/A[8], A[7:0] on the following cycle. Consequently, if the CREG contents must be read after programming the EXP cell, the system design should be modified to handle this exception.



10136-006A

Figure 2. Controlling External PROM

Address Control Logic

The address control logic consists of four smaller logic blocks. These are:

PC GRP – Program counter multiplexer (PCMUX), program counter register (PC) and combinatorial incrementer (PC + 1)

STACK – 17-word by 9-bit-wide stack with subroutine mux (S MUX)

CNTR – Count register (CREG) with counter mux (C MUX), combinatorial decrementer (CREG–1), and zero detect

GOTO – Multifunction branch control logic

PC GRP

The PC GRP consists of a 4:1 multiplexer, a program counter (PC) register, and a 9-bit combinatorial incrementer (PC + 1). It selects the PC, PC + 1, the branch address, or the top of stack as the next instruction address input to the program memory and the PC.

When $\overline{\text{RESET}}$ is internally registered, the first clock edge after $\overline{\text{RESET}}$ goes LOW latches $\overline{\text{RESET}}$ internally. The next clock edge loads the contents of location 511 decimal into the instruction-pipeline register and clears the EQ flag. A programmable configuration bit allows the option of bypassing the synchronizing register. In this case, after $\overline{\text{RESET}}$ goes LOW, the output of the PC MUX is forced to all "1"s (address 511 decimal) during the setup time, and the first clock edge loads the contents of location 511 decimal into the instruction-pipeline register and clears the EQ flag. Note: by default, the $\overline{\text{RESET}}$ input is registered.

STACK

This 17-deep, 9-bit-wide stack block consists of a 3:1 multiplexer (S MUX) that stores the data into the topmost location of the stack. The STACK register is incremented by one after an item is written onto the STACK (post-incremented) and decremented by one before an item is read from the STACK (pre-decremented). The S MUX chooses from three sources: PC +1 , count register, and the top of the stack (for holding). PC + 1 is the input source when doing subroutine calls. PC MUX is the output destination when a return-from-subroutine instruction is performed. The PSHCNTR and POPCNTR instructions can be used for nested counts up to the depth of the STACK. Table 1 shows how the stack operates when more than 17 values are pushed. Table 2 shows how the stack operates when more than 17 values are popped.

CNTR

The CNTR block consists of a nine-bit, four-to-one multiplexer (C MUX), driving a nine-bit register (CREG); a six-bit combinatorial decrementer (CREG-1); and a zero-detection circuit. The CNTR logic block is typically used for timing functions and iterative loop counting.

The CMUX has the following input sources: top of stack, the branch-logic output, CREG – 1, and the CREG (for holding).

GOTO

The GOTO logic block serves three functions:

1. It provides a nine-bit count value from the DATA field in the pipeline register (P[24:16]) or from the TEST inputs T[7:0] masked by the DATA field P[23:16]. This is represented by T*M.
2. It provides a branch address from the DATA field in the pipeline register P[24:16] or from the TEST inputs T[7:0] masked by the 8 LSBs of the DATA field P[23:16]. This is represented by T*M. The MSB or ninth bit of the branch address will be the MSB of the DATA field.
3. It compares T[7:0] masked by the MASK field P[23:16], called T*M, to the CONSTANT field from the pipeline register P[31:24]. If a match occurs, the EQ flip-flop is set. EQ remains unchanged if there is no match. Constant field bits that correspond to masked test bits must be zero.

The EQ flag can be tested by the condition code selection logic. Multiple tests of any group of T inputs in a manner analogous to sum-of-products can be performed since a no-match comparison does not reset the EQ flag. Any conditional branch on EQ will reset the EQ flag. Conditional returns on EQ will not change the EQ flag. $\overline{\text{RESET}}$ input LOW will reset the EQ flag.

Note: A zero in the MASK field blocks the corresponding bit in the TEST field; a one activates the corresponding bit.

The constant field bits that correspond to masked test field bits must be zero. A zero is substituted for masked test field bits. The "POL" bit is a "don't care" when using test inputs to load registers.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Condition Code Selection Logic

The condition code selection logic consists of a 16:1 multiplexer. The 16 condition inputs are the eight test bits, the EQ flag, CREG ZERO status, and six UNCOND test conditions connected to zero for the unconditional mode. The TEST field in the pipeline register (P[28:25]) selects one of the 16 conditions. If one of the UNCOND is chosen, and the POL bit is a one, the instruction is executed with a "forced PASS" condition. If one of the UNCOND is chosen, and the POL bit is zero, the instruction is executed with a "forced FAIL" condition. See opcode descriptions for more details.

The polarity bit POL in the instruction allows the user to test for either a pass or fail condition. Refer to Table 3 for details.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Instruction Decode

The instruction decoder is a PLA that generates the control for 28 different instructions. The decoder inputs include the OPCODE field P[34:30], the zero detection flag from the CNTR, and the selected test condition code from the condition code selection logic.

Operational Modes

The Am29CPL154 operates as a nine-bit microcontroller in normal mode, and there are several configuration bits that can be programmed to modify this normal operation. The EXP bit allows the nine program address lines from the PC MUX to be output on the output pins (P[1,15:8]) so that a user can expand the width of the control lines by using external registered memories. The SSR bit allows on-chip diagnostic capabilities for in-system testing. The remaining bits serve to individually select whether the input pins will be synchronized or not. The default setting of these bits (unprogrammed,1) will cause each pin to be synchronized, and so programming a given bit (to 0) will cause that corresponding input to become internally unsynchronized.

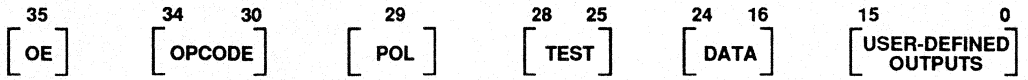
TABLE 1.

STACK LOCATION	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH	PSH
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
2	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
3	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
4	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
5	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
6	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13	14
7	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12	13
8	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11	12
9	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10	11
10	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9	10
11	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8	9
12	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7	8
13	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6	7
14	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5	6
15	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4	5
16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3	4
17	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	2	3

TABLE 2.

STACK LOCATION	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	POP
1	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17
2	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16
3	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15
4	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14
5	15	14	13	12	11	10	9	8	7	6	5	4	3	10	17	16	15	14	13
6	14	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12
7	13	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11
8	12	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10
9	11	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9
10	10	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8
11	9	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7
12	8	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6
13	7	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5
14	6	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
15	5	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
16	4	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18
17	3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	18	17

Am29CPL154 General Instruction Format



10136-008A

WHERE:

OE = Synchronous Output Enable for P[15:8].
OPCODE = A five-bit opcode field for selecting one of the 27 single-data-field instructions.
POL = A one-bit test condition polarity select (refer to Table 3).
TEST = A four-bit test condition select.

TEST[28:25]	UNDER TEST
0000	T [0]
0001	T [1]
0010	T [2]
0011	T [3]
0100	T [4]
0101	T [5]
0110	T [6]
0111	T [7]
1000	EQ
1001	CREG ZERO
1010-1111	UNCONDITIONAL [0]

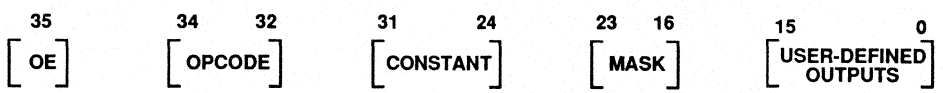
DATA = A nine-bit conditional branch address, test input mask, or counter value field designated as PL in instruction mnemonics.

3

Table 3

Input Condition Being Tested	POL	Test Result
0	0	Fail
0	1	Pass
1	0	Pass
1	1	Fail

Am29CPL154 Comparison Instruction Format



10136-009A

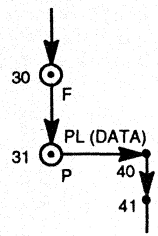
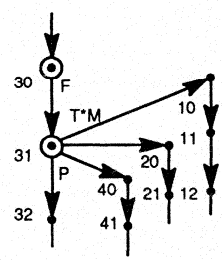
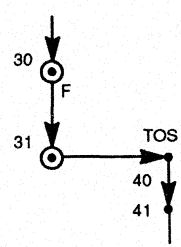
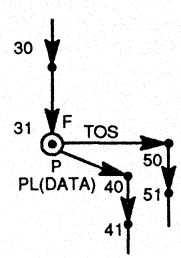
WHERE:

OE = Synchronous Output Enable for P[15:8].
OPCODE = Compare instruction (binary 100).
CONSTANT = An eight-bit constant for equal-to comparison with T*M.
MASK = An eight-bit mask field for masking the incoming T[7:0] inputs.

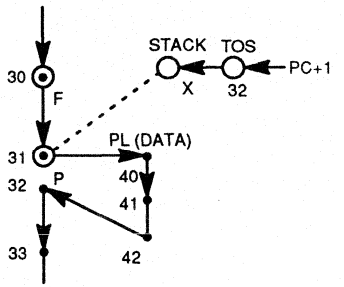
Am29CPL154 INSTRUCTION SET DEFINITION

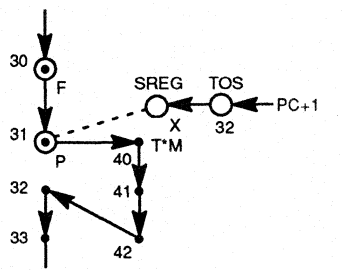
• = Other instruction
⊙ = Instruction being described
○ = Register in part

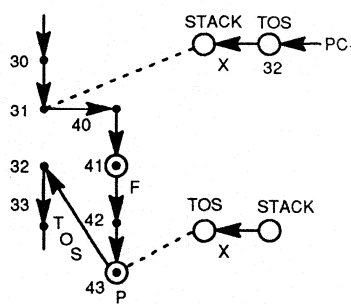
P = Test Pass
F = Test Fail
X,Y are arbitrary values in the CREG or STACK

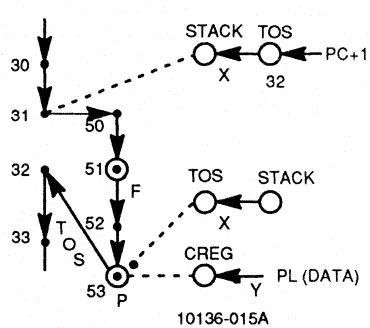
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
19	GOTOPL	**IF (cond) THEN GOTO PL (data)** Conditional branch to the address in the PL (DATA field). The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10135-009A	If (cond = true) Then PC = PL(data) Else PC = PC + 1
IF	GOTOTM	**IF (cond) THEN GOTO TM (data)** Conditional branch to the address defined by the T*M (T[7:0] under bitwise mask from the 8 LSBS of the DATA field). This instruction is intended for multiway branches. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.	 10135-011A	If (cond = true) Then PC = T*M Else PC = PC + 1
03	GOTOSTK	**IF (cond) THEN GOTO (STACK)** Conditional branch to the address at the top of the stack, or else continue. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-010A	If (cond = true) Then PC = TOS Else PC = PC + 1
18	FORK	**IF (cond) THEN GOTO PL (data) ELSE GOTO (STACK)** Conditional branch to the address in the PL (DATA field) or the TOS. A branch to PL is taken if the condition is true and a branch to TOS if false. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-011A	If (cond = true) Then PC = PL(data) Else PC = TOS

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

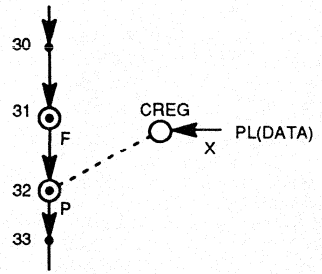
1C	CALPL	**IF (cond) THEN CALL PL (data)** Conditional jump to subroutine at the address in the PL (DATA field). The PC + 1 is pushed into the TOS as the return address. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is exe cuted with a forced FAIL condition if the test field is UNCOND and POL = 0.		If (cond = true) Then
				STACK = TOS
				TOS = PC + 1
				PC = PL(data)
				Else
				PC = PC + 1
				10136-012A

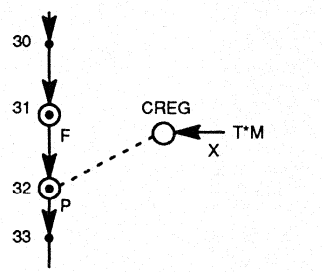
1E	CALTM	**IF (cond) THEN CALL TM (data),** Conditional jump to subroutine at the address specified by the T*M (T[7:0] under bitwise mask from the 8 LSBs of the DATA field). The PC + 1 is pushed into the TOS as the return address. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.The MSB of the branch address will be the MSB of the DATA field.		If (cond = true) Then
				STACK = TOS
				TOS = PC + 1
				PC = T*M
				Else
				PC = PC + 1
				10136-013A

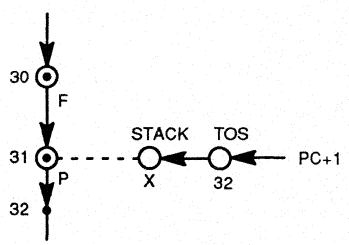
02	RET	**IF (cond) THEN RET** Conditional return from subroutine. The TOS provides the return from subroutine address and the stack is popped. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.		If (cond = true) Then
				PC = TOS
				TOS = STACK
				Else
				PC = PC + 1
				10136-014A

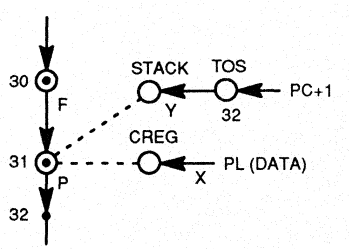
00	RETPL	**IF (cond) THEN RET, LOAD PL (data)** Conditional return from subroutine and load the CREG from the PL (DATA field). The TOS provides the return from subroutine address and the STACK is popped. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	
			10136-015A
				If (cond = true) Then
				PC = TOS
				TOS = STACK
				CREG = PL(data)
				Else
				PC = PC + 1
				10136-015A

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

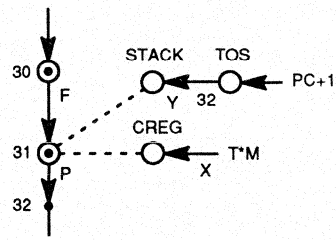
04	LDPL	**IF (cond) THEN LOAD PL (data)** Conditional load the CREG from the PL (DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10135-017A	If (cond = true) Then
				CREG = PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

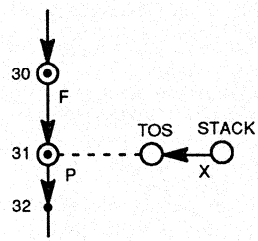
06	LDTM	**IF (cond) THEN LOAD TM (data)** Conditional load the CREG from the T*M (T[7:0] inputs under bitwise mask from the 8 LSBS of the DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.	 10135-019A	If (cond = true) Then
				CREG = T*M
				PC = PC + 1
				Else
				PC = PC + 1

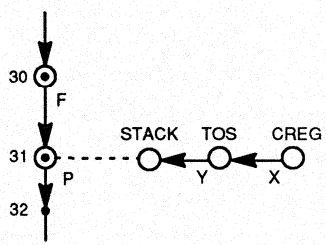
15	PSH	**IF (cond) THEN PUSH** Conditional push the PC + 1 into the TOS. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-017A	If (cond = true) Then
				STACK = TOS
				TOS = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

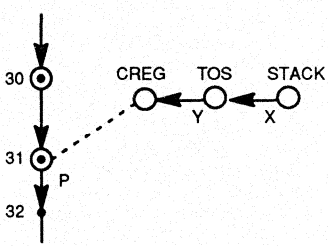
14	PSHPL	**IF (cond) THEN PUSH, LOAD PL (data)** Conditional push the PC + 1 into the TOS and load the CREG from the PL (DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.	 10136-018A	If (cond = true) Then
				CREG = PL(data)
				STACK = TOS
				TOS = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

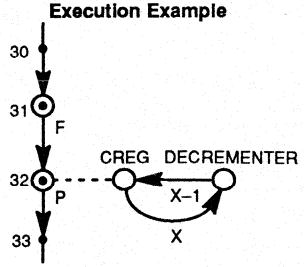
16	PSHTM	**IF (cond) THEN PUSH, LOAD TM (data)**
		Conditional push the PC + 1 into the TOS and load the CREG from the T*M (T[7:0] under bitwise mask from the 8 LSBs of the DATA field). The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.
			
			10136-019A
				If (cond = true) Then
				CREG = T*M
				STACK = TOS
				TOS = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

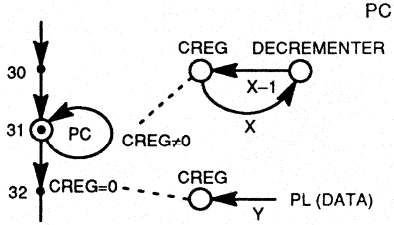
07	POP	**IF (cond) THEN POP**
		Conditional Pop the TOS. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0.
			
			10136-020A
				If (cond = true) Then
				TOS = STACK
				PC = PC + 1
				Else
				PC = PC + 1

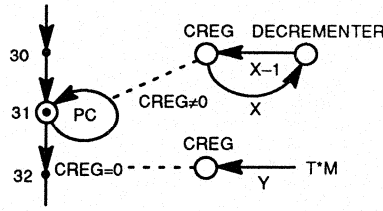
05	PSHCNTR	**IF (cond) THEN PUSH (CREG)**
		Conditional push CREG contents to top of stack. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10136-021A
				If (cond = true) Then
				STACK = TOS
				TOS = CREG
				PC = PC + 1
				Else
				PC = PC + 1

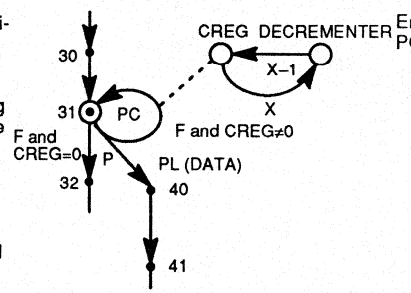
17	POPCNTR	**IF (cond) THEN POP TO (CREG)**
		Conditional pop TOS into CREG. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0.
			
			10136-022A
				If (cond = true) Then
				CREG = TOS
				TOS = STACK
				PC = PC +1
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

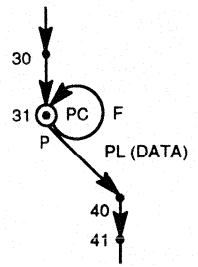
0B	DEC	**IF (cond) THEN DEC**
		Conditional decrement of the CREG. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10135-029A
				If (cond = true) Then
				CREG = CREG –1
				PC = PC + 1
				Else
				PC = PC + 1

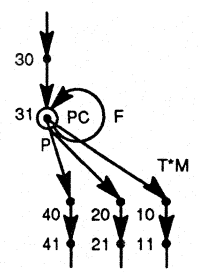
0C	DECPL	**WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the PL (DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from PL. This instruction does not depend on the pass/fail condition.
			
			10135-030A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = PL(data)
				PC = PC + 1

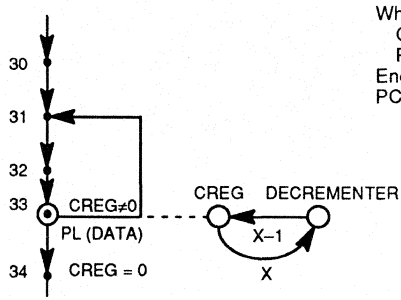
0E	DECTM	**WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the T*M (T[7:0] under bitwise mask from the 8 LSBs of the DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while the CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from T*M. This instruction does not depend on the pass/fail condition. The MSB of the branch address will be the MSB of the DATA field.
			
			10135-031A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PC
				End While
				CREG = T*M
				PC = PC + 1

1D	DECGOPL	**If (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT**
		Conditional Hold/Count. The current instruction will be refetched and the CREG decremented until the condition under test becomes true or the counter is equal to zero. If the condition becomes true, a branch to the address in the PL (DATA field) is executed. If the counter becomes zero without the condition becoming true, a CONTINUE is executed. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10135-032A
				While (cond = false)
				If (CREG < > 0)
				CREG = CREG –1
				PC = PC
				Else
				PC = PC + 1
				End While
				PC = PL (data)

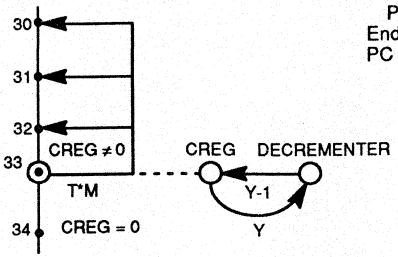
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

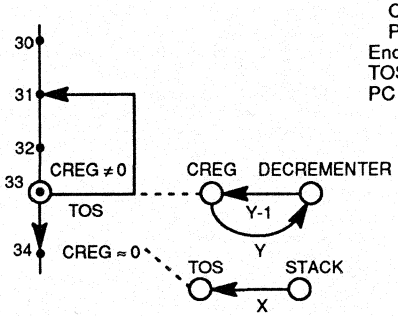
1A	WAITPL	**IF (cond) THEN GOTO PL (data) ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When true, a branch to the address in the PL (DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition if the test field is UNCOND and POL = 0.
			
			10135-033A
				If (cond = true) Then
				PC = PL (data)
				Else
				PC = PC

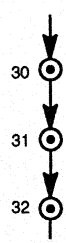
1B	WAITTM	**IF (cond) THEN GOTO TM (data), ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When the condition is true, a branch to the T*M address (T[7:0] under bitwise mask from the eight LSBs of the DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0. The MSB of the branch address will be the MSB of the DATA field.
			
			10136-023A
				If (cond = true) Then
				PC = T*M
				Else
				PC = PC

08	LPPL	**WHILE (CREG < > 0) LOOP TO PL (data)**
		Conditional loop to the address in the PL (DATA field). This instruction is intended to be placed at the bottom of an iterative loop. If the CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the loop) is executed. If the CREG is equal to zero, looping is complete and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10135-034A
				While (CREG < > 0)
				CREG = CREG –1
				PC = PL (data)
				End While
				PC = PC + 1

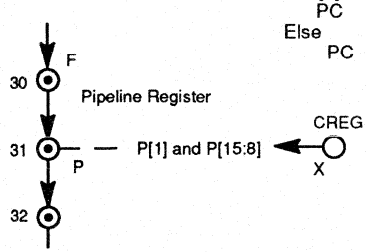
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

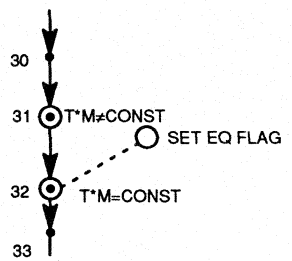
0A	LPTM	**WHILE (CREG < > 0) LOOP TO TM (data)**
		Conditional loop to the address T*M (T[7:0] under bitwise mask from the eight LSBs of the DATA field). This instruction should be placed at the bottom of an iterative loop. If CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the address specified by T*M (top of the loop) is executed. If CREG is equal to zero, looping is complete and the next sequential instruction is executed. This does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero. The MSB of the branch address will be the MSB of the DATA field.
			
			10136-024A
				While (CREG < > 0)
				CREG = CREG –1
				PC = T*M
				End While
				PC = PC + 1

0F	LPSTK	**WHILE (CREG < > 0) LOOP TO (STACK)**
		Conditional loop to the address in the TOS. If CREG ≠ 0, the CREG is decremened and a branch to the TOS address is executed. If the CREG = 0, looping is complete, the stack is popped, and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10136-025A
				While (CREG < > 0)
				CREG = CREG –1
				PC = TOS
				End While
				TOS = STACK
				PC = PC + 1

0D	CONT	**CONTINUE** The next sequential instruction is fetched unconditionally. This instruction can be used to reset the EQ flag by selecting EQ in the TEST field.	 10135-036A	PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

01	OUTPUT	**IF (cond) THEN OUTPUT**
		The CREG contents will be output on pins P[1] and P[15:8] during the next clock cycle. Care should be taken to ensure that the outputs are enabled for the next sequential instruction by setting the microcode bit OE = 1. The instruction is executed with a forced PASS condition, if the test field is UNCOND and POL = 1. The instruction is executed with a forced FAIL condition, if the test field is UNCOND and POL = 0.
			
			10136-026A
				If (cond = ture) Then
				P[1] and P[15:8] = CREG
				PC = PC + 1
				Else
				PC = PC + 1

10–13 (100XX binary)	CMP	**CMP TM (mask) TO PL (constant)** This instruction performs bitwise Exclusive-OR of T*M (T[7:0] under bitwise mask from the MASK field) with CONSTANT (P[31:24]). If T*M equals CONSTANT, the EQ flag is set to one, which may be branched on in a following instruction. If not equal, the EQ flag is unaffected. This allows sequences of compares, in a manner analogous to sum-to-products, to be performed which can be followed by a single conditional branch if one or more of the comparisons are true. Note: The EQ flag is set to zero on reset or when EQ is selected as the test condition in a branch. Conditional returns on EQ leave the flag unchanged. Constant field bits that correspond to masked test field bits must be zero. This instruction does not depend on the pass/fail condition.	 10135-037A	Compare T*M and CONSTANT EQ = ((T [7:0] .AND. MASK) .XNOR. CONSTANT) .OR. EQ PC = PC + 1

3

INSTRUCTIONS BASED ON TEST CONDITIONS

Op-code	Mnemonic	Assembler Statement	Condition Pass				Condition Fail				Notes
			PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	
00	RETPL	IF (cond) THEN RET, LOAD PL (data)	TOS	Pop	Load PL	NC	PC + 1	Hold	Hold	NC	5
01	OUTPUT	IF (cond) THEN OUTPUT	PC + 1	Hold	Hold	NC	PC + 1	Hold	Hold	NC	1
02	RET	IF (cond) THEN RET	TOS	Pop	Hold	NC	PC + 1	Hold	Hold	NC	5
03	GOTOSTK	IF (cond) THEN GOTO (STACK)	TOS	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
04	LDPL	IF (cond) THEN LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
05	PSHCNTR	IF (cond) THEN PUSH (CREG)	PC + 1	Push CREG	Hold	NC	PC + 1	Hold	Hold	NC	6
06	LDTM	IF (cond) THEN LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC + 1	Hold	Hold	NC	
07	POP	IF (cond) THEN POP	PC + 1	Pop	Hold	NC	PC + 1	Hold	Hold	NC	5
0B	DEC	IF (cond) THEN DEC	PC + 1	Hold	DEC	NC	PC + 1	Hold	Hold	NC	
14	PSHPL	IF (cond) THEN PUSH, LOAD PL (data)	PC + 1	Push PC + 1	Load PL	NC	PC + 1	Hold	Hold	NC	6
15	PSH	IF (cond) THEN PUSH	PC + 1	Push PC + 1	Hold	NC	PC + 1	Hold	Hold	NC	6
16	PSHTM	IF (cond) THEN PUSH, LOAD TM (data)	PC + 1	Push PC + 1	Load TM	NC	PC + 1	Hold	Hold	NC	6
17	POPCNTR	IF (cond) THEN POP TO (CREG)	PC + 1	Pop	Load TOS	NC	PC + 1	Hold	Hold	NC	5
18	FORK	IF (cond) THEN GOTO PL (data) ELSE GOTO (STACK)	PL	Hold	Hold	Reset	TOS	Hold	Hold	NC	3
19	GOTOPL	IF (cond) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
1A	WAITPL	IF (cond) THEN GOTO PL (data) ELSE WAIT	PL	Hold	Hold	Reset	PC	Hold	Hold	NC	3
1B	WAITTM	IF (cond) THEN GOTO TM (data), ELSE WAIT	TM	Hold	Hold	Reset	PC	Hold	Hold	NC	3
1C	CALPL	IF (cond) THEN CALL PL (data)	PL	Push PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	3,6
1E	CALTM	IF (cond) THEN CALL TM (data)	TM	Push PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	3,6
1F	GOTOTM	IF (cond) THEN GOTO TM (data)	TM	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3

Key:
- PC = Program Counter
- TOS = Top of Stack
- CREG = Counter Register
- PL = Pipeline (data) Field
- TM (data) = Test Inputs Masked by DATA Field
- TM (mask) = Test Inputs Masked by MASK Field
- DEC = Decrement
- NC = No Change

Notes:

1. If condition Passes, Output CREG contents on next clock cycle.
2. If Condition = EQ, reset EQ flag.
3. If Condition = EQ and Conditon Passes, reset EQ flag.
4. If Condition = EQ and CREG $\neq 0$, reset EQ flag.
5. When Stack is popped, the next value in the Stack is transferred to TOS.
6. When Stack is pushed, TOS is transferred to next available Stack location before value is written into TOS.
7. Set EQ Flag if CONST field = T*M.

INSTRUCTIONS DEPENDENT ON CREG

			CREG = 0				CREG ≠ 0				
Op-code	Mnemonic	Assembler Statement	PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	Notes
08	LPPL	WHILE (CREG < > 0) LOOP TO PL (data)	PC + 1	Hold	Hold	NC	PL	Hold	DEC	Reset	4
0A	LPTM	WHILE (CREG < > 0) LOOP TO TM (data)	PC + 1	Hold	Hold	NC	TM	Hold	DEC	Reset	4
0C	DECPL	WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC	Hold	DEC	NC	
0E	DECTM	WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC	Hold	DEC	NC	
0F	LPSTK	WHILE (CREG < > 0) LOOP TO (STACK)	PC + 1	Pop	Hold	NC	TOS	Hold	DEC	Reset	4

INSTRUCTIONS DEPENDENT ON TEST CONDITION AND CREG VALUE

					Condition Pass			Condition Fail				
Op-code	Mnemonic	Assembler Statement	CREG Content	PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	Notes
1D	DECGOPL	IF (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT	≠ 0	PL	Hold	Hold	Reset	PC	Hold	DEC	NC	3
			= 0	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	

UNCONDITIONAL INSTRUCTIONS

Opcode	Mnemonic	Assembler Statement	PC MUX	STACK	CREG	EQ FLAG	Notes
0D	CONT	CONTINUE	PC + 1	Hold	Hold	NC	2
10-13 (Binary 100XX)	CMP	CMP TM (mask) TO PL (constant)	PC + 1	Hold	Hold	Set	7

Key: PC = Program Counter
SREG = Stack Register
CREG = Counter Register
PL = Pipeline (data) Field
TM (data) = Test Inputs Masked by DATA Field
TM (mask) = Test Inputs Masked by MASK Field
DEC = Decrement
NC = No Change

Notes:

1. If condition Passes, Output CREG contents on next clock cycle.
2. If Condition = EQ, reset EQ flag.
3. If Condition = EQ and Conditon Passes, reset EQ flag.
4. If Condition = EQ and CREG ≠ 0, reset EQ flag.
5. When Stack is popped, the next value in the Stack is transferred to TOS.
6. When Stack is pushed, TOS is transferred to next available Stack location before value is written into TOS.
7. Set EQ Flag if CONST field = T*M.

Am29CPL154 SSR Diagnostics Option

As a programmable option, the Am29CPL154 FPC may be configured to contain Serial Shadow Register (SSR) diagnostics capability. SSR diagnostics is a simple, straightforward method of in-system testing to isolate problems down to the IC level.

The SSR diagnostics configuration activates a 36-bit-wide D-type register called a "shadow" register, on the pipeline register inputs. The shadow register can be serially loaded from the SDI pin, parallel loaded from the pipeline register, or held. The pipeline register can be loaded from the Program Memory in normal mode or from the shadow register during diagnostics. A redefinition of four device pins is required to control the different diagnostics functions. T[7] also functions as the Serial Data Input (SDI), P[0] becomes the Serial Data Output (SDO), P[7] becomes the diagnostic clock (DCLK), and P[6] becomes the diagnostic mode control (MODE). The various diagnostic and normal modes are shown in table 4.

Serially loading a test instruction into the shadow register and parallel loading the shadow register contents into the pipeline register forces execution of the test instruction. The test result can then be clocked into the pipeline register as in normal operation mode, parallel loaded into the shadow register, and serially shifted out for system diagnostics.

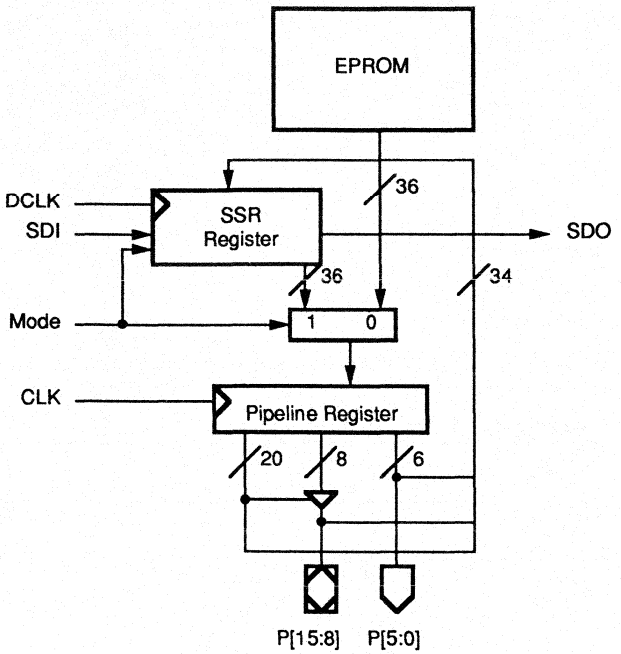
Table 4

Inputs				Outputs			Operation
SDI	MODE	DCLK	CLK	SDO	Shadow Register	Pipeline Register	
X	L	↑	H, L, ↓	S_0	$S_{i-1} \leftarrow S_i$ $S_{35} \leftarrow$ SDI	Hold	Serial Right – Shift Shadow Register
T [7] (Note 1)	L	H, L, ↓	↑	S_0	Hold	$P_i \leftarrow EPROM_i$	Normal Operation; Load Pipeline Register from EPROM
L	H	↑	H, L, ↓	L	$S_i \leftarrow P_i$	Hold	Load Shadow Register from Pipeline Register (Note 2)
X	H	H, L, ↓	↑	SDI	Hold	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	H, L, ↓	H	Hold	Hold	Hold Shadow Register

Notes:

1. During normal operation, this pin behaves as the T[7] test input.
2. S7, S6 are undefined. S[15:8] load from the source driving pins P[15:8]. If P[35] in the microword is a ONE, S[15:8] are loaded from the pipeline register. If P[35] in the microword is a ZERO, S[15:8] are loaded from an external source.

Key:
- H = HIGH
- L = LOW
- X = Don't Care
- ↑ = LOW-to-HIGH transition
- ↓ = HIGH-to-LOW transition



10136-027A

Figure 3. SSR Diagnostics Logic

Erasure

In order to fully erase all memory locations, it is necessary to expose the memory array to a standard ultraviolet light source having a wavelength of 2537 angstroms. The minimum recommended dose (UV intensity x exposure time) is 15 Wsec/cm^2. For a UV lamp with a 12 mW/cm^2 power rating, the exposure time would be about 30 minutes. The device should be located one inch from the source in a direct line.

It should be noted that erasure will begin with exposure to light having wavelengths less than 4000 angstroms.

To prevent exposure to sunlight or fluorescent lighting, an opaque label should be affixed over the window after programming.

OTP (One-Time Programmable) Am29CPL154 devices are available in plastic and are ideal for volume production. They can be inventoried unprogrammed and used with current software revisions; there is no window to be covered to prevent light from changing data.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.3 V to V_{CC} + 0.3 V
DC Output or I/O Pin Voltage	–0.3 V to V_{CC} + 0.3 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		115	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		125	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 4.5 V to 5.5 V	25	pF
		Others		T_A = –55°C to +125°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 2)

No.	Parameter Symbol	Parameter Description		H-30 Min.	H-30 Max.	H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			18		20	ns
2		CLK to A[8:0]			30		36	ns
3	t_S	T[7:0] to CLK, Registered		8		8		ns
4		T[7:0] to CLK, Asynchronous (Note 3)		33		40		ns
5		$\overline{RESET}$ to CLK, Registered		12		12		ns
6		$\overline{RESET}$ to CLK, Asynchronous (Note 3)		30		40		ns
7	t_H	CLK to T[7:0]		0		0		ns
8	(Note 4)	CLK to $\overline{RESET}$		0		0		ns
9	t_{PZX}	CLK to P[15:8] Enable			33		40	ns
10	t_{PXZ}	CLK to P[15:8] Disable			33		40	ns
11	t_{WL}	CLK Width	LOW	14		16		ns
12	t_{WH}		HIGH	14		16		ns
13	t_P	CLK Period (Note 3)		33		40		ns
14	f_{MAX}	Maximum Frequency ($1/t_P$)		30		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (T[7:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[7:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[7:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD

   T[7:0] to CLK setup time:
   T[7:0] (a) + (b) – (c) = T[7:0] to CLK setup time

   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time
4. These hold time parameters are tested on a sample basis.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-30 Min.	H-30 Max.	H-25 Min.	H-25 Max.	Unit
SSR Configuration								
15	t_{PD}	Mode to SDO			25		30	ns
16		SDI to SDO			25		30	ns
17	t_{CO}	DCLK to SDO			32		36	ns
18	t_S	Mode to CLK		25		30		ns
19		Mode to DCLK		25		30		ns
20		SDI to DCLK		25		30		ns
21		P[15:8] to DCLK		25		30		ns
22	t_H	CLK to Mode		6		6		ns
23	(Note 1)	DCLK to Mode		0		0		ns
24		DCLK to SDI		0		0		ns
25		DCLK to P[15:8]		0		0		ns
26	t_{WL}	DCLK Width	LOW	20		25		ns
27	t_{WH}		HIGH	20		25		ns
28	t_P	DCLK Period		40		50		ns

Note:

1. These hold time parameters are tested on a sample basis.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.3 V to V_{CC} + 0.3 V
DC Output or I/O Pin Voltage	–0.3 V to V_{CC} + 0.3 V
DC Input Current	–10 mA to +10 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices

Ambient Temperature (T_A) Operating in Free Air	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = 25°C, 125°C and –55°C.

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC} – 0.5 V, V_{CC} = Max. (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0.5 V, V_{CC} = Max. (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	CMOS	V_{IN} = GND or V_{CC}		130	mA
			TTL	V_{IN} = 0.5 V or 2.4 V		140	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = Max. T_A = 25°C No Load			100 pF Typical		

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. The dynamic current consumption is:
   I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Max.	Unit
C_{IN}	Input Capacitance	$\overline{RESET}$	V_{IN} = 2.0 V	V_{CC} = 4.5 V to 5.5 V	25	pF
		Others		T_A = –55°C to +125°C	15	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	15	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
1	t_{CO}	CLK to P[15:0]			25	ns
2		CLK to A[8:0]			40	ns
3	t_S	T[7:0] to CLK, Registered		10		ns
4		T[7:0] to CLK, Asynchronous (Note 3)		40		ns
5		$\overline{RESET}$ to CLK, Registered		16		ns
6		$\overline{RESET}$ to CLK, Asynchronous (Note 2)		40		ns
7	t_H	CLK to T[7:0]		0		ns
8	(Note 4)	CLK to $\overline{RESET}$		0		ns
9	t_{PZX}	CLK to P[15:8] Enable			40	ns
10	t_{PXZ}	CLK to P[15:8] Disable			35	ns
11	t_{WL}	CLK Width	LOW	20		ns
12	t_{WH}		HIGH	20		ns
13	t_P	CLK Period (Note 3)		40		ns
14	f_{MAX}	Maximum Frequency ($1/t_P$)		25		MHz

Note:

2. See Switching Test Circuit for test conditions.
3. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:
   a. Measure delay from input (T[7:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.
   b. Measure setup time from T[7:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.
   c. Measure delay from T[7:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

   To calculate the desired parameter measurement, the following formula is used:
   Measurement (a) + Measurement (b) – Measurement (c)

   CLK PERIOD:
   CLK (a) + (b) – (c) = CLK PERIOD

   T[7:0] to CLK setup time:
   T[7:0] (a) + (b) – (c) = T[7:0] to CLK setup time

   $\overline{RESET}$ to CLK setup time:
   $\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time
4. These hold time parameters are tested on a sample basis.

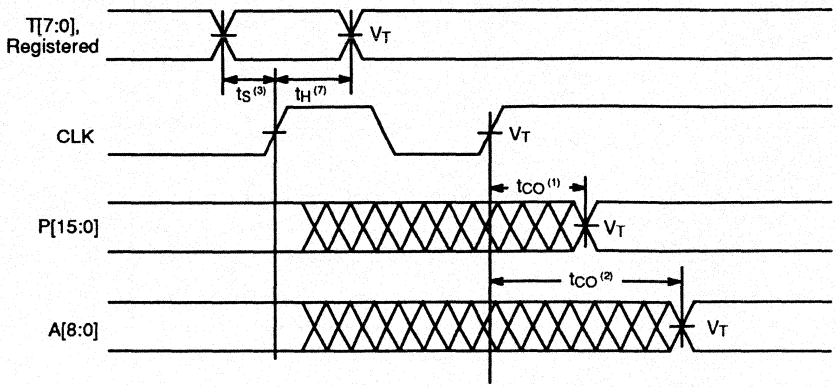
SWITCHING CHARACTERISTICS over MILITARY operating range (Continued)

No.	Parameter Symbol	Parameter Description		H-25 Min.	H-25 Max.	Unit
SSR Configuration						
15	t_{PD}	Mode to SDO			30	ns
16		SDI to SDO			30	ns
17	t_{CO}	DCLK to SDO			30	ns
18	t_S	Mode to CLK		30		ns
19		Mode to DCLK		30		ns
20		SDI to DCLK		30		ns
21		P[15:8] to DCLK		30		ns
22	t_H	CLK to Mode		6		ns
23	(Note 1)	DCLK to Mode		0		ns
24		DCLK to SDI		0		ns
25		DCLK to P[15:8]		0		ns
26	t_{WL}	DCLK Width	LOW	30		ns
27	t_{WH}		HIGH	30		ns
28	t_P	DCLK Period		60		ns

Note:

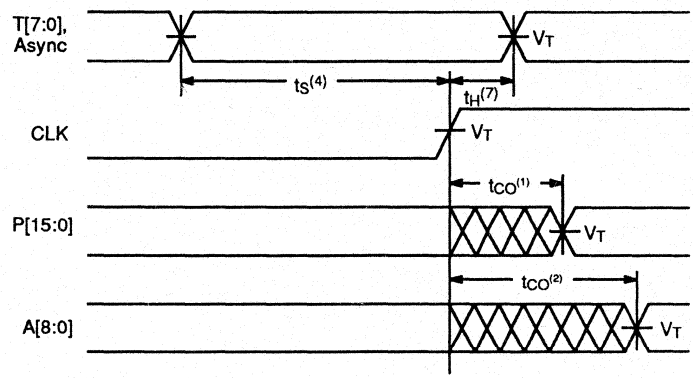
1. These hold time parameters are tested on a sample basis.

SWITCHING WAVEFORMS
Normal Configuration



10136-028A

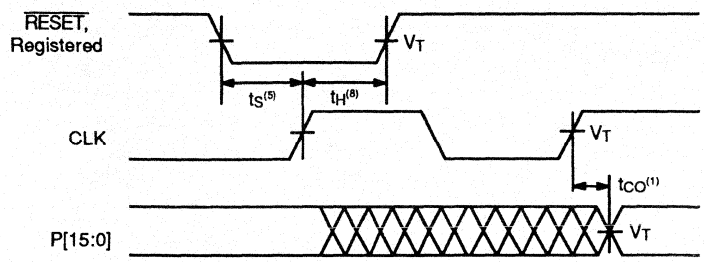
Registered Test Inputs



10136-029A

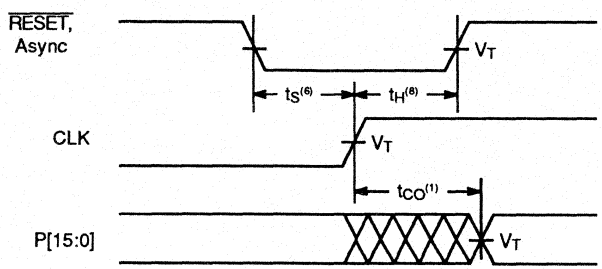
Asynchronous Test Inputs

SWITCHING WAVEFORMS (Continued)
Normal Configuration



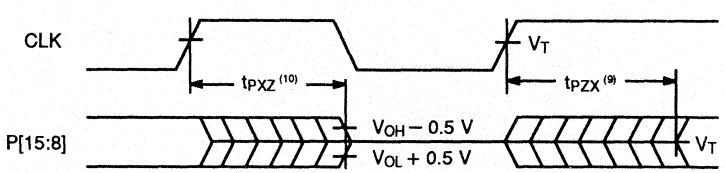
10136-030A

Registered $\overline{\text{RESET}}$



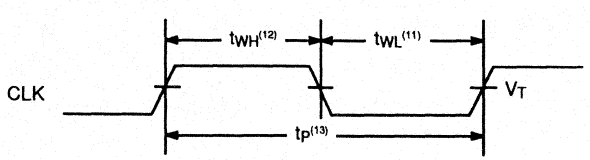
10136-031A

Asynchronous $\overline{\text{RESET}}$



10136-032A

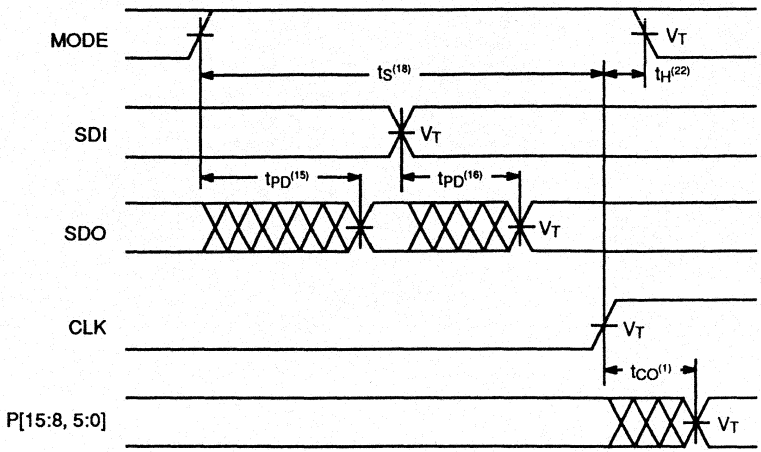
CLK to Output Disable/Enable



10136-033A

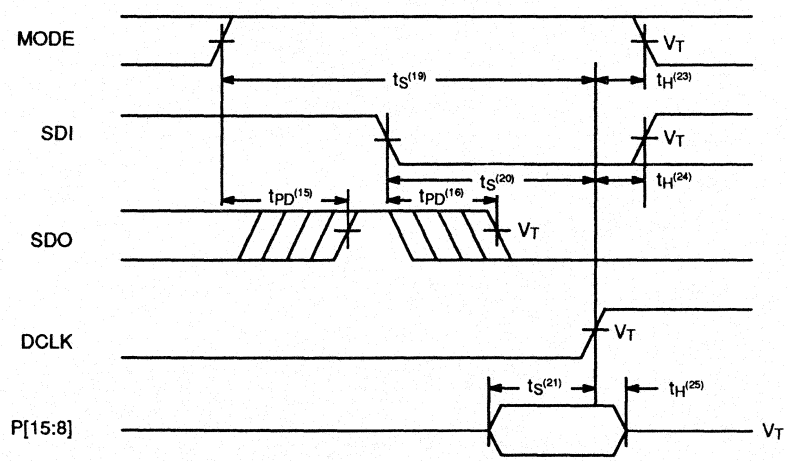
Clock Width/Period

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10136-034A

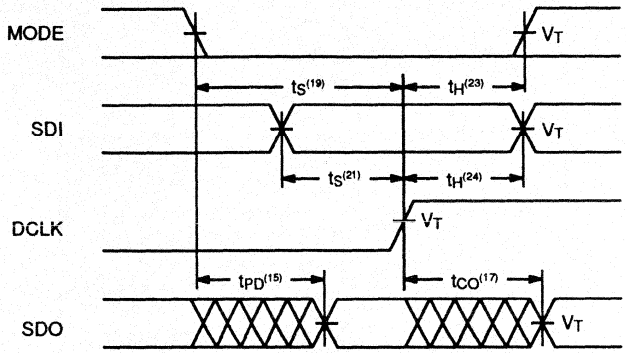
Load Pipeline Register from Shadow Register



10136-035A

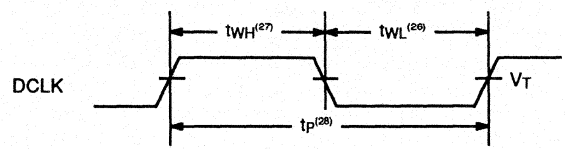
Load Shadow Register from Pipeline Register and/or Pins

SWITCHING WAVEFORMS (Continued)
SSR Configuration



10136-036A

Shift Shadow Register



10136-037A

DCLK Width/Period

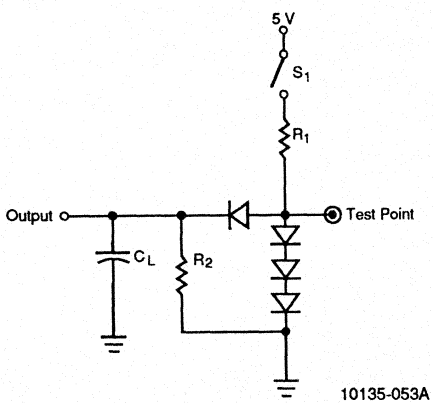
3

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

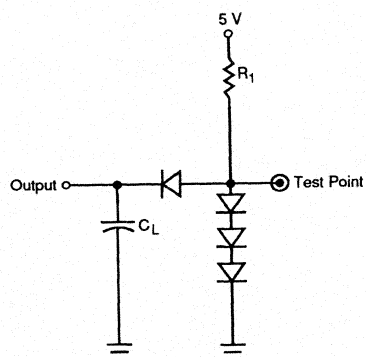
KS000010-PAL

SWITCHING TEST CIRCUIT



10135-053A

Three-State Outputs



10135-054A

Two-State Outputs

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	667 Ω	5 kΩ	667 Ω	5 kΩ	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Note:

Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω: t_r ≤ 2.5 ns.

TEST PHILOSOPHY AND METHODS

The following eight points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

7. Threshold Testing

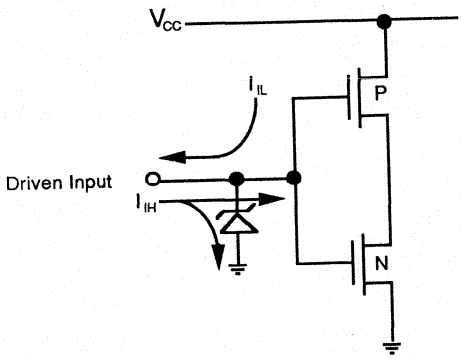
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.

8. AC Testing

   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



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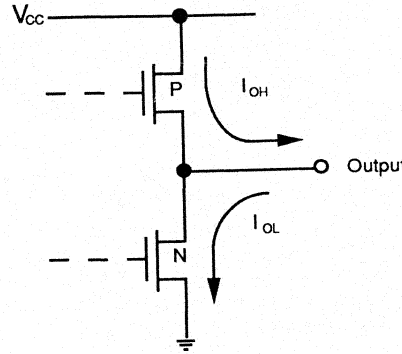

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Thermal Inpedance Values (θ_{JA}), Typical

28-Pin Plastic SKINNYDIP (PD3028)	50°C/W
28-Pin Windowed Ceramic SKINNYDIP (CDE028)	40°C/W
28-Pin Plastic Leaded Chip Carrier (PL 028)	55°C/W
28-Pin Windowed Ceramic Leadless Chip Carrier (CLV028)	55°C/W

Final

Am2971A

Enhanced Programmable Event Generator (PEG)™

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

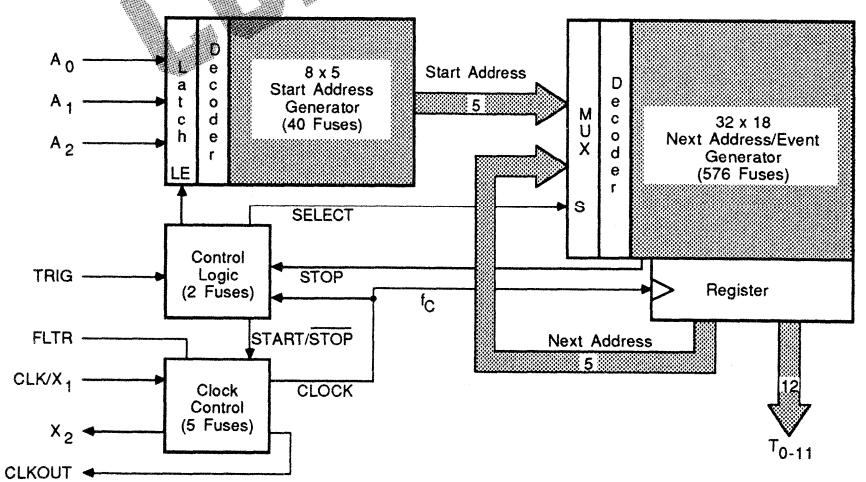
- Generates arbitrarily defined output sequences on 12 parallel outputs
- Timing resolution down to 10 ns
- Internal frequency-multiplying Phase-Locked Loop (PLL)
- Crystal-controlled on-chip oscillator
- Programmable trigger polarity and STOP function

GENERAL DESCRIPTION

The PEG is a versatile source of 12 simultaneous timing sequences. It can act as a digital substitute for multiple tapped delay lines or as a general-purpose user-programmable waveform generator.

Timing is derived from an external TTL source or an on-chip crystal oscillator, combined with an on-chip programmable frequency-multiplying PLL and clock divider. This achieves excellent timing resolution, down to 10 ns, from low-cost stable frequency sources of 10 MHz or less. The PEG uses platinum-silicide fuse technology and is programmed similar to any other AMD PROM.

BLOCK DIAGRAM



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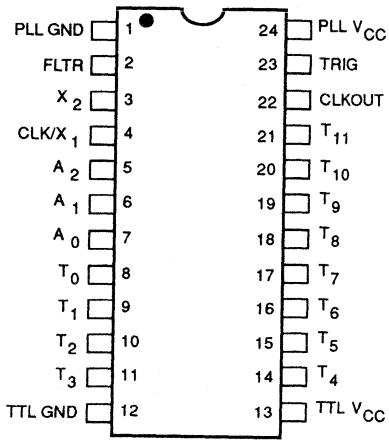
Publication # 05280 Rev. E Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAMS

DIP



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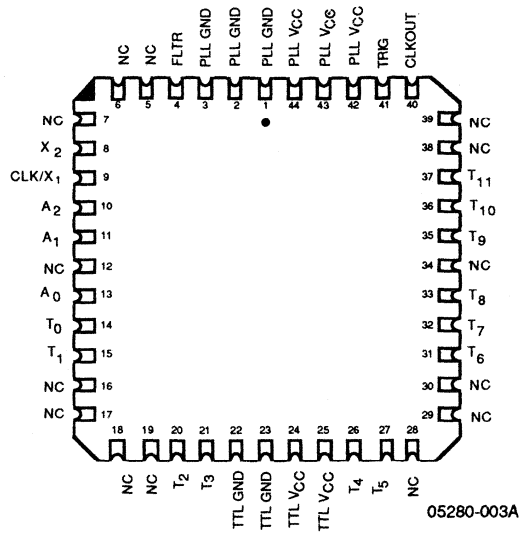
LCC*



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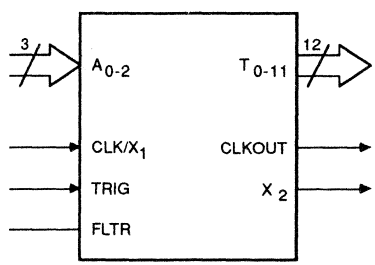
* Top View, JEDEC type-C package (NC = No Connection)

LOGIC SYMBOL



Approximate Gate Count: 100

Die Size: 0.173" x 0.257"

05280-004A

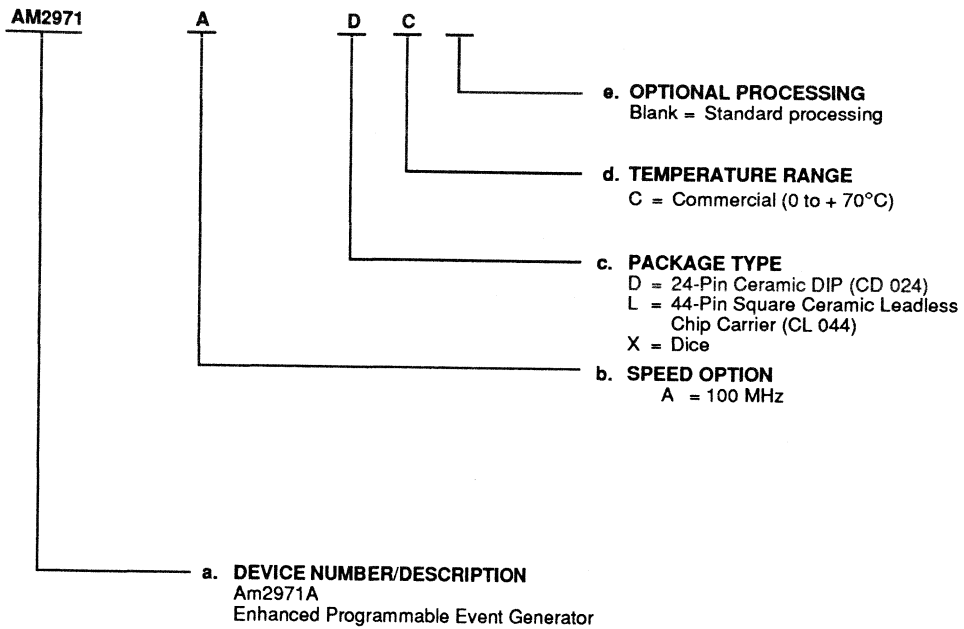
THERMAL CHARACTERISTICS

	24-pin Ceramic DIP	44-pin Ceramic LCC	Unit
θ_{JC} Max.	11	15	°C/W
θ_{JA} Max.	49	75	°C/W

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM2971A	DC, LC, XC

Valid Combinations

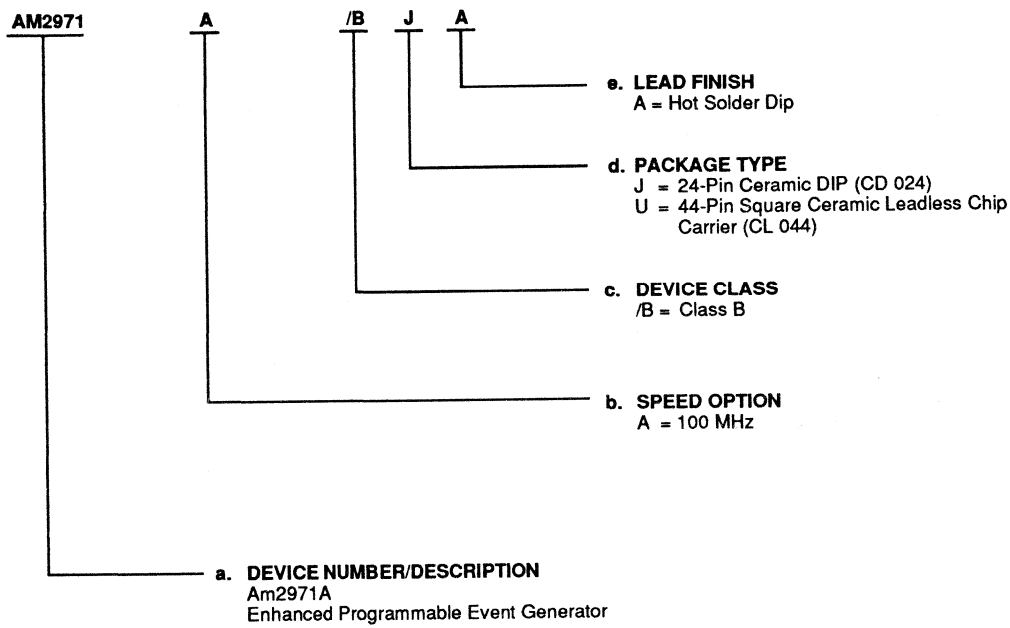
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2971A	/BJA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_0–A_2
Addresses (Inputs)

These three bits access the Start Address Generator which contains eight user-programmed start locations. Each cycle starts at the location pointed to by the Start Address Generator word selected by the A_0–A_2 inputs. In the Program Mode, these inputs are unused and may be allowed to float.

CLK/X_1 and X_2
Clock/Crystal (Input/Output)

A TTL-level clock may be applied to the CLK/X_1 input, with the X_2 output left floating, or an AT-cut parallel resonant crystal may be connected between these two pins.

CLKOUT
Output Clock (Output)

CLKOUT is a clock output pin which may be used for system reference. The output frequency for CLKOUT (f_O) is fuse-programmable to be either 0.5, 1, or 2 times the input frequency. This output is not valid in the Bypass Mode. In the Program Mode a high-voltage pulse is applied to CLKOUT to blow selected fuses.

FLTR
Filter

This pin is used to connect a 0.47-µF filter capacitor between the Phase-Locked Loop and ground when an external crystal is used or the PLL is selected. When clocking the PEG with an external TTL source greater than 10 MHz in the Bypass Mode, this pin should be tied LOW. See Figure 8 for proper device decoupling with the PLL Bypassed.

T_0–T_{11}
Timing Outputs (Outputs; Active HIGH)

These are the twelve timing outputs which follow a user-programmed timing pattern. They are registered for glitch-free operation. In the Program and Verify Modes, T_0–T_{10} function as address inputs to access each individual fuse. T_0–T_5 serve as Row Address inputs, and T_6–T_{10} serve as Column Address inputs (see Table 6). After power-up, these outputs are all LOW. T_{11} functions as data input in the Program Mode and as data output in the Verify Mode.

TRIG
Trigger (Input)

The timing cycle of the PEG can be started by either the rising or falling edge of the start (TRIG) pulse; the polarity is defined as a fuse option (fuse #621) in the TRIGGER POLARITY block. The trailing edge of the start (TRIG) pulse stops the timing sequence if the STOP TRIG fuse (fuse #622) is left unprogrammed (0).

POWER, GROUND
TTL/PLL Power Pair

There are two sets of V_{CC} and ground pins. One power pair is used by the PLL (Phase-Locked Loop) and the internal ECL circuitry. The other power pair is used by the remainder of the chip (TTL). Surface-mount packages have additional supply connections. All power and grounds must be connected regardless of mode of operation.

3

FUNCTIONAL DESCRIPTION

The leading edge of the trigger pulse (polarity is fuse-programmable) causes the continuously running internal clock to step through the on-chip PROM addresses, starting at one of eight fuse-programmed locations selected by the $A_{0\text{-}2}$ inputs.

Each addressed PROM location generates a fuse-programmed 12-bit pattern on the $T_{0\text{-}11}$ outputs, and internally generates the fuse-programmable next PROM address as well as a fuse-programmable STOP bit, if desired. Since there is no program counter, there is an almost infinite number of ways of programming the PEG for any desired output pattern. The user will most likely choose an ascending address sequence, but this is only one of many arbitrary choices.

The address sequence can loop but cannot execute conditional jumps.

The sequence of operations stops either as a result of the trailing edge of the trigger pulse (if so enabled by a fuse) or by the programmable STOP bit. A new sequence can only be started after the previous sequence has stopped.

The internal clock frequency, f_C (see Operational Description for an explanation of all internal and external signal frequencies), is derived from and is proportional to the frequency on the X_1 input, which is either an external TTL signal or the resonant frequency of a crystal connected between X_1 and X_2. Controlled by programmable fuses, the frequency on X_1 is either used directly or is first multiplied by a factor of 1.25, 2.5, 5, or 10 to generate the internal clock frequency. A clock output is available; its frequency (fuse-programmable) is either half, double, or equal to the frequency on X_1. This output is not valid in the Bypass Mode.

Operational Description

Frequency Definitions

To avoid confusion, the definitions of the various frequencies associated with the PEG are given below:

f_I = This is the user's Input Frequency into the CLK/X_1 pin.

f_O = This is the PEG's Output Frequency at the CLKOUT pin. A CLKOUT signal is valid only when the PLL is used.

f_C = This is the Internal Clock Frequency, which is gated into the event generator state machine.

When a timing sequence has been stopped, there is no f_C.

f_A = This is the Internal Altered Input Frequency, which is equivalent to f_C in value. This frequency is always generated, but it is not gated to the state machine (thus becoming f_C) unless a sequence is started.

f_{PLL} = This is the Phase-Locked Loop Frequency (f_I x 5 or f_I x 10).

TRIG-to-Output Delay

Operation of the PEG is initiated by a transition (of programmed polarity) on the TRIG input. This transition starts a series of internal events which lead to the clocking of the T_0–T_{11} output registers and to programmed changes on these outputs.

There are two possible conditions:

If the TRIG transition is synchronous with the frequency on X_1 (i.e., X_1 is a TTL clock signal and TRIG is synchronized with it), then the TRIG-to-output delay can be well-controlled, but the designer must analyze the timing and programming relationship carefully, as described below.

In the more normal case where TRIG is asynchronous to the frequency on X_1, the TRIG-to-output delay can be described very simply, but has an unavoidable uncertainty of one internal clock period.

Trigger Asynchronous

Start Delay

The delay from the active trigger edge to the first possible change of output pattern on T_0–T_{11} is the sum of:

1) Propagation delays in the trigger circuit plus output driver,
2) Up to one clock period of f_A due to the asynchronous relationship between TRIG and f_A, and
3) One clock period of f_A (used internally to prevent metastable operation).

Stop Delay

A timing sequence can be stopped either by the trailing edge of the start (TRIG) pulse (if so enabled by leaving fuse #622 unprogrammed) or by a programmed STOP bit in the Next Address/Event Generator fuse block.

The timing sequence stops when it detects either or both of these conditions. If stopped by a programmed STOP bit, the outputs remain at the level that is programmed in the same address location as the STOP bit. If stopped from the TRIG input, there is a delay equivalent to the starting delay.

Trigger Synchronous

Detailed Analysis of the Start and Stop Timing Sequences

The operation of the TRIG function can best be described by a synchronous state machine which uses f_A as the clock. All transitions occur on the rising clock edge. Figure 1 is the state diagram, Figure 2 the equivalent timing diagram. The state diagram uses the terms "active" and "inactive" edges of TRIG, since the actual polarity of TRIG is user-programmable.

State A is the idle state, after a reset or after operation has stopped for more than two periods of f_A. In state A, Select and f_C are HIGH (i.e., the Next Address/Event Generator PROM is addressed from the Start Address Generator PROM), but the output registers are not clocked; they retain their previous value.

When TRIG goes active, the next rising edge of f_A forces the state machine into state B and causes f_C to be equal to f_A. The output registers are still not clocked.

The next rising edge of f_A forces the state machine into state C, clocks the output from the Next Address/Event Generator PROM into the output register and forces Select LOW. Subsequent cycles use the registered "next address" output as an address to the Next Address/Event Generator PROM. State C lasts until a STOP condition is encountered.

When a STOP condition is encountered, the next rising edge of f_C forces the state machine into state D. If TRIG goes active while the state machine is in state D, the next rising edge of f_A will cause it to go to state B; otherwise it will go to state A.

The shortest possible sequence is A-B-C-D-A, staying one f_A period in states B, C, D.

The fastest possible retrigger goes C-D-B-C, staying one f_A period in states D and B, at frequencies below 50 MHz. At frequencies greater than 50 MHz, the PEG will stay two clock periods in state D.

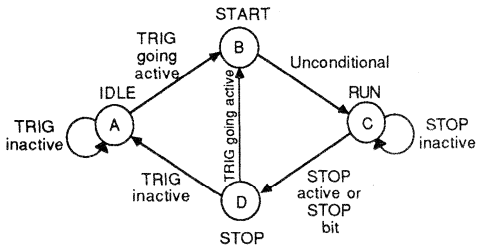


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Figure 1. State Machine Diagram

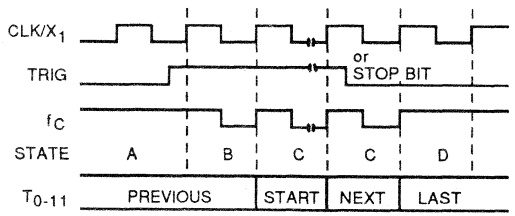

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Figure 2. State Machine Timing (Bypass Mode)

Start And Stop Timing Synchronous With f_I

The following paragraphs describe in detail the timing relationship and requirements between TRIG and the output changes on T_0–T_{11}, provided that TRIG is synchronous with f_I.

Bypass Mode ($f_C = f_I$)

TRIG must change from inactive to active for a specified setup time before the rising edge on X_1 and must stay active at least until 5 ns after the next subsequent rising edge on X_1. If the inactive-going edge of TRIG is programmed as a STOP condition, the shortest legitimate TRIG pulse will cause the state machine to cycle from state A to B to C to D, clocking the output register twice (first with the code accessed by the start address, then with the code accessed by the "next address" bits). If TRIG lasts additional X_1 clock periods, the state machine will spend this additional time in state C and the PEG will step through more codes.

PLL x5 or x10 Mode

When the f_{PLL} output is used as f_A, either 5 or 10 internal clock cycles occur for every f_I clock cycle. Since f_A is phase-synchronized to the rising edge of X_1, the timing analysis is very similar to the previous one, with f_A substituted for periods on X_1. The setup times associated with f_I also apply to f_A, since f_A is in phase with f_I. If the TRIG setup time with respect to X_1 exceeds one f_{PLL} period, then the state machine may trigger on the earlier internal clock. Because of the spread of guaranteed device parameters, an uncertainty is introduced. Thus, using the "STOP-from-TRIG" feature to generate a predetermined number of output sequences could result in an incorrect number of transitions (either more or less).

÷2 or ÷4 Mode

In this mode the rising transitions of f_A are no longer uniquely related to the rising transitions of f_I or f_{PLL}, since the ÷2 counter can be in either of two starting states and the ÷4 counter can be in any one of four possible starting states.

The START and STOP sequences, therefore, have an additional unpredictable delay of either a 0 or 1/2 period of f_A (if ÷2 is chosen), or either a 0, 1/4, 1/2, or 3/4 period of f_A (if ÷4 if chosen).

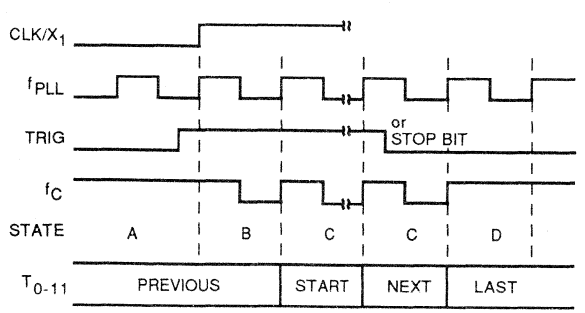

Figure 3. PLL Mode

05280-007A

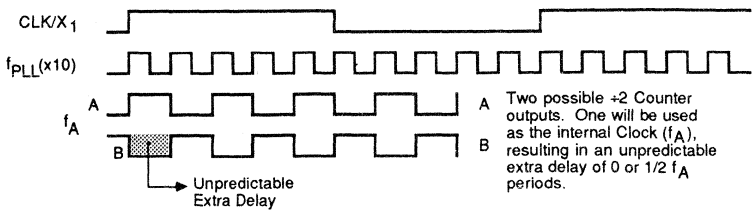

Figure 4. ÷2 Mode

05280-008A

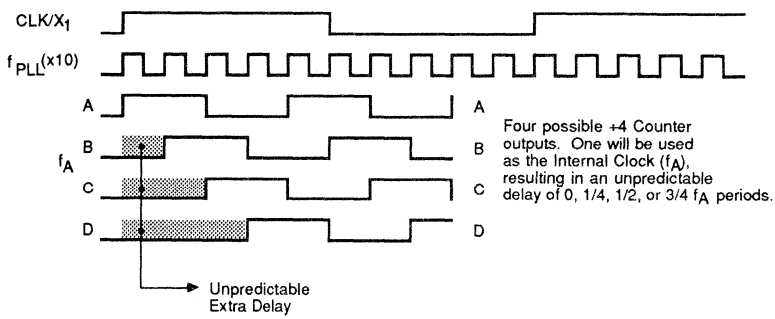

Figure 5. ÷4 Mode

05280-009A

Output Skew and Jitter

The twelve timing waveform outputs (T_0–T_{11}) are synchronized internally in an output register in order to minimize output skew.

The guaranteed maximum value for the remaining skew is specified by parameters 6–10 in the Switching Characteristics Table (depending upon the PEG version used and the number and type of transitions).

See Switching Characteristics for tighter skew specifications of certain outputs. More closely matched outputs should be used for more critical timing.

Any oscillator, and especially a Phase-Locked Loop, exhibits a certain amount of jitter — random phase modulation of the internal clock. Such jitter affects all outputs together (synchronously).

Jitter is typically less than ±1.0 ns for the ceramic DIP and Flatpack, and less than ±0.5 ns for the LCC package.

Output Event Resolution

Each of the twelve timing waveform outputs (T_0–T_{11}) can be programmed to change on any rising edge of the internal clock frequency (f_C), with the following restrictions:

The Am2971A has a maximum operating frequency of 100 MHz with a TTL source, all outputs in use. An output resolution of 10 ns for transitions of the same output or between transitions of different outputs is obtainable when a maximum of nine outputs (any nine) are switched simultaneously. If more than nine outputs are used, resolution within the same output is 20 ns, and 10 ns between outputs. If a crystal is used to clock the Am2971A, all outputs may be used, but only six outputs (any six) can be programmed to switch simultaneously. The output resolution with six outputs switching can be 10 ns within or between outputs. At internal frequencies less than 85 MHz, there are no programming restrictions (all outputs can switch simultaneously).

Table 1. Output Resolution
(Between Successive Transitions of the Same Output)

Number of outputs switching simultaneously		12, 11, 10	9, 8, 7	6, 5, 4, 3, 2, 1
TTL Clock Source	PLL	20 ns	10 ns	10 ns
	Bypass			
Crystal Clock Source		Not Allowed	Not Allowed	10 ns

Oscillator

The Am2971A contains an inverting linear amplifier which can be used as a crystal oscillator. Various types of crystals are available, and the manufacturers' literature should be consulted to determine the appropriate type.

Crystal frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32 pF), or to specify the load when ordering a special crystal.

The circuit of a typical 1st-harmonic oscillator is shown in Figure 6. The crystal load is comprised of the two 68-pF capacitors effectively in series. This 34 pF approximates the standard 32-pF crystal load. If a closer match is required, one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer.

A typical crystal specification for use in this circuit is:

Frequency Range: 2–20 MHz
Resonance: AT, Parallel Resonant Mode
Load: 32 pF
Stability: to match system requirements

In order to eliminate stray pick-up, it is good practice to ground the case of the crystal and to keep all connections as short as possible.

At fundamental frequencies below 6 MHz, the crystal might accidently operate in 3rd-harmonic mode. To prevent this, a resistor should be added in series with the X_2 pin as shown in the circuit diagram (Figure 6).

The resistor value should equal the impedance of C:

$$R = XC = \frac{1}{2\pi f * C} = \frac{2342\ \Omega}{f(MHz)}$$

Example: R = 390 Ω for 6 MHz

Design Considerations

1) Oscillator external connections must be less than 1" long—wirewrap is not recommended.
2) V_{CC} and GND connections to power plane should be less than 1/2" long.
3) Effective supply decoupling over a broad frequency range is mandatory (Reference Figures 7 and 8).

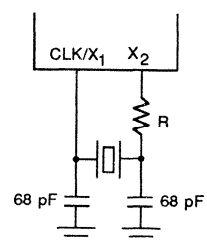

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Figure 6. Am2971A Crystal Oscillator Circuit

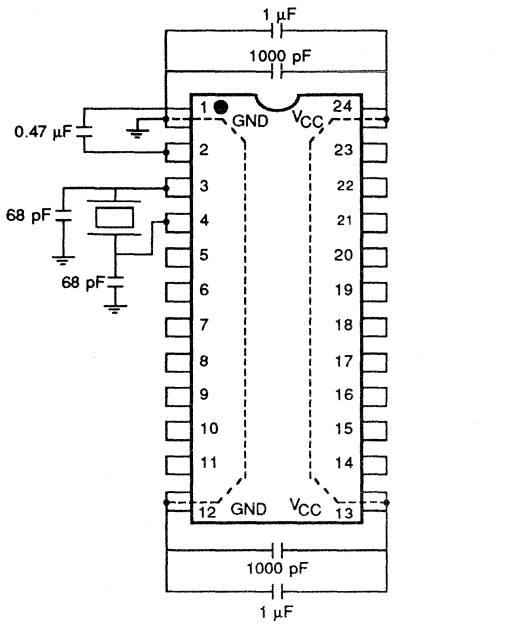


Figure 7. Am2971A Recommended Layout and Decoupling (Crystal Input)

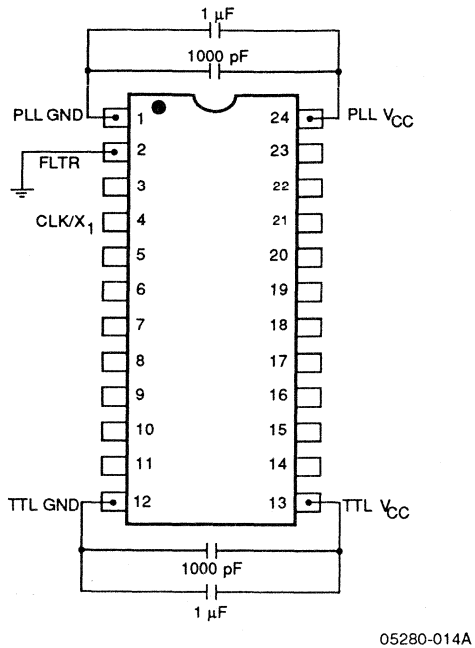


Figure 8. PEG Decoupling With PLL Bypassed

Bypass Mode Decoupling

When using the PEG with a direct TTL source above 10 MHz with the PLL bypassed, the decoupling shown in Figure 8 is mandatory.

The decoupling of the FLTR (filter) pin is necessary at frequencies higher than 10 MHz because the PLL will attempt to lock onto the incoming clock signal at CLK/X_1. This can cause anomalies in device operation and increase device jitter. Grounding the FLTR pin will isolate the PLL from the incoming clock and permit proper operation of the PEG.

PEG SUPPORT

AmPEGASUS

AMD's PEG Adaptor Socket and Universal Software (Am-PEGASUS) is a passive programmer adaptor socket made for use in conjunction with Data I/O Corporation's Model 29/29A/29B Universal Programmer equipped with a UniPak 2/2A/2B adaptor. This passive unit makes use of the generic 2K x 8 PROM socket by reassigning the PROM configuration into a PEG pin configuration and programming algorithm. The socket draws its power from the Model 29 and contains protective circuitry to provide additional safeguards for the UniPak. Additional information can be obtained from the AmPEGASUS User's Manual, PID# 09241A.

AmPEGPDS

AMD's PEG Programming Development Software (AmPEGPDS) is a software tool designed to aid the user in creating fuse map in the JEDEC standard for programming a PEG device. The main purpose of the software is to create and translate the input specification into a format that can be accepted by the programmer. The input specification is created by the designer using AmPEGPDS as an editor. AmPEGPDS is available on a standard 5-1/4" floppy disk, included in both of the PEG Application Kits described as follows.

PEG Application Kits

The **PEG Starter Kit** includes:

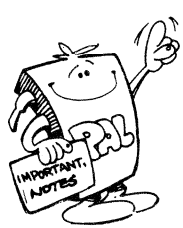
- Am2971A PEG Data Sheet
- AmPEGPDS
- AmPEGPDS Software User's Manual
- Two PEG Unprogrammed Samples
- Applications Articles
- Am2971A Product Description

The PEG Starter Kit is available free of charge from any AMD Sales Representative.

The **PEG Design Kit** includes the **PEG Starter Kit** plus:

- AmPEGASUS Programming Adaptor Socket (customer to specify DIP or LCC)
- AmPEGASUS Translation Software
- AmPEGASUS User's Manual

Consult your AMD Sales Representative for pricing information on the PEG Design Kit.


IMPORTANT
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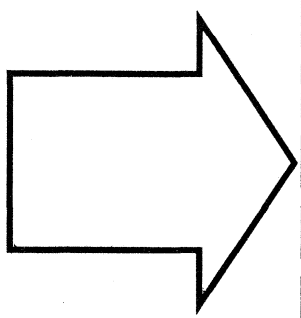


ECL/PGA Data Sheets

Final

PAL10H20EG8-6/PAL10020EG8-6

ECL Latched Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High-performance; t_{PD} = 6 ns
- Eight user-programmable output logic macrocells for latched or combinatorial operation
- A registered version of the device is available as PAL10H20EV8 or PAL10020EV8 (see AMD Publication No. 06176)
- Up to twenty inputs and eight outputs
- Individually user-programmable output polarity
- Varied product-term distribution for increased design flexibility
- Individual product term for output enable
- Asynchronous-RESET and PRESET capability
- Power-up RESET capability
- PRELOAD for improved testability
- Special designed-in test features for factory AC and DC testing
- Proven fuses ensure high programming yield, fast programming and unsurpassed reliability
- 10KH/100K ECL options
- 50-ohm drive with wired-OR capability
- 24-pin 300-mil SKINNYDIP® and 28-pin chip carrier packages
- Supported by PALASM® software

GENERAL DESCRIPTION

The PAL10H20EG8/PAL10020EG8 is an advanced bipolar ECL Programmable Array Logic (PAL®) device. It uses the familiar sum-of-products (AND-OR) single array logic structure, allowing users to program custom logic functions. Fabricated with AMD's new advanced bipolar oxide-isolation process technology, and utilizing the innovative architectural features of the PAL22V10, the PAL10H20EG8/PAL10020EG8 represents the most advanced ECL PAL device available on the market today.

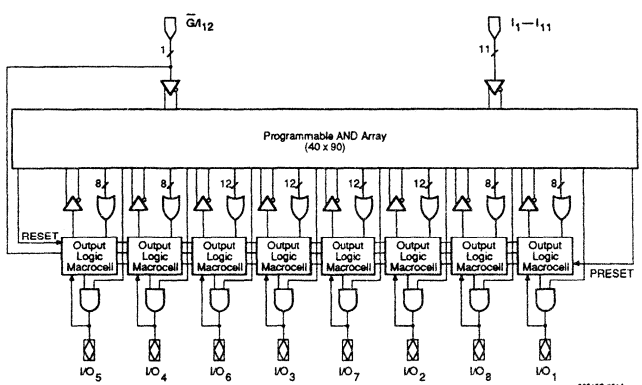
The PAL10H20EG8/PAL10020EG8 contains up to twenty inputs and eight outputs. It incorporates AMD's unique output logic macrocell (as in the PAL22V10), which allows the user to define and program the architecture of each output on an individual basis. Each output is user-programmable for either latched or combinatorial operation. Each output also has user-programmable output-polarity control, further simplifying the design. The flexibility of the programmable output logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PAL10H20EG8/PAL10020EG8 by providing a varied number of logical product terms per output. Four outputs have twelve logical product terms each, and the other four have eight logical product terms each. This varied allocation of logical product terms allows complex functions to be implemented in a single ECL PAL device. Each output also has a separate output-enable product term.

System operation has been enhanced by the addition of asynchronous-PRESET and RESET product terms for the PAL10H20EG8/PAL10020EG8. These product terms are common to all latched outputs.

The PAL10H20EG8/PAL10020EG8 incorporates power-up RESET on all latched outputs. It also has the ability to PRELOAD latches to any desired state during testing. PRELOAD permits full logical verification during testing.

BLOCK DIAGRAM



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PAL, PALASM, and SKINNYDIP are registered trademarks of Advanced Micro Devices, Inc.
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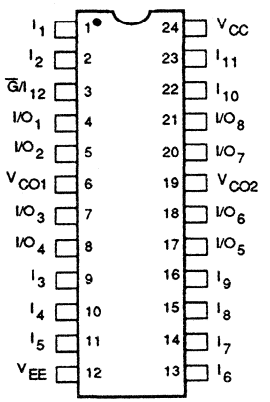
Publication # 08545 Rev. C Amendment/0
Issue Date: January 1990

CONNECTION DIAGRAMS
Top View

SKINNYDIP



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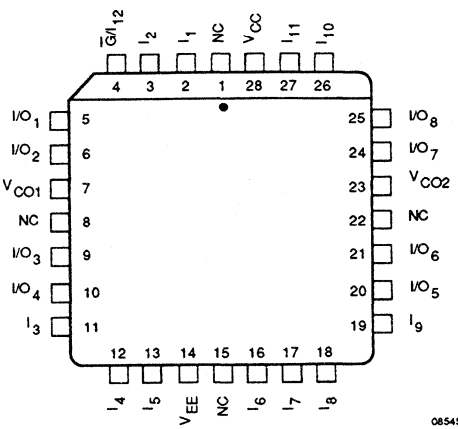
PLCC



08545C-002A

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Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

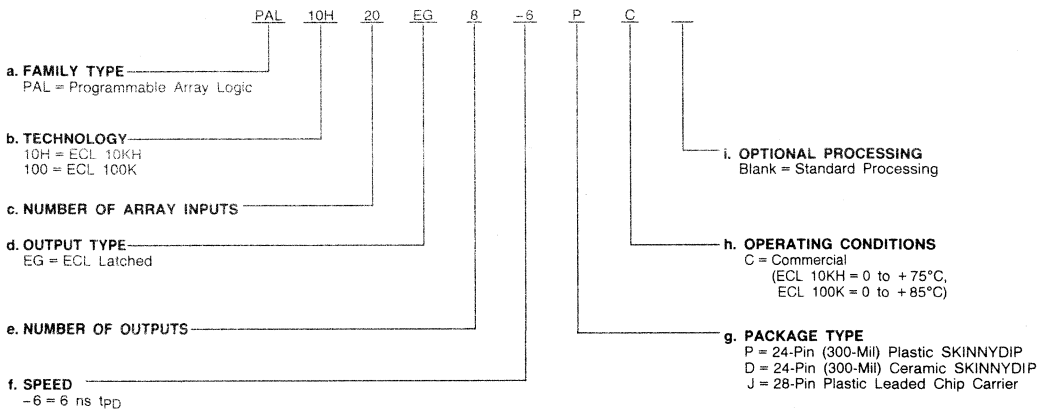
$I_1 - I_{11}$	Dedicated Input Pins (11)	V_{CC}	Circuit Ground
$I/O_1 - I/O_8$	Bidirectional Input/Output Pins (8)	V_{CO1}, V_{CO2}	Circuit Ground Pins for Outputs (2)
$\overline{G}/I_{12}$	Gate or Input Pin		
NC	No Connect	V_{EE}	Negative Supply Voltage

ORDERING INFORMATION

PAL Products

AMD PAL products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Speed
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations	
PAL10H20EG8-6	PC, DC, JC
PAL10020EG8-6	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: marked with AMD logo

4

FUNCTIONAL DESCRIPTION

The PAL10H20EG8/PAL10020EG8 is an advanced bipolar ECL PAL device. It contains a programmable fuse array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram in Figure 1 illustrates the basic architecture of the PAL10H20EG8/PAL10020EG8. There are up to twenty external inputs and eight outputs. The inputs are connected to a programmable-AND array. Initially, the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of the fuses, the AND gates may be "connected" to only the true inputs, the complement inputs, or to neither type of input. When both the true and complement fuses are left intact, a logical-FALSE results at the output of the AND gate. An AND gate with all the fuses programmed will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates.

There are an average of ten product terms per OR gate (output), distributed in a varied fashion. Four outputs have eight product terms each while the other four have twelve product terms each. This varied distribution of product terms allows more complex logic functions to be implemented.

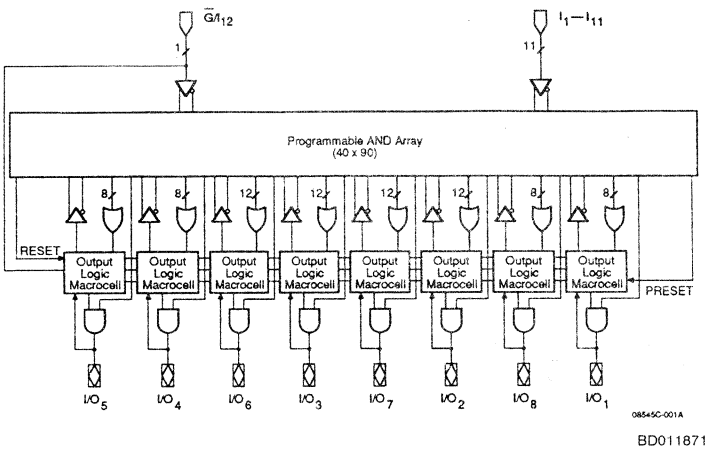
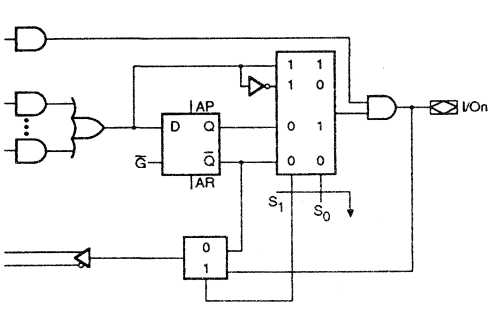


Figure 1. Block Diagram

Output Logic Macrocells

A useful feature of the PAL10H20EG8/PAL10020EG8 is its versatile programmable output logic macrocell. It allows the user to program the outputs on an individual basis in a very flexible manner.

The PAL10H20EG8/PAL10020EG8 output logic macrocell incorporates a latch that is transparent when $\overline{G}$ is LOW. As shown in the output logic macrocell diagram, each macrocell contains two programmable fuses (S_0 and S_1) for programming the output functions. S_1 controls whether the output will be latched or combinatorial. S_0 controls the output polarity (active-HIGH or active-LOW). Depending on the states of these two fuses, an individual output operates in one of four modes: Latched/Active-LOW, Latched/Active-HIGH, Combinatorial/Active-LOW, and Combinatorial/Active-HIGH. Each output is also provided with a separate output enable product term.



Enable term	$\overline{G}$	D	Active-HIGH Output
L	X	X	L (disable)
H	L	L	L (transparent)
H	L	H	H (transparent)
H	H	X	Q (latch)

Figure 2. PAL10H20EG8/PAL10020EG8 Output Logic Macrocell

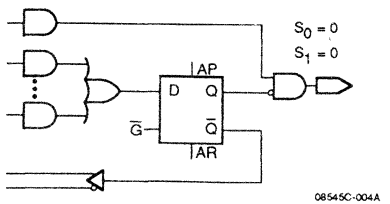


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Figure 3-1. Latched/Active-LOW

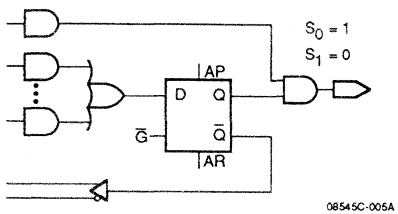

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Figure 3-2. Latched/Active-HIGH

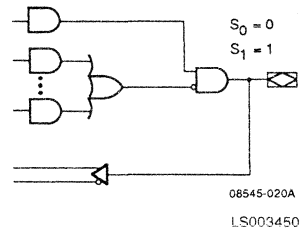

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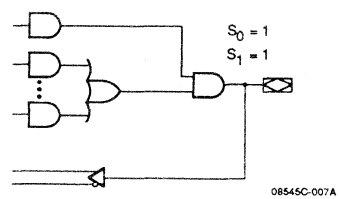
Figure 3-3. Combinatorial/Active-LOW



LD001530

Figure 3-4. Combinatorial/Active-HIGH

S_1	S_0	Output Configuration
0	0	Latched/Active-LOW
0	1	Latched/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed Fuse
1 = Programmed Fuse

4

Feedback

Another feature of the PAL10H20EG8/PAL10020EG8 output macrocell structure is the flexibility of its feedback selection. The feedback can be from either the I/O line or the latched output. The feedback multiplexer is also controlled by the S_1 fuse. The feedback path changes with the output-mode selection. If the output is selected to be latched, the feedback is latched. If the output is combinatorial, the feedback is from the I/O line. This feature enables the designer to optimally use the device to meet precise application requirements. Additionally, it allows the device to perform control tasks, such as arbitration functions, easily.

Output Enable

Each of the eight output logic macrocells of the PAL10H20EG8/PAL10020EG8 contains a dedicated product term for the output-enable function. When this product term is asserted LOW, the output is forced into a LOW state, where it remains until the output-enable product term goes HIGH.

PRESET and RESET

To improve in-system functionality, the PAL10H20EG8/PAL10020EG8 has additional PRESET and RESET product terms. Common asynchronous RESET and PRESET are provided for all the latches of the PAL10H20EG8/PAL10020EG8. When the asynchronous PRESET product term is asserted HIGH the output latches are loaded with a HIGH and when the RESET product term is asserted HIGH the output latches are loaded with a LOW. For the RESET/PRESET to work the latches should be in latched and not transparent mode. These functions are particularly useful for system power-on and reset. The latches automatically reset at power-up.

PRELOAD

To simplify testing, the PAL10H20EG8/PAL10020EG8 is designed with PRELOAD circuitry that provides an easy method for testing logic functionality. PRELOAD allows any arbitrary values to be loaded into the PAL device's output latches.

A typical functional-test sequence would be to verify all possible outputs for the device being tested. To verify these transitions requires the ability to set the latches to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the latch enable is driven transparent to allow logic to determine the "new state" of the outputs. These outputs can then be checked to validate the design.

Without PRELOAD capability, it is difficult and in some cases impossible to load an arbitrary value into the latches. This can lead to logic verification sequences which are either incomplete or excessively long. With PRELOAD capability, logic verification sequences can be greatly shortened, reducing the

test time and the development costs, and guaranteeing proper in-system operation.

Security Fuse

A security fuse is provided on each PAL10H20EG8/PAL10020EG8 to protect proprietary logic designs. It is programmed at the same time the array is programmed. The security fuse disables the pattern verification circuitry, and is verified by verifying the whole fuse array as if every fuse were programmed. The security fuse also disables preload.

Fabrication

The PAL10H20EG8/PAL10020EG8 is manufactured using Advanced Micro Devices' new oxide-isolation process. This advanced process offers increased density and reduced internal capacitance resulting in the fastest possible programmable logic devices.

The PAL10H20EG8/PAL10020EG8 is fabricated with AMD's fast-programming and highly-reliable fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Testing

The PAL10H20EG8/PAL10020EG8 contains many internal test features, including circuitry and extra fuses which allow AMD to test each part before shipping. This ensures extremely high post-programming functional yields. The test fuses are programmed to assure the ability of each part to perform correct programming. There are extra test words which are preprogrammed during manufacturing and tested to ensure correct logic operation and parametric integrity.

Using the PAL10H20EG8/PAL10020EG8 Device as a State Machine

Latches can be used in the implementation of state machines, but care must be taken in their use. They cannot be treated as if they were registers, which are more common in the TTL PAL devices. Since a latch is a level-sensitive storage device, it is more difficult to control the sequencing of states. In theory, when the gate pin is lowered, the latch can assume a new state. After waiting for the state to stabilize and for the feedback signal to propagate, the new state can be latched. Latching the state delays any further state changes until the next time the gate signal $\overline{G}$ goes LOW.

Latches Are Not Registers

The danger in treating a latch just like a register is that a feedback race condition will be explicitly built into the circuit. Enough setup time must be allowed for latching new data, yet if too much delay is allowed, the transparent latch may actually change state twice before being latched. For example, a divide-by-two counter (Figure 4a) may oscillate until the gate pin is raised if too much setup time is provided. The final state will depend on how fast the output was oscillating (Figure 4b), and will be unpredictable.

Use a Dual-Phase Clock

The usual method of dealing with this problem is to use a dual-phase clock, with two sets of latches. Implementation in the PAL10H20EG8/PAL10020EG8 would require a second device for the opposite phase. The logic must be partitioned such that all latches that are enabled on one phase of the clock feed only latches that are enabled on the opposite phase. This allows operation in a master-slave mode. The implementation can be made by providing one latch merely as a holding element, which can pass the data unchanged to another latch; this is essentially a master-slave register. In such a situation, two latches are needed for each state bit. The divide-by-two counter using a master and a slave is shown in Figure 4c.

If the entire state machine can be partitioned into two groups of state bits such that group 1 states only feed group 2 states and vice versa, then it becomes possible to place logic between the master latch and the slave latch. At that point the terms "master" and "slave" lose significance; each latch may implement a state bit by itself.

Greater System Speed And Efficiency

This kind of arrangement can sometimes be used to obtain a greater overall system speed than would be possible using

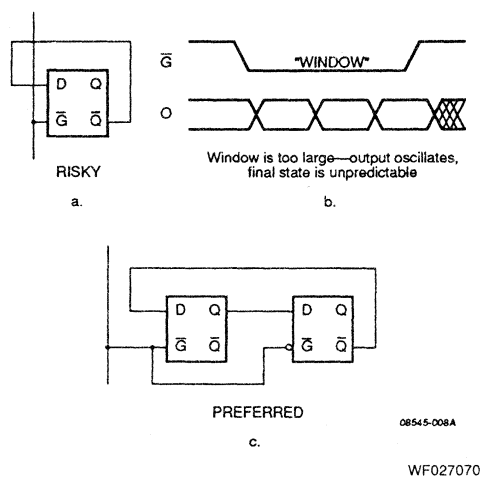
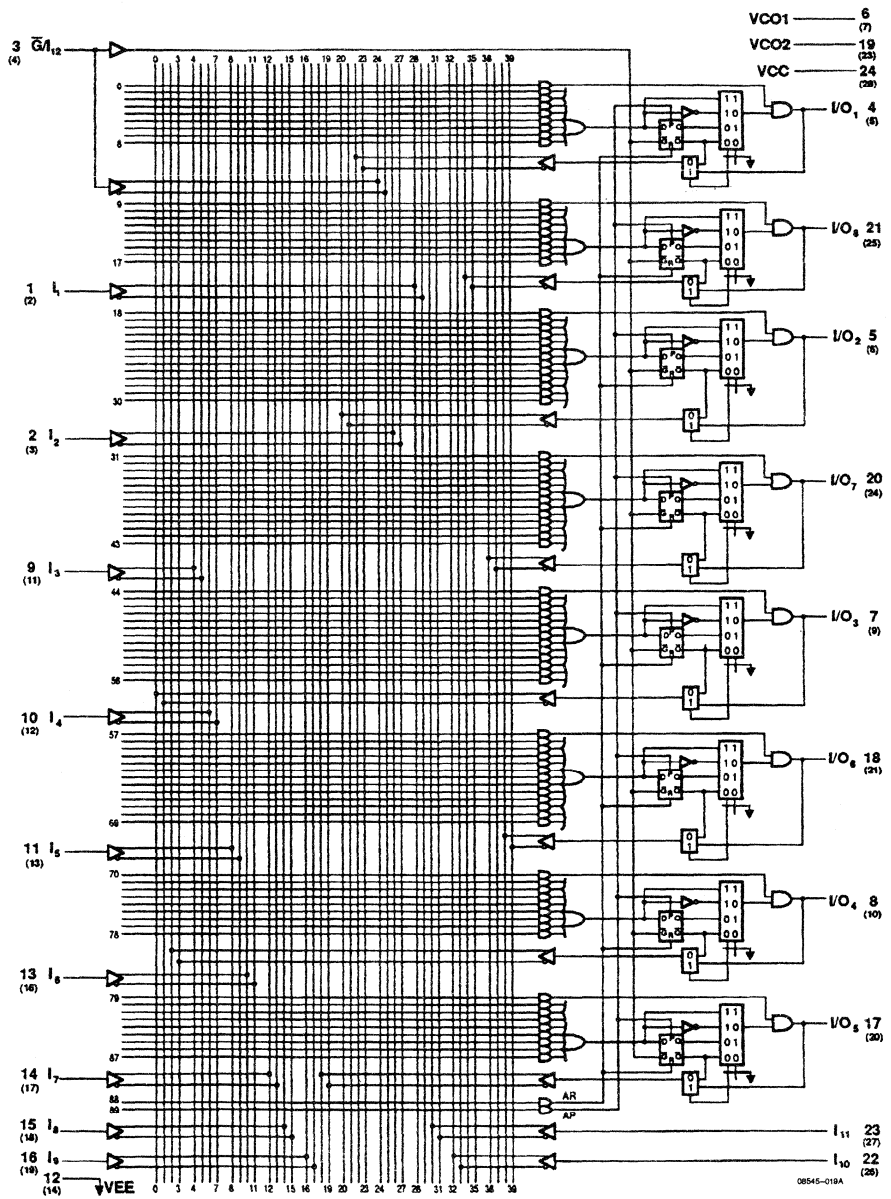


Figure 4. Using a Dual-Phase Clock

registers instead of latches. Since a register is essentially made up of two latches, it can also provide for a more efficient design with latches.



LD001761

DIP (PLCC) pinouts.

Figure 5. Logic Diagram for PAL10H20EG8/PAL10020EG8

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage (V_{EE})
with Respect to Ground ..... −8 V to 0 V
DC Input Voltage
with Respect to Ground ..... V_{EE} to 0 V
Output Current
-Continuous ..... 35 mA
-Surge ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices — 10KH Devices
Ambient Temperature (T_A) Operating
Air Flow 500 lfpm ..... 0°C to +75°C
Supply Voltage (V_{EE}) ..... −5.46 V to −4.94 V

Commercial (C) Devices — 100K Devices
Ambient Temperature (T_A) Operating
Air Flow 500 lfpm ..... 0°C to +85°C
Supply Voltage (V_{EE}) ..... −4.8 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1, 2)

PAL10H20EG8 (10KH) Devices

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$T_A = 0°C$	−1020	−840	mV
				$T_A = +25°C$	−980	−810	
				$T_A = +75°C$	−920	−735	
V_{OL}	Output LOW Voltage			$T_A = 0°C$	−1950	−1630	mV
				$T_A = +25°C$	−1950	−1630	
				$T_A = +75°C$	−1950	−1600	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$T_A = 0°C$	−1170	−840	mV
				$T_A = +25°C$	−1130	−810	
				$T_A = +75°C$	−1070	−735	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$T_A = 0°C$	−1950	−1480	mV
				$T_A = +25°C$	−1950	−1480	
				$T_A = +75°C$	−1950	−1450	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$T_A = 0°C$		300	μA
				$T_A = +25°C$		300	
				$T_A = +75°C$		300	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$T_A = 0°C$	0.5		μA
				$T_A = +25°C$	0.5		
				$T_A = +75°C$	0.3		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = 0°C$	−260		mA
				$T_A = +25°C$	−260		
				$T_A = +75°C$	−260		

Notes: 1. Designed to meet specifications shown after thermal equilibrium has been established. Guaranteed with transverse air flow exceeding 500 linear feet per minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

DC CHARACTERISTICS over COMMERCIAL operating ranges (Cont'd.) (Notes 1, 2)

PAL10020EG8 (100K) Devices

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	V_{EE} = −4.2 V	−1025	−880	mV
				V_{EE} = −4.5 V	−1025	−880	
				V_{EE} = −4.8 V	−1035	−880	
V_{OL}	Output LOW Voltage			V_{EE} = −4.2 V	−1810	−1605	mV
				V_{EE} = −4.5 V	−1810	−1620	
				V_{EE} = −4.8 V	−1810	−1620	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		V_{EE} = −4.2 V	−1150	−880	mV
				V_{EE} = −4.5 V	−1165	−880	
				V_{EE} = −4.8 V	−1165	−880	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		V_{EE} = −4.2 V	−1810	−1475	mV
				V_{EE} = −4.5 V	−1810	−1475	
				V_{EE} = −4.8 V	−1810	−1490	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		V_{EE} = −4.2 V		300	μA
				V_{EE} = −4.5 V		300	
				V_{EE} = −4.8 V		300	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		V_{EE} = −4.2 V	0.5		μA
				V_{EE} = −4.5 V	0.5		
				V_{EE} = −4.8 V	0.5		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		V_{EE} = −4.2 V	−285		mA
				V_{EE} = −4.5 V	−285		
				V_{EE} = −4.8 V	−285		

Notes: 1. Designed to meet specifications shown after thermal equilibrium has been established. Guaranteed with transverse air flow exceeding 500 linear feet per minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

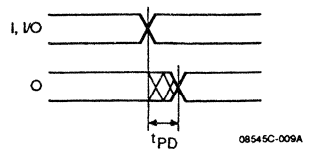
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1, 2)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PD}	Input or Feedback to Output		6	ns
t_S	Input or Feedback Setup Time	4		ns
t_H	Hold Time	0		ns
t_G	Gate to Output or Feedback		4	ns
t_{AR}/t_{AP}	Asynchronous RESET/PRESET to Latched Output		8	ns
t_{ARW}/t_{APW}	Asynchronous RESET/PRESET Width	6		ns
t_{ARR}/t_{APR}	Asynchronous RESET/PRESET Recovery Time	6		ns
t_{WL}	Gate Width LOW	3		ns
t_{EA}	Input to Output Enable		7	ns
t_{ER}	Input to Output Disable		7	ns
t_{RO}	Output Rise Time (20% – 80%)	0.7	2.2	ns
t_{FO}	Output Fall Time (80% – 20%)	0.7	2.2	ns

1. Designed to meet specifications shown after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Test conditions: see Setup for Testing Switching Characteristics.

Definitions of Switching Parameters

t_{PD}: Signal propagation delay from an input or an I/O pin through the array to a combinatorial ouput or a latched output while $\overline{G}$ is LOW.



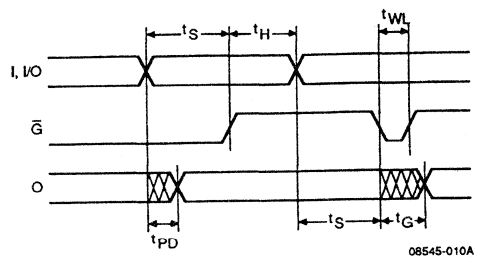
WF027080

t_S: Time that input data must be valid before $\overline{G}$ goes HIGH in order to latch data.

t_H: Time that input data must be valid after $\overline{G}$ goes HIGH in order to latch data.

t_G: Delay between lowering $\overline{G}$ and data appearing at the output.

Note: In order for a signal to appear at the output at a time t_G after lowering $\overline{G}$, the signal must be set up a time t_S before $\overline{G}$ is lowered. If this amount of time is not allowed, then the output will change at a time t_{PD} after the inputs were changed. The t_S needed is illustrated in the waveforms.



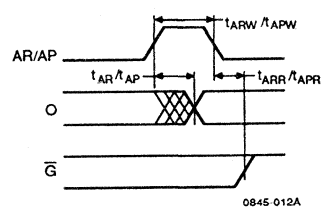
WF027090

t_{WL}: The minimum gate LOW pulse width needed to latch new data.

t_{AR}/t_{AP}: Delay from an input or I/O pin activating asynchronous reset or preset to data appearing at a latched output.

t_{ARW}/t_{APW}: The minimum input or I/O pin pulse width needed to activate asynchronous reset or preset.

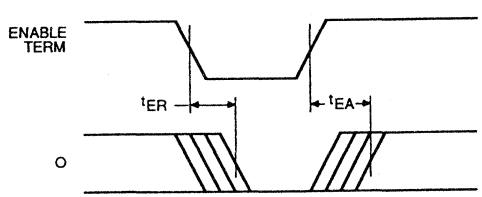
t_{ARR}/t_{APR}: Time that input or I/O pin must inactivate asynchronous reset or preset before $\overline{G}$ goes LOW in order to pass data.



WF027100

t_{EA}: Delay between input or I/O pin activating enable term and data appearing at outputs.

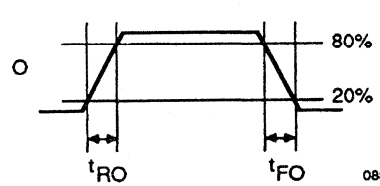
t_{ER}: Delay between input or I/O pin deactivating enable term and outputs going LOW.



WF027110

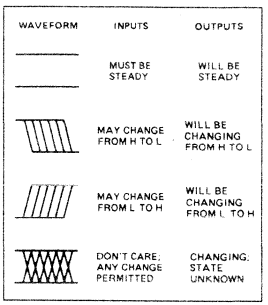
t_{RO}: Time taken for an output signal voltage to swing from 20% to 80% of the full logic swing.

t_{FO}: Time taken for an output signal voltage to swing from 80% to 20% of the full logic swing.



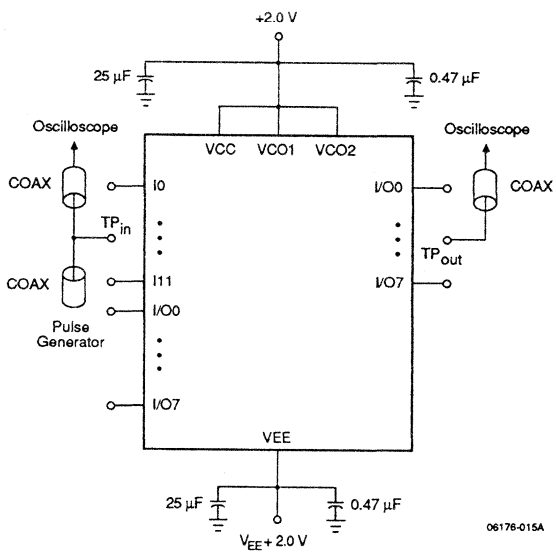
WF025960

KEY TO SWITCHING WAVEFORMS



KS000012

Setup for Testing Switching Characteristics



LS003460

Each oscilloscope channel input should have a 50 Ω termination to ground. Oscilloscope bandwidth should be a least 1 GHz.

The pulse generator should be capable of providing 1.5 ns rise and fall times (20% to 80%).

All input and output cables should be equal lengths of matched 50 Ω coaxial cable. Wire lengths between input (or I/O) pins and TP_{in} or between output pins and TP_{out} should be less than 1/4 in. long. Stubs should be avoided if possible; unavoidable stubs should be less than 2 in. long.

Used inputs that are not switching should be forced to V_{IL} or V_{IH}.

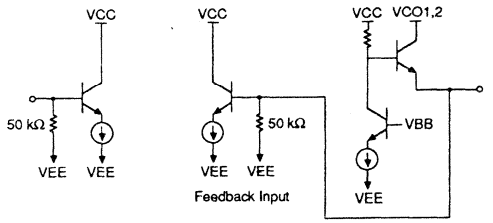
Outputs that are switching but not sensed should be terminated through 50 Ω to ground.

Unused inputs and outputs may be left open.

Note that all voltages are shifted by +2.0 V with respect to normal ECL operating conditions in order to take advantage of the input terminations of the oscilloscope.

Timing thresholds in this configuration are taken to be +0.7 V.

Input and Output Equivalent Schematics

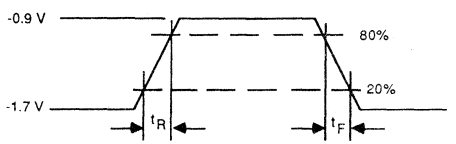


06176C-019A

TC004760

SWITCHING TEST WAVEFORM

INPUT PULSE



06176C-014A

WF023080

$t_R = t_F = 2.2$ ns Max. for 10KH

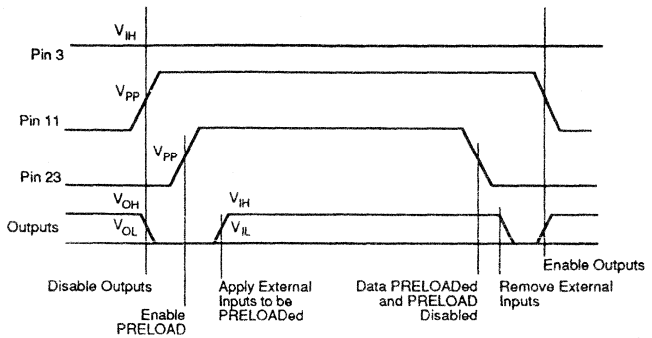
$t_R = t_F = 1.0$ ns Max. for 100K

PRELOAD OF LATCHED OUTPUTS

The PAL10H20EG8/PAL10020EG8 latched outputs are provided with circuitry to allow loading each latch to either a HIGH or LOW state. This simplifies testing since any state can be loaded into the latches to control outputs. The pin levels necessary to perform the PRELOAD function are detailed below.

PRELOAD is accessed by applying V_{PP} on pin 23. The data to be preloaded is set on the output pins. Bringing pin 23 back to a logic-LOW level latches the data into the output latches. During PRELOAD the outputs are disabled by a supervoltage on pin 11.

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Level During PRELOAD and Verify	−1.1	−0.9	−0.7	V
V_{IL}	Input LOW Level During PRELOAD and Verify	−1.85	−1.65	−1.45	V
V_{PP}	Voltage Applied to Pins 11 and 23 (DIP)	1.8	2.0	2.2	V

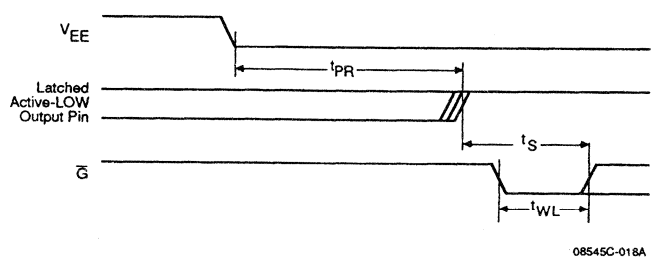


PRELOAD Timing Waveform

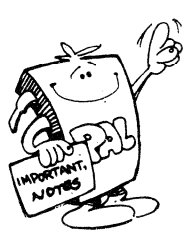
POWER-UP RESET

The latches in the PAL10H20EG8/PAL10020EG8 have been designed with the capability to RESET during system power-up. Following power-up, all latches will be LOW. The output state will depend upon the state of the output buffer and the polarity fuse. This feature provides extra flexibility to the designer. A timing diagram and a parameter table are shown below. Due to the asynchronous operation of the power-up RESET and the wide range of ways V_{EE} can fall to steady state, two conditions are required to insure a valid power-up RESET. These conditions are:

1. The V_{EE} fall must be monotonic.
2. Following RESET, the gate pin must not be driven LOW until all applicable input and feedback setup times are met.



Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t_{PR}	Power-Up RESET Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_{WL}	Gate Width LOW				


IMPORTANT
NOTES

Final

PAL10H20EV8-6/PAL10020EV8-6

ECL Registered Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High-performance; t_{PD} = 6 ns, f_{MAX} = 125 MHz
- Eight user-programmable output logic macrocells for registered or combinatorial operation
- A latched version of the device is available as PAL10H20EG8 or PAL10020EG8 (see AMD Publication No. 08545)
- Up to twenty inputs and eight outputs
- Individually user-programmable output polarity
- Varied product-term distribution for increased design flexibility
- Individual product term for output enable
- Asynchronous-RESET and PRESET capability
- Power-up RESET capability
- PRELOAD for improved testability
- Special designed-in test features for factory AC and DC testing
- Proven fuses ensure high programming yield, fast programming and unsurpassed reliability
- 10KH/100K ECL options
- 50-ohm drive with wired-OR capability
- 24-pin 300-mil SKINNYDIP® and 28-pin plastic chip carrier package
- Supported by PALASM® software

GENERAL DESCRIPTION

The PAL10H20EV8/PAL10020EV8 is an advanced bipolar ECL Programmable Array Logic (PAL®) device. It uses the familiar sum-of-products (AND-OR) single array logic structure, allowing users to program custom logic functions. Fabricated with AMD's new advanced bipolar oxide-isolation process technology, and utilizing the innovative architectural features of the PAL22V10, the PAL10H20EV8/PAL10020EV8 represents the most advanced ECL PAL device available on the market today.

The PAL10H20EV8/PAL10020EV8 contains up to twenty inputs and eight outputs. It incorporates AMD's unique output logic macrocell (as in the PAL22V10), which allows the user to define and program the architecture of each output on an individual basis. Each output is user-programmable for either registered or combinatorial operation. Each output also has user-programmable output-polarity control, further simplifying the design. The flexibility of the programmable output logic macrocells permits the system designer to tailor the device to particular application requirements.

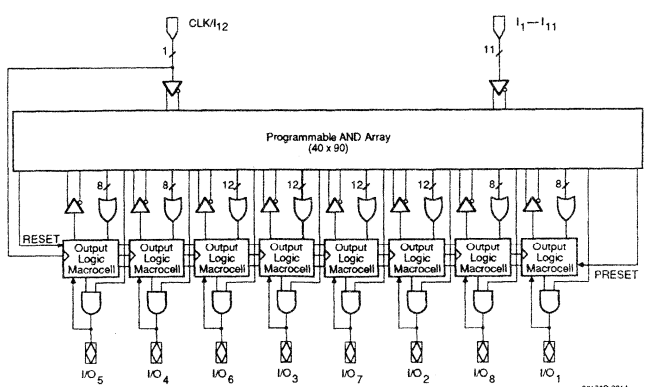
Increased logic power has been built into the PAL10H20EV8/PAL10020EV8 by providing a varied number of logical product terms per output. Four outputs have twelve logical product terms each, and the other four have eight logical product terms each. This varied allocation of logical product terms allows complex functions to be implemented in a single ECL PAL device. Each output also has a separate output-enable product term.

System operation has been enhanced by the addition of asynchronous-PRESET and RESET product terms for the PAL10H20EV8/PAL10020EV8. These product terms are common to all registered outputs.

The PAL10H20EV8/PAL10020EV8 incorporates power-up RESET on all registered outputs. It also has the ability to PRELOAD registers to any desired state during testing. PRELOAD permits full logical verification during testing.

4

BLOCK DIAGRAM

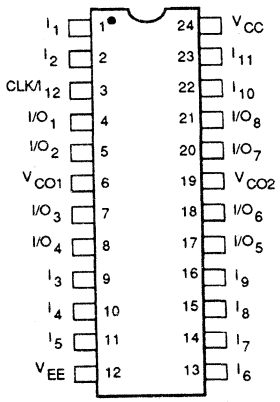


BD007871

Publication # 06176 Rev. C Amendment/0
Issue Date: January 1990

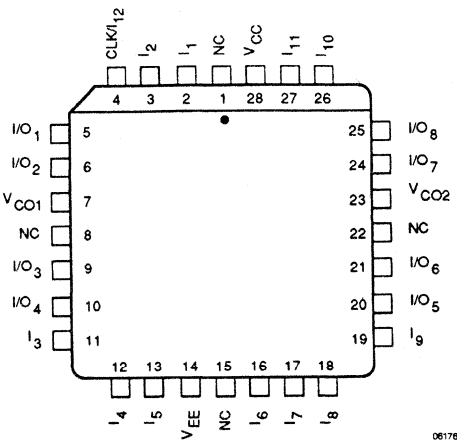
CONNECTION DIAGRAMS
Top View

SKINNYDIP



CD011400

PLCC



06176C-002A

CD011410

Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

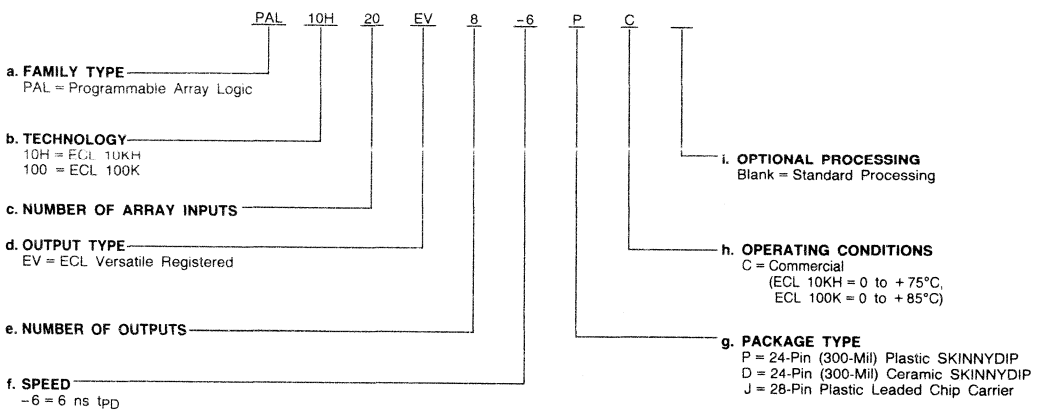
$I_1 - I_{11}$	=	Dedicated Input Pins (11)
$I/O_1 - I/O_8$	=	Bidirectional Input/Output Pins (8)
CLK/I_{12}	=	Clock or Input Pin
NC	=	No Connect
V_{CC}	=	Circuit Ground
V_{CO1}, V_{CO2}	=	Circuit Ground Pins for Outputs (2)
V_{EE}	=	Negative Supply Voltage

ORDERING INFORMATION

PAL Products

AMD PAL products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Speed
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations	
PAL10H20EV8-6	PC, DC, JC
PAL10020EV8-6	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The PAL10H20EV8/PAL10020EV8 is an advanced bipolar ECL PAL device. It contains a programmable fuse array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram in Figure 1 illustrates the basic architecture of the PAL10H20EV8/PAL10020EV8. There are up to twenty external inputs and eight outputs. The inputs are connected to a programmable-AND array. Initially, the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of the fuses, the AND gates may be "connected" to only the true inputs, the complement inputs, or to neither type of input. When both the true and complement fuses are left intact, a logical-FALSE results at the output of the AND gate. An AND gate with all the fuses programmed will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates.

There are an average of ten product terms per OR gate (output), distributed in a varied fashion. Four outputs have eight product terms each while the other four have twelve product terms each. This varied distribution of product terms allows more complex logic functions to be implemented.

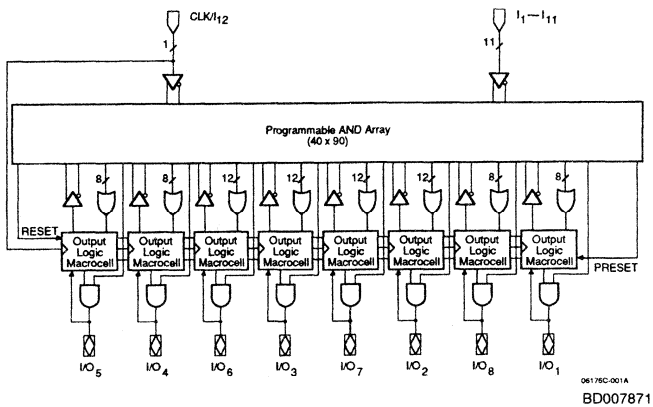


Figure 1. Block Diagram

Output Logic Macrocells

A useful feature of the PAL10H20EV8/PAL10020EV8 is its versatile programmable output logic macrocell. It allows the user to program the outputs on an individual basis in a very flexible manner.

The PAL10H20EV8/PAL10020EV8 output logic macrocell incorporates an edge-triggered register. As shown in the output logic macrocell diagram, each macrocell contains two programmable fuses (S_0 and S_1) for programming the output functions. S_1 controls whether the output will be registered or combinatorial. S_0 controls the output polarity (active-HIGH or active-LOW). Depending on the states of these two fuses, an individual output operates in one of four modes: Registered/Active-LOW, Registered/Active-HIGH, Combinatorial/Active-LOW, and Combinatorial/Active-HIGH. Each output is also provided with a separate output enable product term.

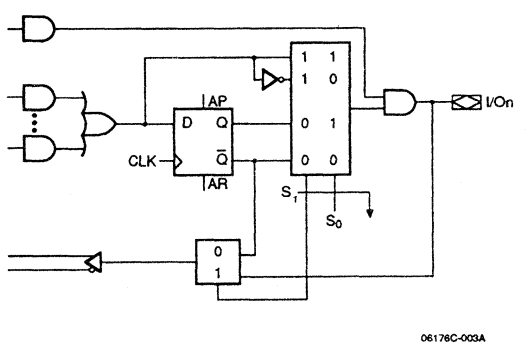
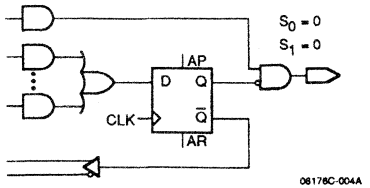
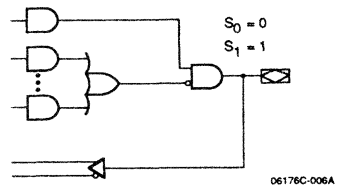


Figure 2. PAL10H20EV8/PAL10020EV8 Output Logic Macrocell



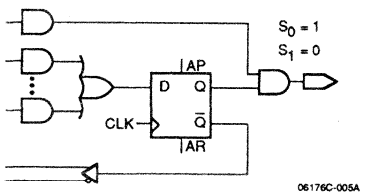
LD001550

Figure 3-1. Registered/Active-LOW



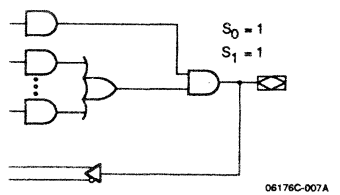
LD001560

Figure 3-3. Combinatorial/Active-LOW



LD001590

Figure 3-2. Registered/Active-HIGH



LD001570

Figure 3-4. Combinatorial/Active-HIGH

S_1	S_0	Output Configuration
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed Fuse
1 = Programmed Fuse

4

Feedback

Another feature of the PAL10H20EV8/PAL10020EV8 output macrocell structure is the flexibility of its feedback selection. The feedback can be from either the I/O line or the registered output. The feedback multiplexer is also controlled by the S_1 fuse. The feedback path changes with the output-mode selection. If the output is selected to be registered, the feedback is registered. If the output is combinatorial, the feedback is from the I/O line. This feature enables the designer to optimally use the device to meet precise application requirements. Additionally, it allows complex control state machines for particular design requirements.

Output Enable

Each of the eight output logic macrocells of the PAL10H20EV8/PAL10020EV8 contains a dedicated product term for the output-enable function. When this product term is asserted LOW, the output is forced into a LOW state where it remains until the output-enable product term goes HIGH.

PRESET and RESET

To improve in-system functionality, the PAL10H20EV8/PAL10020EV8 has additional PRESET and RESET product terms. Common asynchronous RESET and PRESET are provided for all the registers of the PAL10H20EV8/PAL10020EV8. When the asynchronous PRESET product term is asserted HIGH the output registers are loaded with a HIGH; when the RESET product term is asserted HIGH the output registers are loaded with a LOW, both independent of the clock. These functions are particularly useful for system power-on and reset. The registers automatically reset at power-up.

PRELOAD

To simplify testing, the PAL10H20EV8/PAL10020EV8 is designed with PRELOAD circuitry that provides an easy method for testing logic functionality. PRELOAD allows any arbitrary values to be loaded into the PAL device's output registers.

A typical functional-test sequence would be to verify all possible outputs for the device being tested. To verify these transitions requires the ability to set the state registers to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Without PRELOAD capability, it is difficult and in some cases impossible to load an arbitrary present state value into the registers. This can lead to logic verification sequences which are either incomplete or excessively long. With PRELOAD capability, logic verification sequences can be greatly short-

ened, reducing the test time and the development costs, and guaranteeing proper in-system operation.

Security Fuse

A security fuse is provided on each PAL10H20EV8/PAL10020EV8 to protect proprietary logic designs. It is programmed at the same time the array is programmed. The security fuse disables the pattern verification circuitry, and is verified by verifying the whole fuse array as if every fuse were programmed. The security fuse also disables preload.

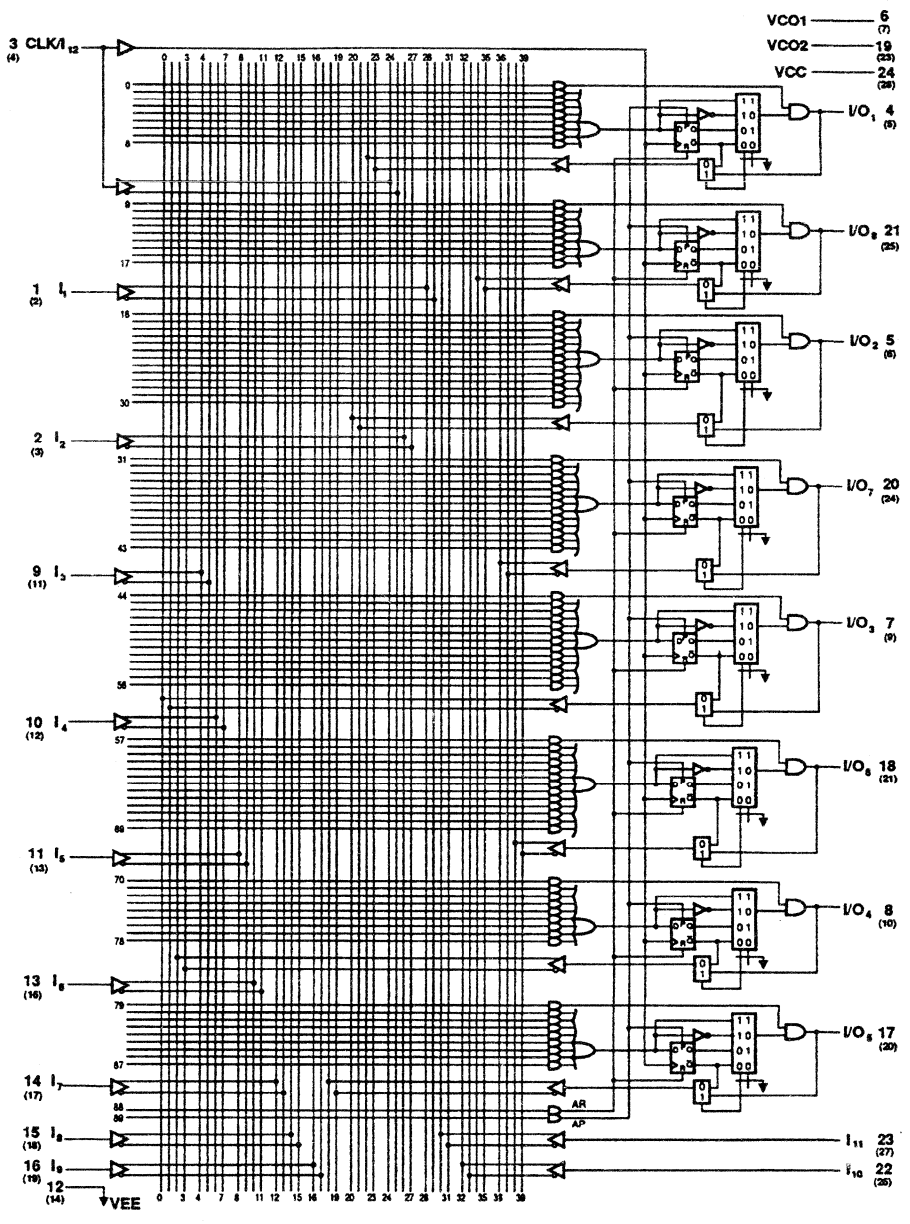
Fabrication

The PAL10H20EV8/PAL10020EV8 is manufactured using Advanced Micro Devices' new oxide-isolation process. This advanced process offers increased density and reduced internal capacitance resulting in the fastest possible programmable logic devices.

The PAL10H20EV8/PAL10020EV8 is fabricated with AMD's fast-programming and highly-reliable fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Testing

The PAL10H20EV8/PAL10020EV8 contains many internal test features, including circuitry and extra fuses which allow AMD to test each part before shipping. This ensures extremely high post-programming functional yields. The test fuses are programmed to assure the ability of each part to perform correct programming. There are extra test words which are preprogrammed during manufacturing and tested to ensure correct logic operation and parametric integrity.



DIP (PLCC) pinouts.

Figure 4. Logic Diagram for PAL10H20EV8/PAL10020EV8

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage (V_{EE})
with Respect to Ground ..... −8 V to 0 V
DC Input Voltage
with Respect to Ground ..... V_{EE} to 0 V
Output Current
-Continuous ..... 35 mA
-Surge ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices — 10KH Devices
Ambient Temperature (T_A) Operating
Air Flow 500 lfpm ..... 0°C to +75°C
Supply Voltage (V_{EE}) ..... −5.46 V to −4.94 V

Commercial (C) Devices — 100K Devices
Ambient Temperature (T_A) Operating
Air Flow 500 lfpm ..... 0°C to +85°C
Supply Voltage (V_{EE}) ..... −4.8 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1, 2)

PAL10H20EV8 (10KH) Devices

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$T_A = 0°C$	−1020	−840	mV
				$T_A = +25°C$	−980	−810	
				$T_A = +75°C$	−920	−735	
V_{OL}	Output LOW Voltage			$T_A = 0°C$	−1950	−1630	mV
				$T_A = +25°C$	−1950	−1630	
				$T_A = +75°C$	−1950	−1600	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$T_A = 0°C$	−1170	−840	mV
				$T_A = +25°C$	−1130	−810	
				$T_A = +75°C$	−1070	−735	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$T_A = 0°C$	−1950	−1480	mV
				$T_A = +25°C$	−1950	−1480	
				$T_A = +75°C$	−1950	−1450	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$T_A = 0°C$		300	µA
				$T_A = +25°C$		300	
				$T_A = +75°C$		300	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$T_A = 0°C$	0.5		µA
				$T_A = +25°C$	0.5		
				$T_A = +75°C$	0.3		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = 0°C$	−260		mA
				$T_A = +25°C$	−260		
				$T_A = +75°C$	−260		

Notes: 1. Designed to meet specifications shown after thermal equilibrium has been established. Guaranteed with transverse air flow exceeding 500 linear feet per minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

DC CHARACTERISTICS over COMMERCIAL operating ranges (Cont'd.) (Notes 1, 2)

PAL10020EV8 (100K) Devices

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$V_{EE} = -4.2$ V	−1025	−880	mV
				$V_{EE} = -4.5$ V	−1025	−880	
				$V_{EE} = -4.8$ V	−1035	−880	
V_{OL}	Output LOW Voltage			$V_{EE} = -4.2$ V	−1810	−1605	mV
				$V_{EE} = -4.5$ V	−1810	−1620	
				$V_{EE} = -4.8$ V	−1810	−1620	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$V_{EE} = -4.2$ V	−1150	−880	mV
				$V_{EE} = -4.5$ V	−1165	−880	
				$V_{EE} = -4.8$ V	−1165	−880	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$V_{EE} = -4.2$ V	−1810	−1475	mV
				$V_{EE} = -4.5$ V	−1810	−1475	
				$V_{EE} = -4.8$ V	−1810	−1490	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$V_{EE} = -4.2$ V		300	μA
				$V_{EE} = -4.5$ V		300	
				$V_{EE} = -4.8$ V		300	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$V_{EE} = -4.2$ V	0.5		μA
				$V_{EE} = -4.5$ V	0.5		
				$V_{EE} = -4.8$ V	0.5		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$V_{EE} = -4.2$ V	−285		mA
				$V_{EE} = -4.5$ V	−285		
				$V_{EE} = -4.8$ V	−285		

Notes: 1. Designed to meet specifications shown after thermal equilibrium has been established. Guaranteed with transverse air flow exceeding 500 linear feet per minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1, 2)

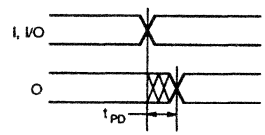
Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Output				6	ns
t_S	Input or Feedback Setup Time			4.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output or Feedback				3.5	ns
t_{AR}/t_{AP}	Asynchronous RESET/PRESET to Registered Output				8	ns
t_{ARW}/t_{APW}	Asynchronous RESET/PRESET Width			6		ns
t_{ARR}/t_{APR}	Asynchronous RESET/PRESET Recovery Time			6		ns
t_{WL}	Clock Width	LOW		2.5		ns
t_{WH}		HIGH		2.5		ns
f_{MAX}	Maximum Frequency	External Feedback	1/(ts+tco)	125		MHz
		Internal Feedback		195		MHz
		No Feedback		200		MHz
t_{EA}	Input to Output Enable				7	ns
t_{ER}	Input to Output Disable				7	ns
t_{RO}	Output Rise Time (20% – 80%)			0.7	2.2	ns
t_{FO}	Output Fall Time (80% – 20%)			0.7	2.2	ns

Notes:

1. Designed to meet specifications shown after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Test conditions: see Setup for Testing Switching Characteristics.

Definitions of Switching Parameters

t_{PD}: Signal propagation delay from an input or an I/O pin through the array to a combinatorial ouput.

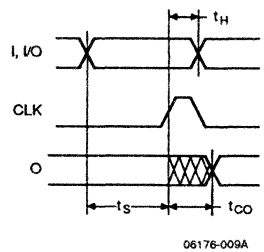


WF027020

t_S: Time that input data must be valid before CLK edge.

t_H: Time that input data must be valid after CLK edge.

t_{CO}: Delay between clock edge and data appearing at the output.

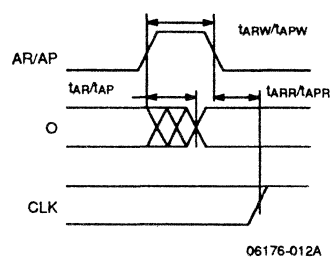


WF027030

t_{AR}/t_{AP}: Delay from an input or I/O pin activating asynchronous reset or preset to data appearing at a registered output.

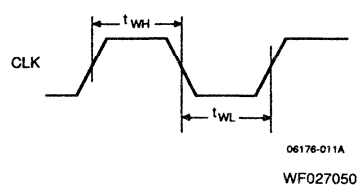
t_{ARW}/t_{APW}: The minimum input or I/O pin pulse width needed to activate asynchronous reset or preset.

t_{ARR}/t_{APR}: Time that input or I/O pin must inactivate asynchronous reset or preset before CLK edge.



t_{WL}: The minimum LOW clock width.

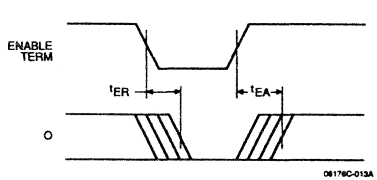
t_{WH}: The minimum HIGH clock width.



WF027050

t_{EA}: Delay between input or I/O pin activating enable term and data appearing at outputs.

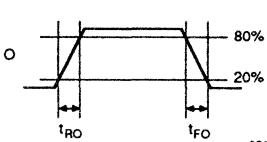
t_{ER}: Delay between input or I/O pin deactivating enable term and outputs going LOW.



WF026800

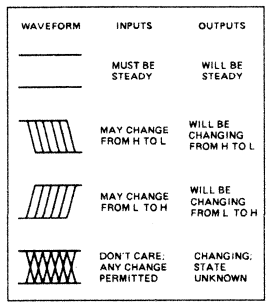
t_{RO}: Time taken for an output signal voltage to swing from 20% to 80% of the full logic swing.

t_{FO}: Time taken for an output signal voltage to swing from 80% to 20% of the full logic swing.



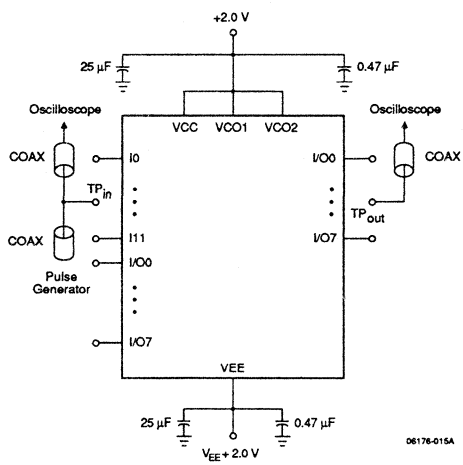
WF027060

KEY TO SWITCHING WAVEFORMS



KS000012

Setup for Testing Switching Characteristics



LS003460

Each oscilloscope channel input should have a 50 Ω termination to ground. Oscilloscope bandwidth should be a least 1 GHz.

The pulse generator should be capable of providing 1.5 ns rise and fall times (20% to 80%).

All input and output cables should be equal lengths of matched 50 Ω coaxial cable. Wire lengths between input (or I/O) pins and TP_{in} or between output pins and TP_{out} should be less than 1/4 in. long. Stubs should be avoided if possible; unavoidable stubs should be less than 2 in. long.

Used inputs that are not switching should be forced to V_{IL} or V_{IH}.

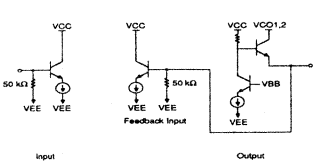
Outputs that are switching but not sensed should be terminated through 50 Ω to ground.

Unused inputs and outputs may be left open.

Note that all voltages are shifted by +2.0 V with respect to normal ECL operating conditions in order to take advantage of the input terminations of the oscilloscope.

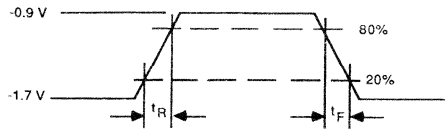
Timing thresholds in this configuration are taken to be +0.7 V.

Input and Output Equivalent Schematics



SWITCHING TEST WAVEFORM

INPUT PULSE



06176C-014A
WF023080

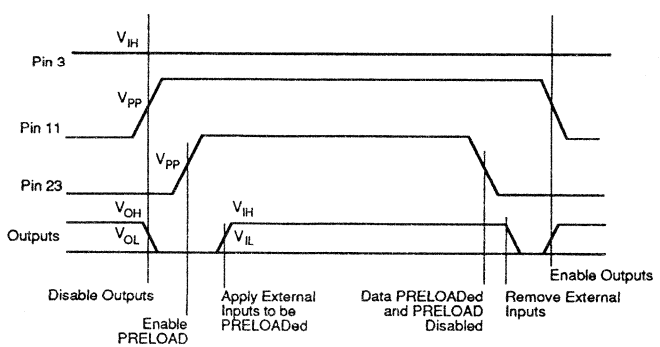
$t_R = t_F = 2.2$ ns Max. for 10KH
$t_R = t_F = 1.0$ ns Max. for 100K

PRELOAD OF REGISTERED OUTPUTS

The PAL10H20EV8/PAL10020EV8 registered outputs are provided with circuitry to allow loading each register to either a HIGH or LOW state. This simplifies testing since any state can be loaded into the registers to control test sequencing. The pin levels necessary to perform the PRELOAD function are detailed below.

PRELOAD is accessed by applying V_{PP} on pin 23. The data to be preloaded is set on the output pins. Bringing pin 23 back to a logic-LOW level loads the data into the output registers. During PRELOAD the outputs are disabled by a supervoltage on pin 11.

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Level During PRELOAD and Verify	−1.1	−0.9	−0.7	V
V_{IL}	Input LOW Level During PRELOAD and Verify	−1.85	−1.65	−1.45	V
V_{PP}	Voltage Applied to Pins 11 and 23 (DIP)	1.8	2.0	2.2	V



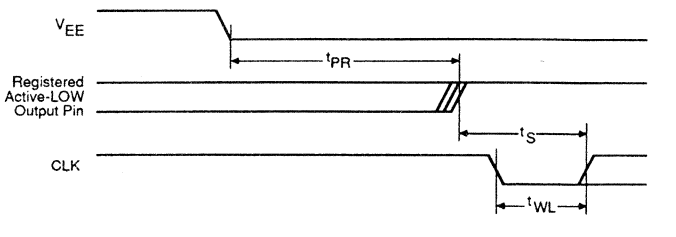
06176-016A
WF027121

PRELOAD Waveform

POWER-UP RESET

The registers in the PAL10H20EV8/PAL10020EV8 have been designed with the capability to RESET during system power-up. Following power-up, all registers will be LOW. The output state will depend upon the state of the output buffer and the polarity fuse. This feature provides extra flexibility to the designer. A timing diagram and a parameter table are shown below. Due to the asynchronous operation of the power-up RESET and the wide range of ways V_{EE} can fall to steady state, two conditions are required to insure a valid power-up RESET. These conditions are:

1. The V_{EE} fall must be monotonic.
2. Following RESET, the CLK input must not be driven from LOW-to-HIGH until all applicable input and feedback setup times are met.



06176C-017A

WF026070

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t_{PR}	Power-Up RESET Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_{WL}	Clock Width				

Am2064/Am2018

Programmable Gate Array

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Up to 1800 usable gate equivalence for higher board densities**
- **TTL or CMOS input threshold levels allow for more board flexibility**
- **Field programmable gate array means easy and quick design modifications**
- **Reconfigurable device for multiple in-system patterns**
- **Readback feature allows you to check configuration data**

GENERAL DESCRIPTION

The Logic Cell Array™ (LCA)™ is a high density, CMOS programmable gate array. It is composed of an interior array of logic blocks, surrounded by a ring of I/O interface blocks. Unlike conventional gate arrays, however, the definition of logic functions and interconnections in an LCA device does not require any custom factory fabrication. The configurable logic blocks (CLBs), I/O blocks (IOBs), and interconnection resources of the device are completely user-configurable. Each device is identical until it is configured. When configured, the LCA then begins operating according to the logic defined by the user. An LCA can either load its configuration data automatically from an external EPROM or have the data loaded under microprocessor control. The LCA is configured each time it is powered up, and offers the user the unique benefit of being able to reconfigure in-system at any time during operation.

The Logic Array is a CMOS, static RAM-based device. Static RAM technology is a mature technology that has been in production for years, with millions of operating device hours. Compared to other programming alternatives, static memory provides the best combination of high density, high performance, high reliability, and comprehensive testability. The LCA is the first device to apply the benefits of static RAM technology to overcome the disadvantages of conventional gate arrays. The static memory cells used for the configuration memory of the LCA have been designed specifically for high reliability and noise immunity. The memory cell of the LCA is much more stable than a typical high-speed conventional memory cell.

PGA development system software is available for all phases of the design cycle. From design entry through simulation, both logic and timing, automatic placement and routing, and in-circuit emulation, software that operates on an IBM®-PC-AT™ or compatible system speeds the design process. For users of Daisy™ or Mentor™ workstations, interfaces for PGA design are also available from AMD. A valid workstation interface is available from Valid Logic Systems.

4

Part Number	Logic Capacity (Usable Gates)	Configurable Logic Blocks	Configurable I/O Blocks	Configuration Program (Bits)
Am2064	1200	64	58	12,048
Am2018	1800	100	74	17,888

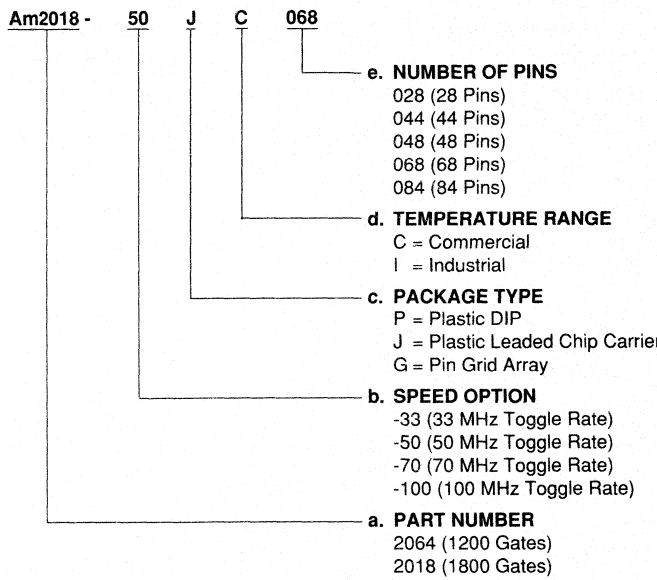
Publication # 10352 Rev. B Amendment /0
Issue Date: **May 1989**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Package Type**
d. **Temperature Range**
e. **Number of Pins**



PACKAGE AVAILABILTY

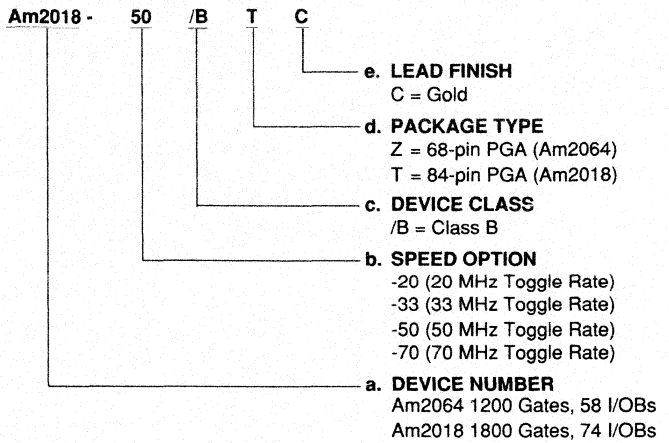
PART NUMBER	28-PIN PLCC	44-PIN PLCC	48-PIN PLASTIC DIP	68-PIN PLCC	68-PIN PGA	84-PIN PLCC	84-PIN PGA
Am2064	X		X	X	X		
Am2018		X		X	X	X	X

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
Am2064-20 Am2064-33 Am2064-50	/BZC
Am2018-20 Am2018-33 Am2018-50 Am2018-70	/BTC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

SILICON MENU

AMD Part	Organization	Equivalent Gate Count	Configurable Logic Block	User I/Os	Configuration Program Bits	Max Standby Current (CMOS Inputs)	Max Standby Current (TTL Inputs)	Packages	Max Toggle Rate Between CLBs
Am2064-20 Am2018-20	8x8 10x10	1200 1800	64 100	58 74	12048 17888	10 mA 15 mA	10 mA 10 mA	68PGA 84PGA	20 MHz 20 MHz
Am2064-33 Am2018-33	8x8 10x10	1200 1800	64 100	58 74	12048 17888	10 mA 15 mA	10 mA 10 mA	68PGA 84PGA	33 MHz 33 MHz
Am2064-50 Am2018-50	8x8 10x10	1200 1800	64 100	58 74	12048 17888	10 mA 15 mA	10 mA 10 mA	68PGA 84PGA	50 MHz 50 MHz
Am2018-70	10x10	1800	100	74	17888	15 mA	10 mA	84PGA	70 MHz

FUNCTIONAL DESCRIPTION

The general structure of a Logic Cell Array is shown in Figure 1. The elements of the array include three categories of user-programmable elements: I/O Blocks, Configurable Logic Blocks and Programmable Interconnections. The I/O Blocks provide an interface between the logic array and the device package pins. The Configurable Logic Blocks perform user-specified logic functions, and the interconnect resources are programmed to form networks that carry logic signals among blocks.

Configuration of the Logic Cell Array is established through a distributed array of memory cells. The PGA Development System generates the program used to configure the Logic Cell Array. The Cell Array includes logic to implement automatic configuration.

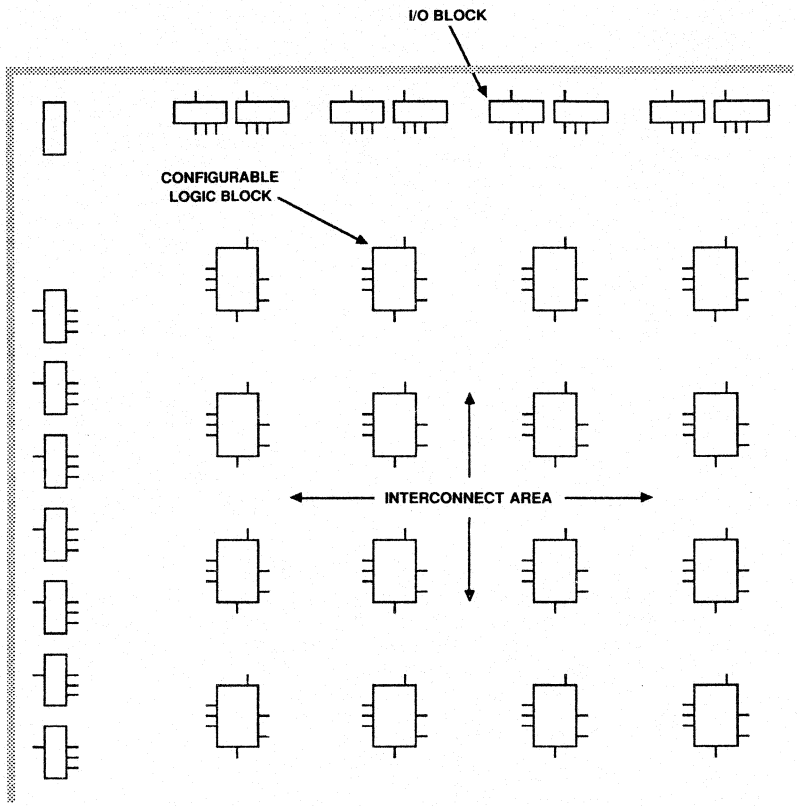


Figure 1. Logic Cell Array Structure

Configuration Memory

The configuration of the Advanced Micro Devices' Logic Cell Array is established by programming memory cells which determine the logic functions and interconnections. The memory loading process is independent of the user logic functions.

The static memory cell used for the configuration memory in the Logic Cell Array has been designed specifically for high reliability and noise immunity. Based on this design, integrity of the LCA configuration memory is assured even under adverse conditions. Compared with other programming alternatives, static memory provides the best combination of high density, high performance, high reliability and comprehensive testability. As shown in Figure 2, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing data to the cell. The cell is only written during configuration and only read during readback. During normal operation the pass transistor is "off" and does not affect the stability of the cell. This is quite different from the normal operation of conventional memory devices, in which the cells are continuously read and written.

The outputs Q and $\overline{Q}$ control pass-transistor gates directly. The absence of sense amplifiers and the output capacitive load provide additional stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. In reliability testing no soft errors have been observed, even in the presence of very high doses of alpha radiation.

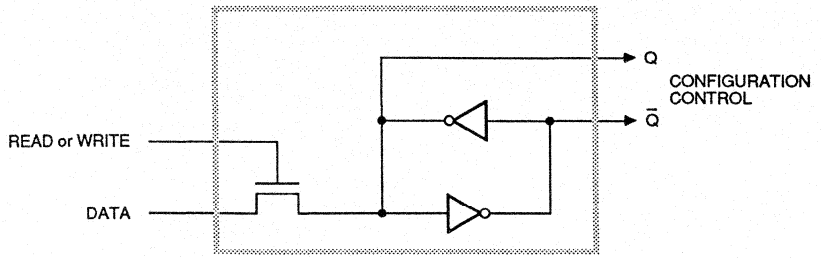


Figure 2. Configuration Memory Cell

Input/Output Block

Each user-configurable I/O block (IOB) provides an interface between the external package pin of the device and the internal logic. Each I/O block includes a programmable input path and a programmable output buffer. It also provides input clamping diodes to provide protection from electrostatic damage, and circuits to protect the LCA from latch-up due to input currents. Figure 3 shows the general structure of the I/O block.

The input buffer portion of each I/O block provides threshold detection to translate external signals applied to the package pin to internal logic levels. The input buffer threshold of the I/O blocks can be programmed to be compatible with either TTL (1.4 V) or CMOS (2.2 V) levels. The buffered input signal drives both the data input of an edge-triggered D-type flip-flop and one input of a two-input multiplexer. The output of the flip-flop provides the other input to the multiplexer. The user can select either the direct input path or the registered input, based on the content of the memory cell controlling the multiplexer. The I/O blocks along each edge of the die share common clocks. The flip-flops are reset during configuration as well as by the active-low chip $\overline{\text{RESET}}$ input.

Output buffers in the I/O blocks provide 4-mA drive for high fan-out CMOS or TTL-compatible signal levels. The output data (driving I/O block pin O) is the data source for the I/O block output buffer. Each I/O block output buffer is controlled by the contents of two configuration memory cells which turn the buffer ON or OFF or select logical three-state buffer control. The user may also select the output buffer three-state control (I/O block pin TS). When this I/O block output control signal is HIGH (a logic "1") the buffer is disabled and the package pin is high-impedance.

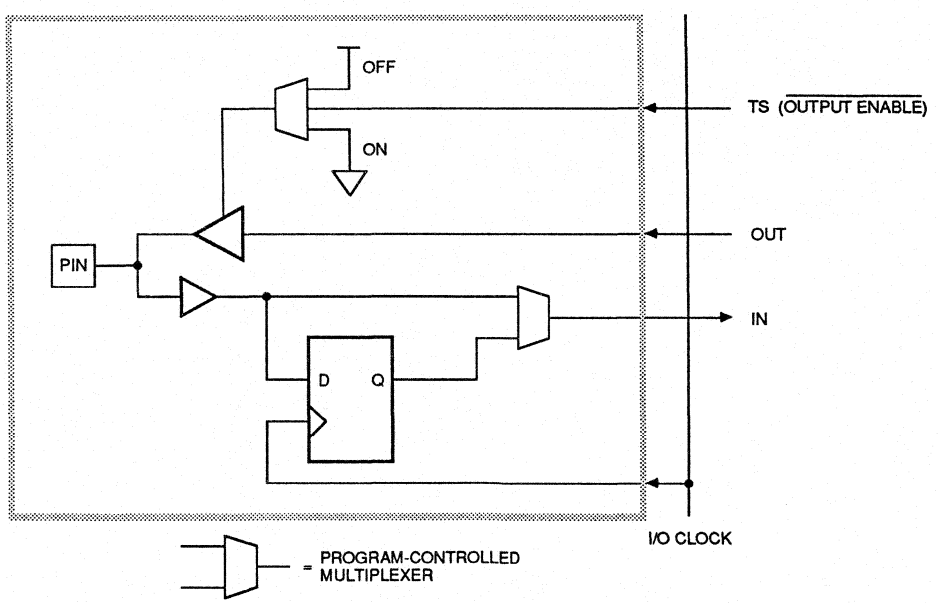


Figure 3. I/O Block

Configurable Logic Block

An Array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix in the center of the device. The Am2064 has sixty-four such blocks arranged in an eight-row by eight-column matrix. The Am2018 has one hundred logic blocks arranged in a ten by ten matrix. Each logic block has a combinatorial logic section, a storage element, and an internal routing and control section. Each CLB has four general-purpose inputs; A, B, C, and D; and a special clock input (K), which may be driven from the interconnect adjacent to the block. Each CLB also has two outputs, X and Y, which may drive interconnect networks. Figure 4 shows the resources of a Configurable Logic Block.

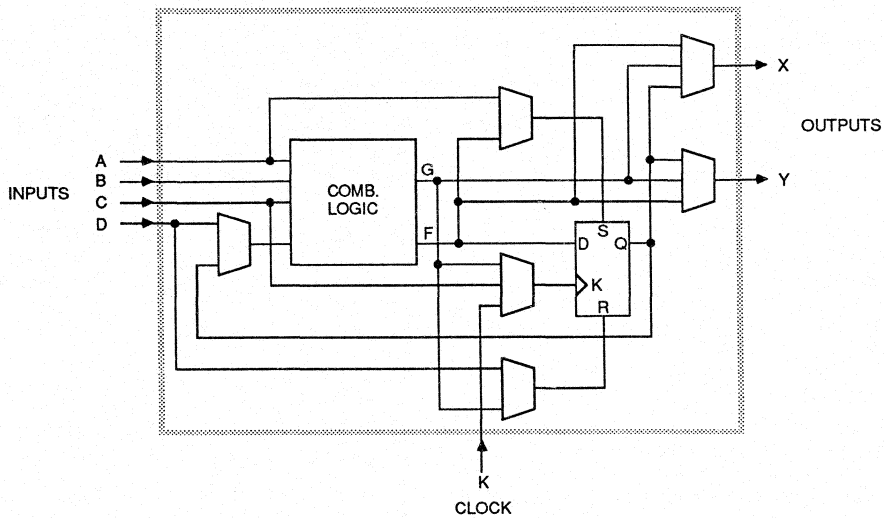


Figure 4. Configurable Logic Block

The logic block combinatorial logic uses a table look-up memory to implement Boolean functions. This technique can generate any logic function of up to four variables with a high-speed sixteen-bit memory. The propagation delay through the combinatorial network is independent of the function generated. Each block can perform any function of four variables or any two functions of three variables each. The variables may be selected from among the four inputs and the block's storage element output "Q". Figure 5 shows various options which may be specified for the combinatorial logic.

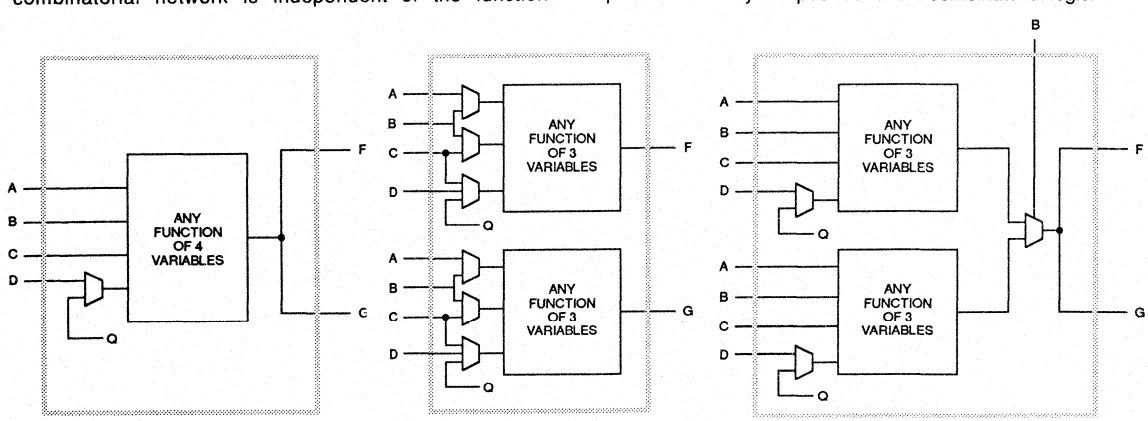


Figure 5. CLB Combinatorial Logic Options

If the single four-variable configuration is selected (Option 1), the F and G outputs are identical. If the two-function alternative is selected (Option 2), logic functions F and G may be independent functions of three variables each. The three variables can be selected from among the four logic block inputs and its storage element output Q. A third form of the combinatorial logic (Option 3) is a special case of the two-function form in which the B input dynamically selects between the two function tables providing a single merged logic function output. This dynamic selection allows some five-variable functions to be generated from the four block inputs and storage element Q. Combinatorial functions are restricted in that one may not use both its storage element output Q and the input variable of the logic block pin D in the same function.

If used, the storage element in each Configurable Logic Block (Figure 6) can be programmed to be either an edge-sensitive D-type flip-flop or a level-sensitive D latch. The clock or enable for each storage element can be selected from:

- The special-purpose clock input K
- The general-purpose input C
- The combinatorial function G

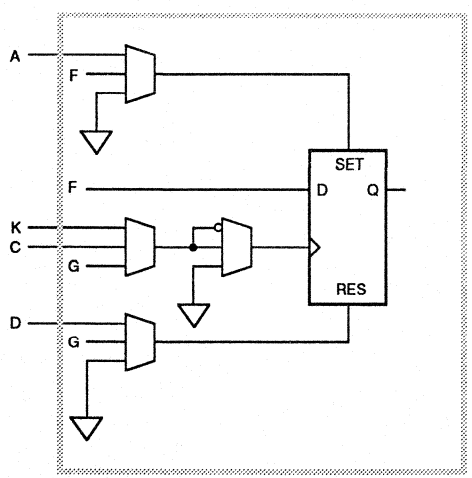


Figure 6. CLB Storage Element

The user may also select the clock active sense within each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device.

The storage element data input is supplied from the function F output of the combinatorial logic. Asynchronous SET and RESET controls are provided for each storage element. The user may enable these controls independently and select their source. They are active-high inputs and the asynchronous reset is dominant. The storage elements are reset by the active-low chip $\overline{\text{RESET}}$ pin as well as by the initialization phase preceding configuration. If the storage element is not used, it is disabled.

The two block outputs, X and Y, can be driven by either the combinatorial functions, F or G, or the storage element output Q (Figure 4). Selection of the outputs is completely interchangeable and may be made to optimize routing efficiencies of the networks interconnecting the logic blocks and I/O blocks.

Programmable Interconnect

Programmable Interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into desired networks. All interconnections are composed of metal segments, with programmable switching points provided to implement the necessary routing. Three types of resources accommodate different types of networks:

- General purpose interconnect
- Long lines
- Direct connection

General-Purpose Interconnect

General-purpose interconnect, as shown in Figure 7a, is composed of four horizontal metal segments between the rows and five vertical metal segments between the columns of logic and I/O blocks. Each segment is only the "height" or "width" of a logic block. Where these segments would cross at the intersections of rows and columns, switching matrices are provided to allow interconnections of metal segments from the adjoining rows and columns. Switches in the switch matrices and on block outputs are specially designed transistors, each controlled by a configuration bit.

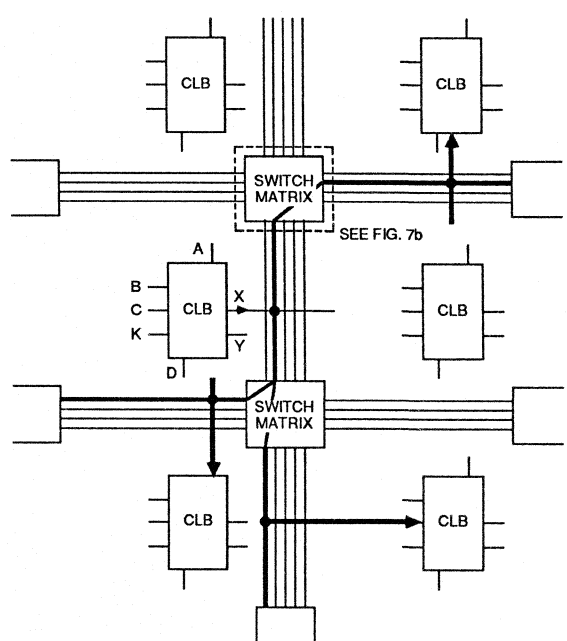
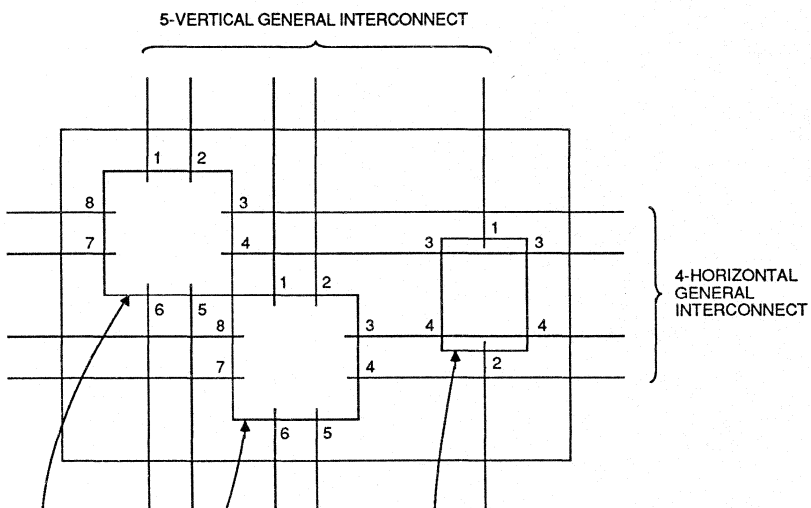


Figure 7a. General-Purpose Interconnect

Logic block output switches provide contacts to adjacent general interconnect segments and therefore to the switching matrix at each end of those segments. A switch matrix can connect an interconnect segment to other segments to form a network. Figure 7a shows the general interconnect used to route a signal from one logic block to three other logic blocks. As shown, combinations of closed switches in a switch matrix allow multiple branches for each network. The inputs of the logic or I/O blocks are multiplexers that can be programmed with configuration bits to select an input network from the adjacent interconnect segments. Since the switch connections to block inputs are unidirectional (as are block outputs) they are usable *only* for input connections. The development system software provides automatic routing of these interconnections. Interactive routing is also available for design optimization. This is accomplished by selecting a network and then toggling the states of the interconnect points by selecting them with the "mouse". In this mode, the connections through the switch matrix may be established by selecting pairs of matrix pins. The switching matrix combinations are indicated in Figure 7b.

Special buffers within the interconnect area provide periodic signal isolation and restoration for higher general interconnect fan-out and better performance. The repowering buffers are bidirectional, since signals must be able to propagate in either direction on a general interconnect segment. Direction controls are automatically established by the Logic Cell Array development system software. Repowering buffers are provided only for the general-purpose interconnect since the direct and long-line resources do not exhibit the same R-C delay accumulation. The Logic Cell Array is divided into nine sections with buffers automatically provided for general interconnect at the boundaries of these sections. These boundaries can be viewed with the development system. For routing within a section, no buffers are used. The delay calculator of the PGA Development System automatically calculates and displays the block, interconnect, and buffer delays for any selected paths.



FROM / TO

TO \ FROM	1	2	3	4	5	6	7	8
1	■	0	1	0	1	1	1	1
2	0	■	1	1	1	1	0	1
3	1	1	■	0	1	0	1	1
4	0	1	0	■	1	1	1	1
5	1	1	1	1	■	0	1	0
6	1	1	0	1	0	■	1	1
7	1	0	1	1	1	1	■	0
8	1	1	1	1	0	1	0	■

FROM / TO

TO \ FROM	1	2	3	4
1	■	1	1	1
2	1	■	1	1
3	1	1	■	0
4	1	1	0	■

1 = VALID CONNECTION
0 = INVALID CONNECTION

Figure 7b. Interconnection Switching Matrix

Long Lines

Long lines, shown in Figure 8a, run both vertically and horizontally the height or width of the interconnect area. Each vertical interconnection column has two long lines; each horizontal row has one, with an additional long line adjacent to each set of I/O blocks. The long lines bypass the switch matrices and are intended primarily for signals that must travel a long distance or must have minimum skew among multiple destinations.

A global buffer in the Logic Cell Array is available to drive a single signal to all B and K inputs of logic blocks. Using the global buffer for a clock provides a very low skew, high fan-out synchronized clock for use at any or all of the logic blocks. At each block, a configuration bit for the K input to the block can select this global line as the storage element clock signal. Alternatively, other clock sources can be used.

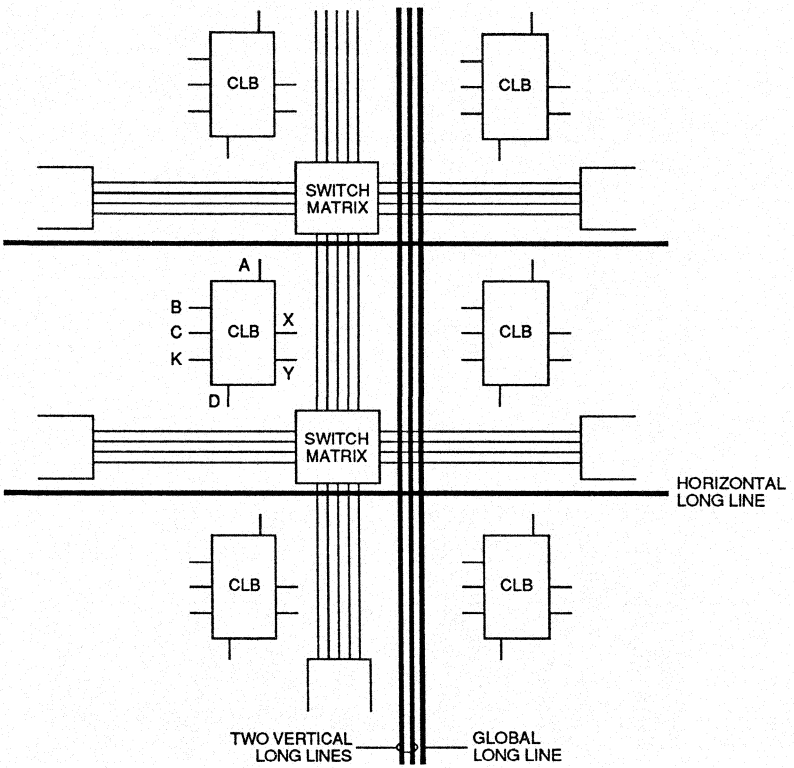


Figure 8a. Long Line Interconnect

A second buffer below the bottom row of the array drives a horizontal long line which, in turn, can drive a vertical long line in each interconnection column. This alternate buffer also has low skew and high fan-out capability. The network formed by this alternate buffer's long lines can be selected to drive the B, C or K inputs of the logic blocks. Alternatively, these long lines can be driven by a logic or I/O block on a column-by-column basis. This capability provides a common, low-skew clock or control line within each column of logic blocks. Interconnections of these long lines are shown in Figure 8b.

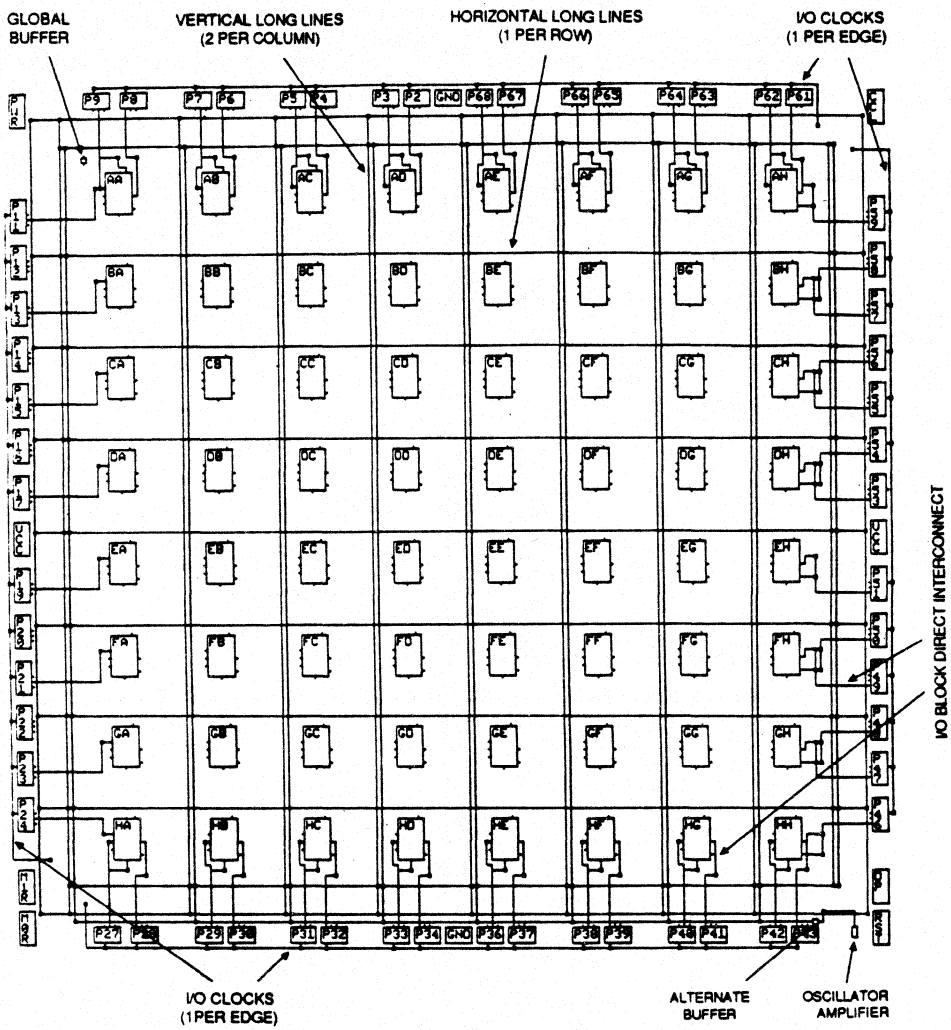


Figure 8b. Am2064 Long Lines, I/O Clocks, I/O Direct Interconnect

Direct Interconnect

Direct interconnect, shown in Figure 9, provides the most efficient implementation of networks between adjacent logic or I/O blocks. Signals routed from block to block by means of direct interconnect exhibit minimum interconnect propagation and use minimum interconnect resources. For each CLB, the X output may be connected directly to the C or D inputs of the CLB above and to the A or B inputs of the CLB below it. The Y output can use direct interconnect to drive the B input of the block immediately to its right. Where logic blocks are adjacent to I/O blocks, direct connect is provided to the I/O block input (I) on the left edge of the die, the output (O) on the right edge, or both on I/O blocks at the top and bottom of the die. Direct interconnections of I/O blocks with CLBs are shown in Figure 8b.

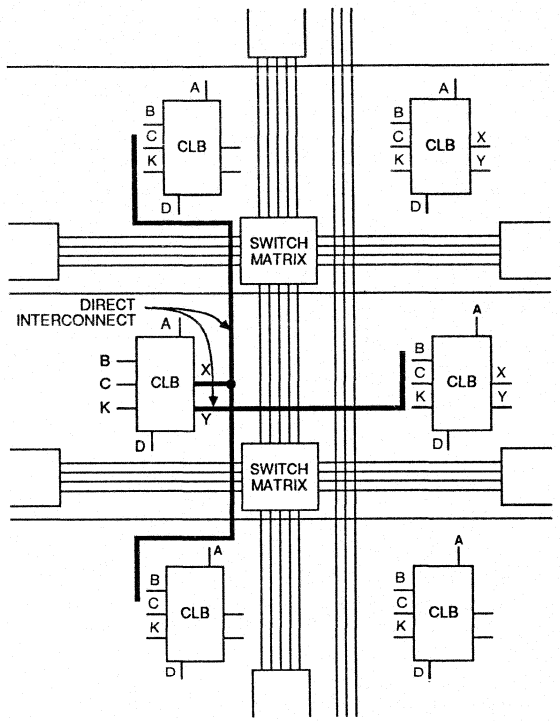
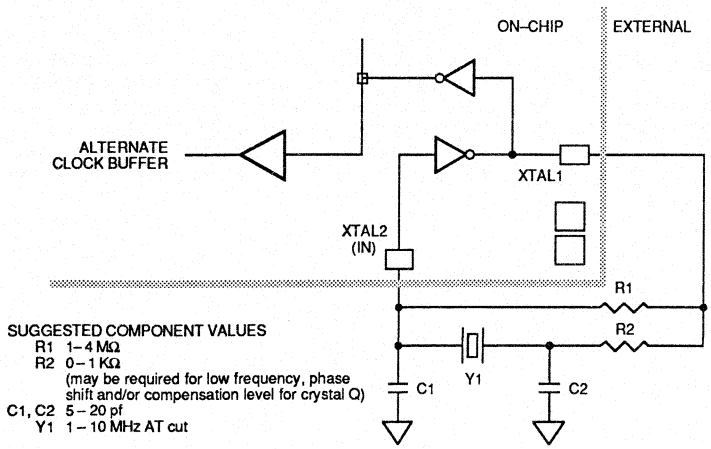


Figure 9. Direct Interconnect

Crystal Oscillator

An internal high-speed inverting amplifier is available to implement an on-chip crystal oscillator. It is associated with the auxiliary clock buffer in the lower right corner of the die. When configured to drive the auxiliary clock buffer, two special adjacent user I/O blocks are also configured to connect the oscillator amplifier with external crystal oscillator components, as shown in Figure 10. This circuit becomes active before configuration is complete in order to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. The feedback resistor R1 between output and input, biases the amplifier at threshold. It should be as large a value as practical to minimize loading of the crystal. The inversion of the amplifier, together with the R-C networks and crystal, produces the 360-degree phase shift of the Pierce oscillator.

A series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control or crystal resistance matching or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be adjusted by the ratio of C2/C1. The amplifier is designed to be used over the range from 1 MHz up to one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Operation at frequencies above 20 MHz generally requires a crystal to operate in a third overtone mode, in which the fundamental frequency must be suppressed by the R-C networks. When the amplifier does not drive the auxiliary buffer, these I/O blocks and their package pins are available for general user I/O.



	XTAL1	XTAL2
28 PLCC	20	17
44 PLCC	29	26
48 DIP	33	30
68 PLCC	46	43
68 PGA	J10	L10
84 PLCC	56	53
84 PGA	K11	L11

Figure 10. Crystal Oscillator

Power

Power Distribution

Power for the LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. For packages having more than forty-eight pins, two V_{CC} pins and two ground pins are provided (see Figure 11). Inside the LCA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are appropriately decoupled. Typically a 0.1-µF capacitor connected between the V_{CC} and ground pins near the package will provide adequate decoupling.

Output buffers capable of driving the specified 4-mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily-loaded output buffers near the ground pads. Multiple VCC and ground pin connections are required for package types which provide them.

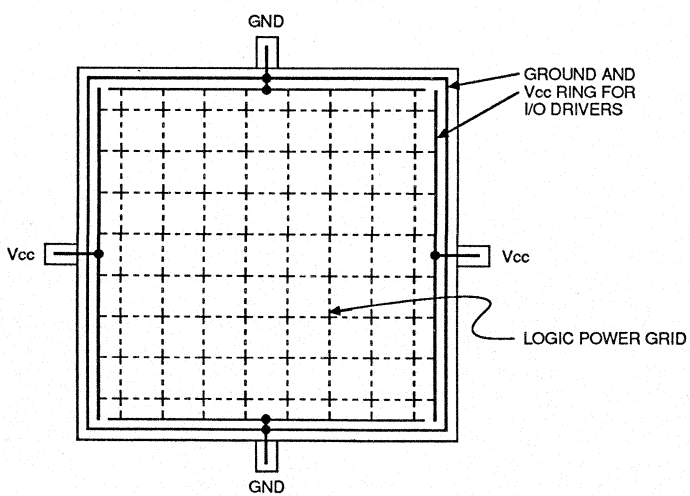


Figure 11. LCA Power Distribution

Am3020/3030/3042/3064/3090

Am3000 Series Family of Programmable Gate Arrays

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Second generation user-programmable gate array**
- **Flexible array architecture**
- **High performance**
  - 50, 70, 100 MHz commercial products
  - 50, 70 MHz military products
- **Improved interconnection resources**
- **Density of up to 9000 gates**
- **100% factory pre-tested**
- **Selectable configuration modes**
- **100% compatibility with AMD PGA development tools**
- **Standard PROM file interface**
- **Off the shelf availability**

GENERAL DESCRIPTION

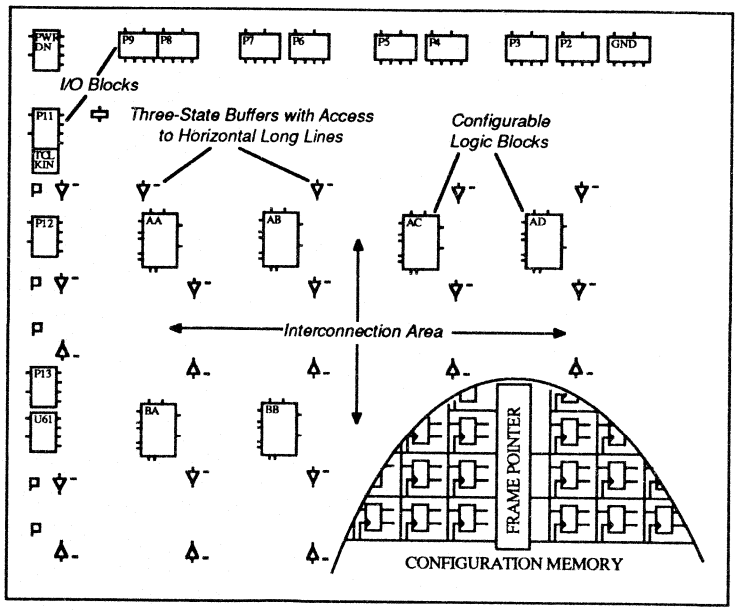
The Am3000 Series Logic Cell™ Array (LCA) is a high-performance, second generation user-programmable gate array. The array contains three types of configurable elements that are customized in accordance with the user-defined system design; a perimeter of Input/Output Blocks (IOBs), a core array of Configurable Logic Blocks (CLBs), and interconnection resources.

The final configuration of the three main programmable elements is determined by the user and easily implemented by AMD user-programmable gate array design tools.

AMD's development tools let users produce a complete design, from schematic capture through device customization, on an IBM PC-AT™ compatible computer. LCA macro libraries and interface software are also available to support schematic capture and simulation on popular CAE workstations.

4

BLOCK DIAGRAM



Logic Cell is a trademark of Xilinx, Inc.

IBM PC-AT is a trademark of International Business Machines Corp.

Publication # 10642 Rev. B Amendment /0
Issue Date: August 1989

PRODUCT SELECTOR GUIDE

BASIC ARRAY	LOGIC CAPACITY (USABLE GATES)	CONFIGURABLE LOGIC BLOCKS	USER I/OS	PROGRAM DATA (BITS)
Am3020	2000	64	64	14779
Am3030	3000	100	80	22176
Am3042	4200	144	96	30784
Am3064	6400	224	120	46064
Am3090	9000	320	144	64160

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Number of Pins

AM3020 -50 J C 068

e. NUMBER OF PINS
068 (68 pins)
084 (84 pins)
132 (132 pins)*
175 (175 pins)

d. TEMPERATURE RANGE
C = Commercial (0°C to 70°C)
I = Industrial (-40°C to +85°C)

c. PACKAGE TYPE
J = Plastic Leaded Chip Carrier
G = Pin Grid Array

b. SPEED OPTION
-50 (50 MHz toggle rate)
-70 (70 MHz toggle rate)
-100 (100 MHz toggle rate)

a. DEVICE NUMBER/DESCRIPTION
Am3000 Series of Programmable Gate Arrays
Am3020 (2000 gates)
Am3030 (3000 gates)
Am3042 (4200 gates)
Am3064 (6400 gates)
Am3090 (9000 gates)

Package Availability Guide

	68-pin PLCC	68-pin PGA	84-pin PLCC	84-pin PGA	175-pin PGA
3020	x	x	x	x	
3030			x	x	
3042			x	x	
3064	**	**	**	**	**
3090					x

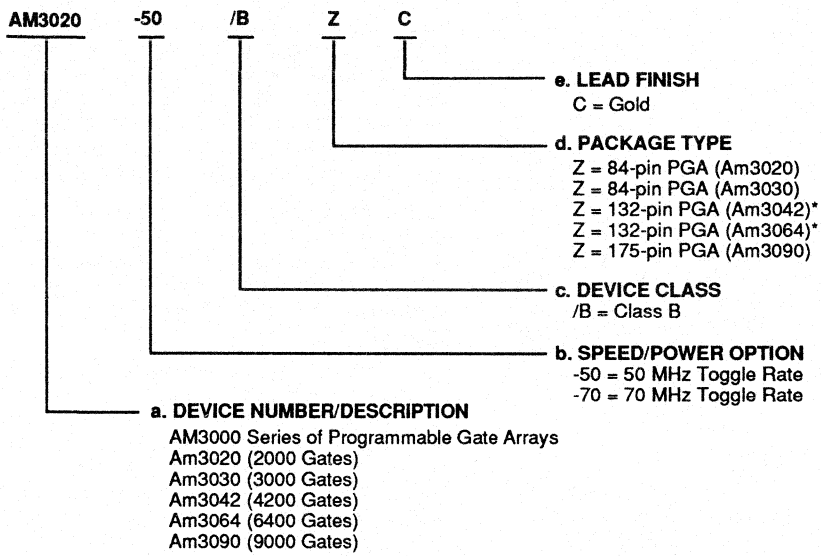
*In development

** Package types for the Am3064 are to be determined

ORDERING INFORMATION
Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed/Power Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
Am3020-50	/BZC
Am3020-70	
Am3030-50	
Am3030-70	
Am3042-50	
Am3042-70	
Am3064-50	
Am3064-70	
Am3090-50	
Am3090-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL–STD–883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

*In development

ARCHITECTURE

Functional Description

The perimeter of configurable IOBs provides a programmable interface between the internal logic array and the device package pins. The array of CLBs performs user-specified logic functions. The interconnections are programmed to form networks, carrying logic signals among blocks. This is analogous to printed circuit board traces connecting MSI/SSI packages.

The logic functions of these blocks are determined by programmed look-up tables. Functional options are performed by program-controlled multiplexers. Interconnecting networks between blocks are composed of metal segments joined by program-controlled pass transistors. These LCA functions are activated by a configuration bit stream that is loaded into an internal, distributed array of configuration memory cells. The configuration bit stream is loaded into the LCA device at power-up and can be reloaded on command. The LCA device includes logic and control signals for automatic or passive configuration. Configuration data can be either bit serial or byte parallel. The PGA Development System generates the configuration bit stream used to configure the LCA device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the LCA's configuration memory has been designed specifically for high reliability and noise immunity, ensuring integrity even under adverse conditions. Static memory provides the best combination of high density, high performance, high reliability, and comprehensive testability. As shown below, the basic memory cell consists of two CMOS inverters and a pass transistor, which is used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the pass transistor is off and does not affect the stability of the cell. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and re-written.

A static configuration memory cell is loaded with one bit of the configuration bit stream and controls one data selection in the LCA device. The memory cell outputs Q and $\overline{Q}$ use full Ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load, together with the absence of address decoding and sense amplifiers, gives the cell high stability.

Due to the structure of the configuration memory cells, they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. No soft errors have been observed in reliability testing, even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic uses framing information, which is embedded in the configuration data by the PGA Development System, to direct memory cell loading. The serial data framing and length count preamble provide synchronous, serial, or daisy-chained compatibility with various AMD programmable gate arrays.

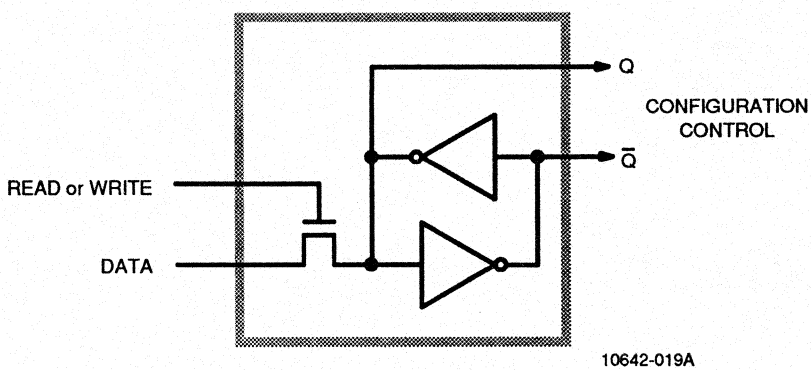


Figure 1. Basic Memory Cell

Input/Output Blocks

Each user-configurable IOB, shown below, provides an interface between the device's external package pin and the internal user logic. Each IOB includes both registered and direct input paths and each provides a programmable three-state output buffer that can be driven by a registered or direct output signal. Configuration options allow a choice of polarity on the output and three-state control signals, a controlled slew rate, and a high impedance pull-up. Each input circuit provides input clamping diodes for electrostatic protection, and circuits to inhibit latch-up produced by input currents.

The input buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed for TTL or CMOS voltage levels. The buffered input signal drives the data input of a storage element that can be configured as a positive edge-triggered D flip-flop, or a level-transparent latch. The sense of the clock can be inverted (negative edge/high transparent) as long as all IOBs on the same clock net use the same clock sense. Clock/load signals, IOB pins .ik and .ok, can be chosen from either of two available metal lines along each die edge. I/O storage elements are reset during configuration or by the active low chip $\overline{\text{RESET}}$ input. Both direct input from IOB pin .i, and registered input from IOB pin .q signals are available for interconnect.

For reliable operation, inputs should have transition times less than 100 ns and should not be left undriven, or floating. Unused CMOS input-pin circuits can be at threshold and produce oscillations. This produces additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces input noise sensitivity. Each user IOB includes a programmable high impedance pull-up resistor that can be selected by the bit stream and which provides a constant HIGH for otherwise undriven package pins. Although the LCA device provides circuitry for input protection against electrostatic discharge, normal CMOS handling precautions should be observed.

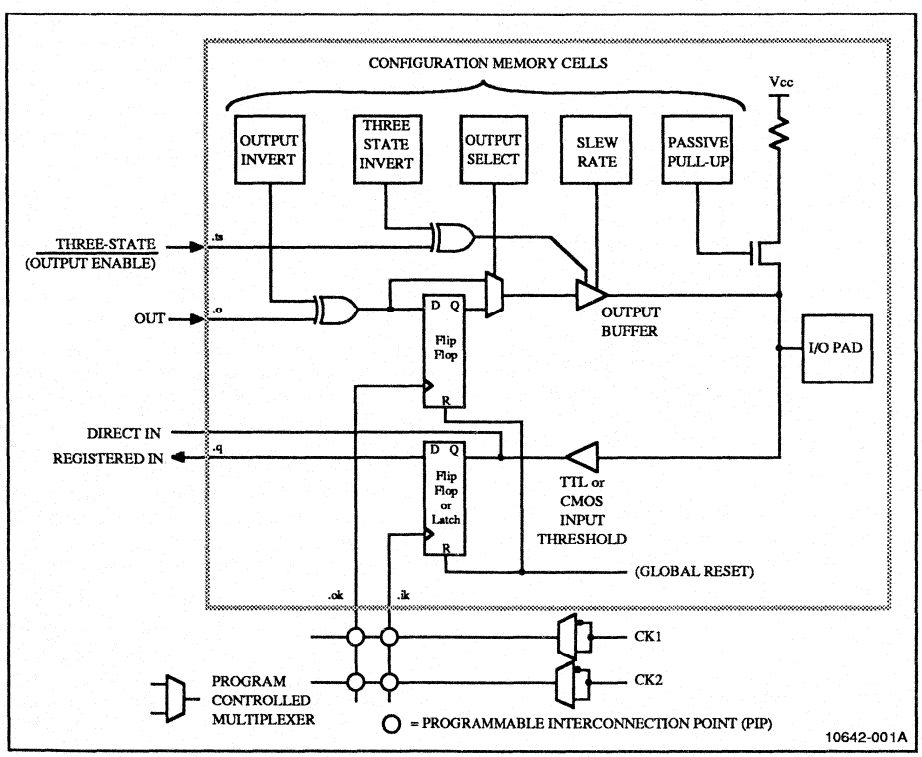


Figure 2. Input/Output Block

Flip-flop loop delays for the IOB and logic block flip-flops are about 3 ns. This increases reliability, especially for asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition, which can result from assertion of the clock during data transitions. Because of the short loop delay in LCA devices, the I/O flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without regard to their clock-relative timing, except as it applies to the internal logic and routing path delays.

Output buffers of the IOBs provide CMOS-compatible 4 mA source-or-sink drive for high fan-out CMOS or TTL compatible signal levels. The network driving IOB pin .o becomes the registered or direct data source for the output buffer. The three-state control signal, IOB pin .ts, can control output activity. An open-drain type output can be obtained by using the same signal for driving the output and three-state signal nets, so that the buffer output is enabled only for a LOW.

The configuration memory cells, shown in Figure 2, control the optional output register and logical signal inversion, as well as the three-state and slew rate configuration bits. A choice of two clocks is available on each die edge. All user inputs are programmed for TTL or CMOS thresholds.

The IOB includes input and output storage elements and the following I/O options selected by configuration memory cells.

- Logical **inversion of the output** is controlled by one configuration bit per IOB.
- Logical **three-state control** of each IOB output buffer is determined by the states of the configuration data bits that turn the buffer on/off or select the output buffer three-state control interconnection, IOB pin .ts. When this IOB output control signal is HIGH, or logic 1, the buffer is disabled and the package pin is high impedance. Inversion of the buffer three-state control logic sense, output enable, is controlled by an additional configuration data bit.
- **Direct or registered output** is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source, IOB pin .ok, can be supplied by either of two metal lines, which are available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased **output transition speed** can be selected to satisfy critical nets. Slower transitions reduce capacitive load peak currents of non-critical outputs and minimize system noise.
- A high impedance **pull-up resistor** can be used to prevent floating, unused inputs.

The table below summarizes the I/O options.

INPUTS	OUTPUTS
Direct	Direct/registered
Flip-flop/latch	Inverted/true
CMOS/TTL threshold (chip inputs)	Full speed/slew limited
Optional pull-up resistor	Optional three-state control

Configurable Logic Blocks

CLBs are the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The Am3020 has 64 such blocks arranged in eight rows and eight columns. The PGA Development System compiles the configuration data, which defines the operation and interconnection of each block. Users can define CLBs and their interconnecting networks by automatic translation from a schematic capture logic diagram or, optionally, by installing library or user macros.

Each CLB has a combinational logic section, two flip-flops, and an internal control section. As shown in the following figure, there are five logic inputs (.a, .b, .c, .d, and .e), a common clock input (.k), an asynchronous direct reset input (.rd), and a clock enable (.ec). All can be driven from the interconnection resources adjacent to the blocks. Each CLB also has two outputs (.x and .y) that can drive interconnection networks.

Data input for either flip-flop within a CLB is supplied from the F or G function outputs of the combinational logic, or the direct data input, .di. Both flip-flops in each CLB share the asynchronous reset, .rd, which, when enabled and HIGH, is dominant over clocked inputs. All flip-flops are reset by the active-LOW chip input, $\overline{\text{RESET}}$, or during the configuration process. The flip-flops share the clock enable (.ec), which, when LOW, recirculates the present states of the flip-flops and inhibits response to the data-in or combinational function inputs on a CLB. The user can enable these control inputs and select their sources. The user also can select the clock net input (.k) and its active sense in each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

The combinational logic portion of the CLB uses a 32-by-1 look-up table to perform Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinational propagation delay through the network is independent of the logic function generated and is spike free for changes in single input variables.

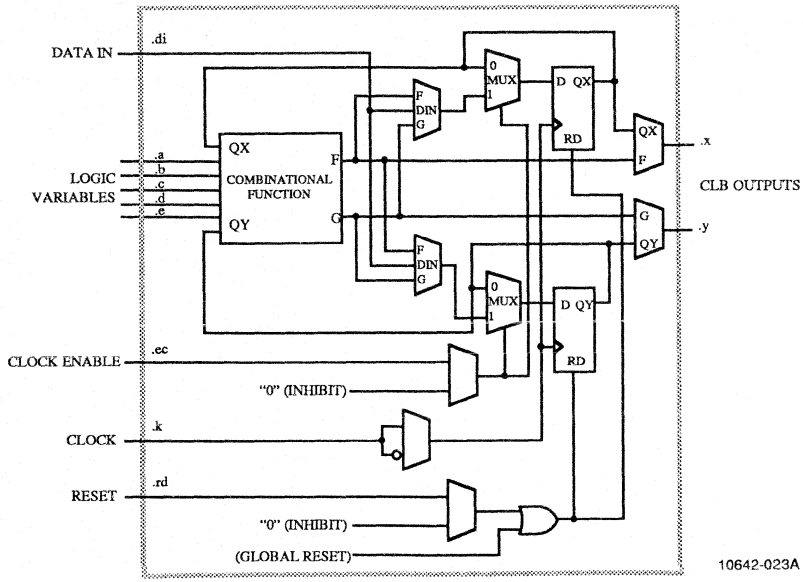


Figure 3. Configurable Logic Block

This technique can generate a single function of five variables, as shown below.

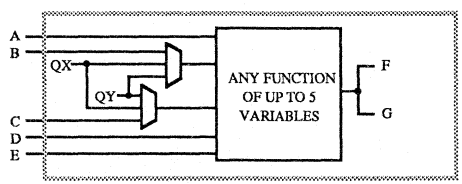


Figure 4. Combinatorial Logic Option 1

It can also generate any two logic functions of up to four variables each.

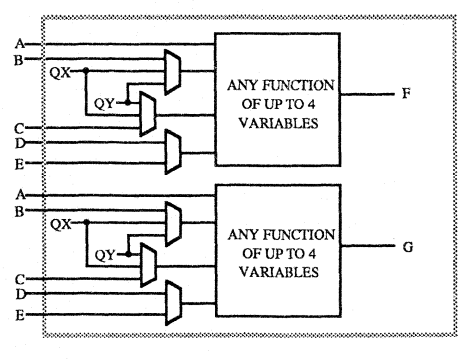


Figure 5. Combinatorial Logic Option 2

It can also generate some functions of seven variables, as shown in the next figure.

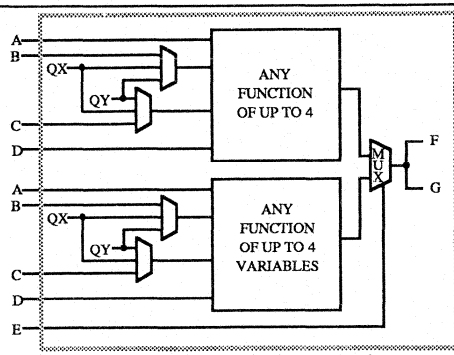


Figure 6. Combinatorial Logic Option 3

The partial functions of six or seven variables are generated by the input variable, .e, which dynamically selects between two functions of four different variables. For the two functions of four variables each, the independent results, F and G, can be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops helps optimize the routing of the networks connecting the logic blocks and IOBs.

The next figure shows a modulo 8 binary counter with parallel enable. It uses one CLB of each type.

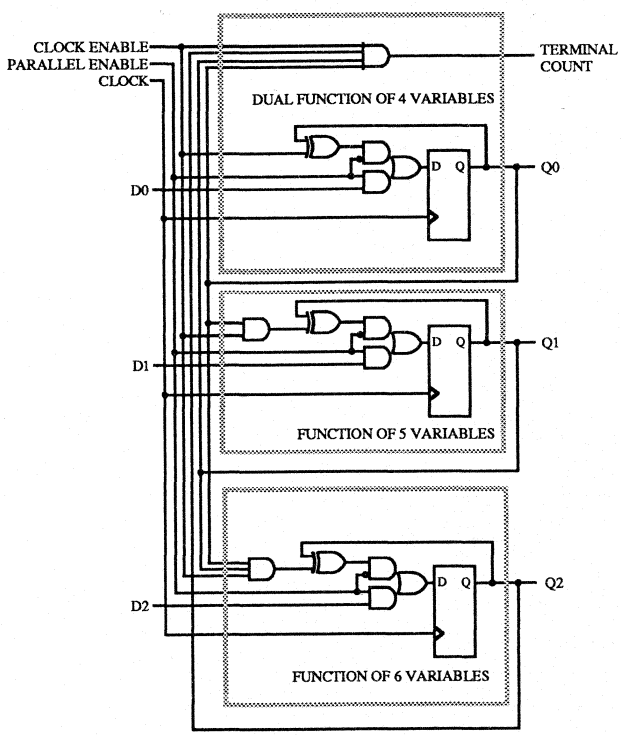


Figure 7. C8BCP Macro (modulo 8 binary counter with parallel enable and clock enable)

INTERCONNECTIONS

Programmable Interconnections

Programmable interconnection resources in the LCA device provide routing paths to connect inputs and outputs of the I/O and logic blocks into logical networks. Interconnections between blocks are composed of two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. The figure below provides an example of a routed net.

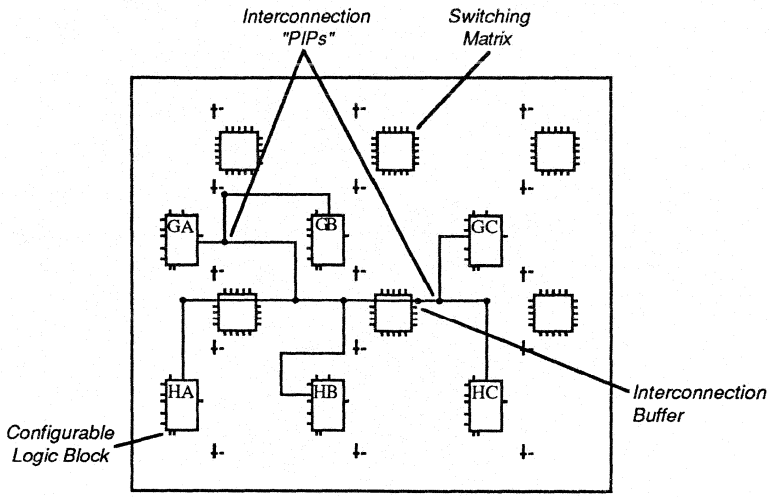


Figure 8. Routing Resources

The PGA Development System automatically routes these interconnections. Interactive routing can also be done to optimize the design. The inputs of the CLB or IOB are multiplexers that can be programmed to select an input network from the adjacent interconnection segments.

Note: The switch connections to block inputs are usable only for input connection, and not for routing, because they are unidirectional (as are block outputs).

The figure below illustrates routing access to logic block input variables, control inputs, and block outputs.

Three types of metal resources are available for network interconnections.

- General-Purpose Interconnection
- Direct Connection
- Long Lines

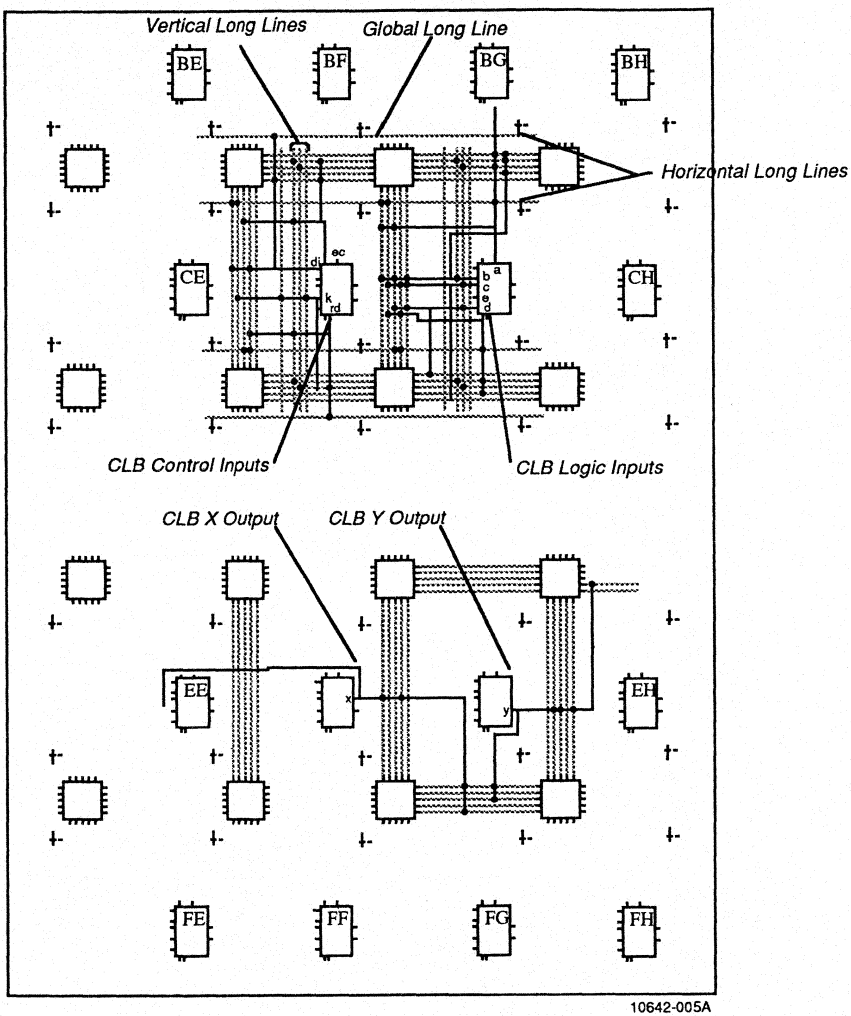


Figure 9. Routing Access to Inputs, Outputs

General-Purpose Interconnections

A general-purpose interconnection, as shown below, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of CLBs and IOBs. These segments can be connected through switch matrices to form networks for CLB and IOB inputs and outputs.

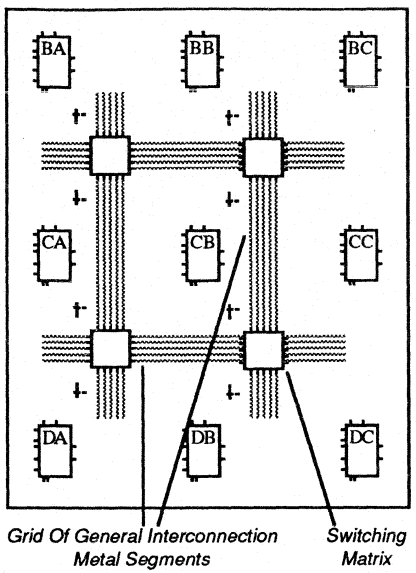


Figure 10. General Purpose Interconnections

Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix can be made by automatic routing, or by using Editnet to select the desired pairs of matrix pins that are to be connected or disconnected. The legitimate switching matrix combinations for each pin are shown in the next figure, and may be highlighted by the use of the SHOW MATRIX command.

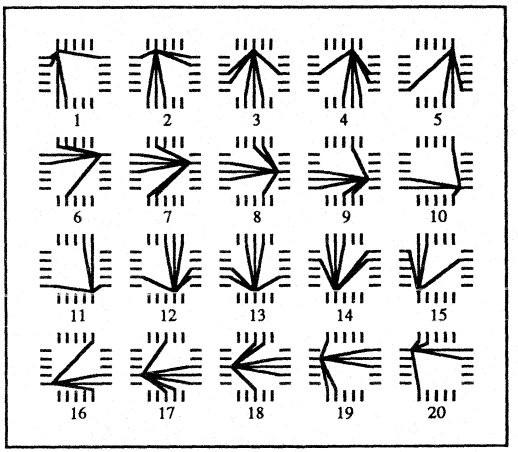


Figure 11. Switch Matrix Interconnection Options

Special buffers in the general interconnection areas are inserted automatically to provide periodic signal isolation and restoration, thus improving performance of lengthy nets. The interconnection buffers can propagate signals in either direction on a general interconnection segment. These bidirectional buffers are above and to the right of the switching matrices, and can be highlighted by the use of the SHOW MATRIX command. The other PIPs adjacent to the matrices are gateways to and from long lines.

The PGA Development System automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the PGA Development System automatically calculates and displays the block, interconnection, and buffer delays for the selected paths. It can also generate the simulation net list with a worst-case delay model.

4

Direct Interconnections

A direct interconnection, shown below, provides the most efficient implementation of networks between adjacent CLBs or IOBs. The .x and .y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs.

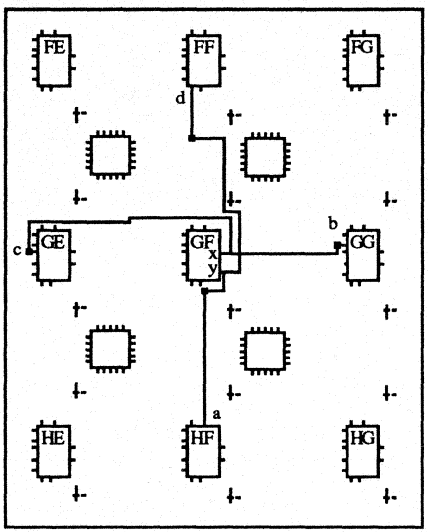


Figure 12. Direct Interconnection

Signals routed from block to block by direct interconnection show minimum interconnection propagation and use no general interconnection resources. For each CLB, the .x output can be connected directly to the .b input of the CLB to its right, and to the .c input of the CLB to its left. The .y output can use a direct interconnection to drive the .d input of the block above, and the .a input of the block below.

Direct interconnection should be used to maximize the speed of high performance portions of logic. Where CLBs are adjacent to IOBs, a direct connection is provided alternately to the IOB inputs (.i) and outputs (.o) on all four edges of the die. The right edge provides additional connections from CLB outputs to adjacent IOBs. Direct interconnections of IOBs and CLBs are shown in the next figure.

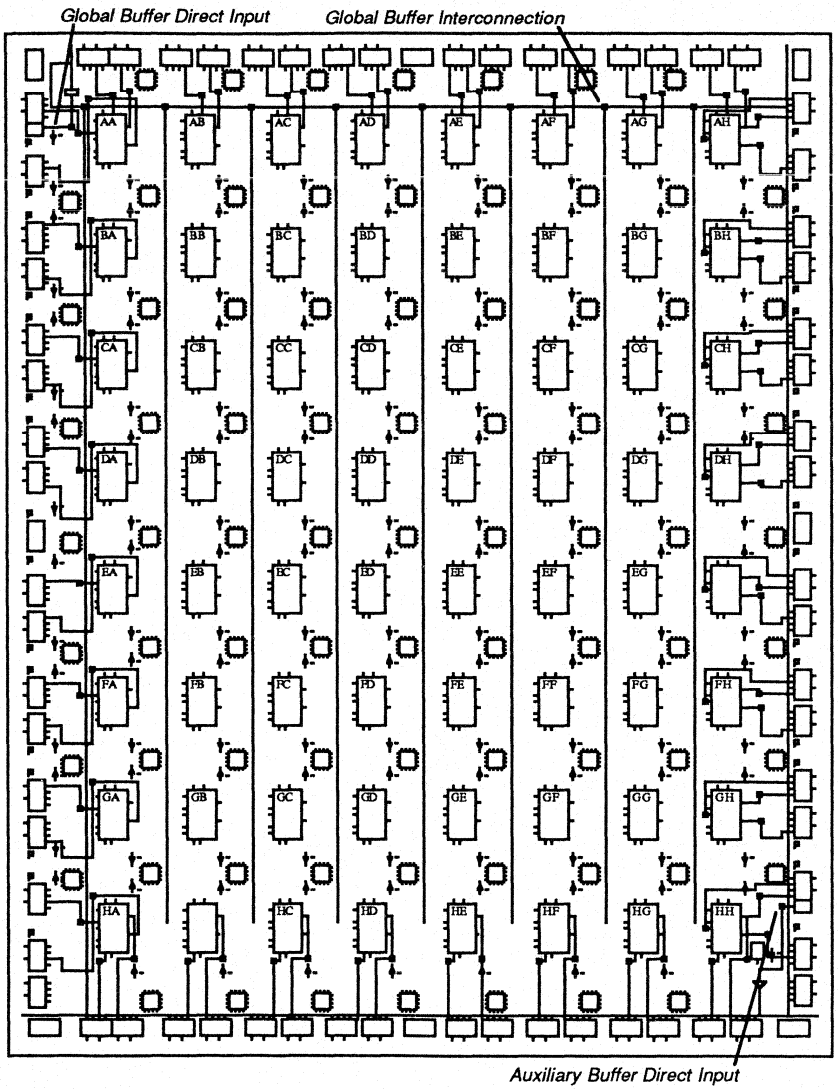


Figure 13. IOB and CLB Direct Interconnections

Long Lines

Long lines, which bypass the switch matrices, are intended primarily for signals that must travel a long distance, or that must have minimum skew among multiple destinations. Long lines, shown below, run the height or width of the interconnection area. Each interconnection column has three vertical long lines, and each interconnection row has two horizontal long lines. Two additional long lines are adjacent to the outer sets of switching matrices. On the Am3020, the outermost long lines are connectable half-length lines. In all other devices, the vertical long lines in each column are also connectable half-length.

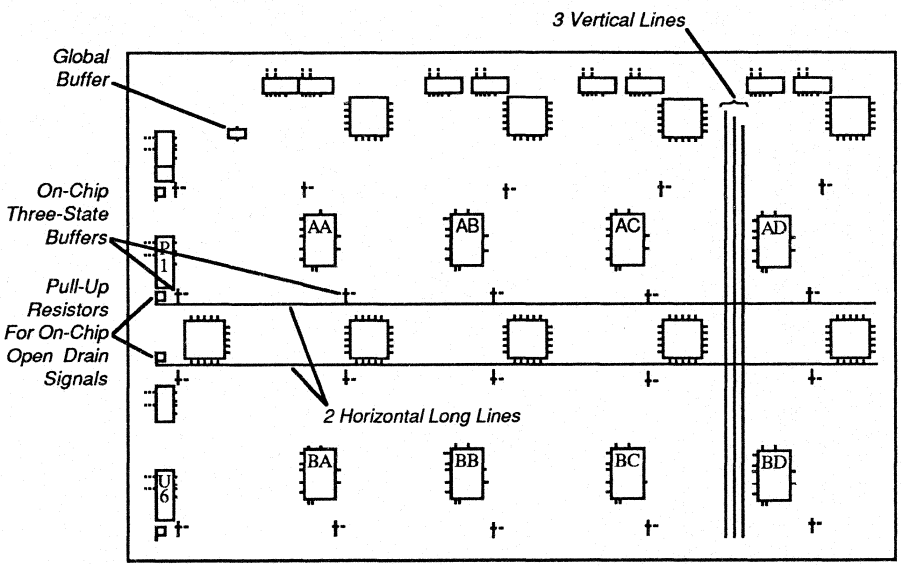


Figure 14. Long Lines

Horizontal and vertical long lines provide high fan-out, low-skew signal distribution in each row and column. The programmable interconnection of long lines is provided at the edges of the routing area. Long lines can be driven by a CLB or IOB output on a column-by-column basis. This provides a common low skew control or clock line within each column of logic blocks. Interconnections of these long lines are shown in the following figure. Isolation buffers are provided at each input to a long line and are enabled automatically by the PGA Development System when a connection is made.

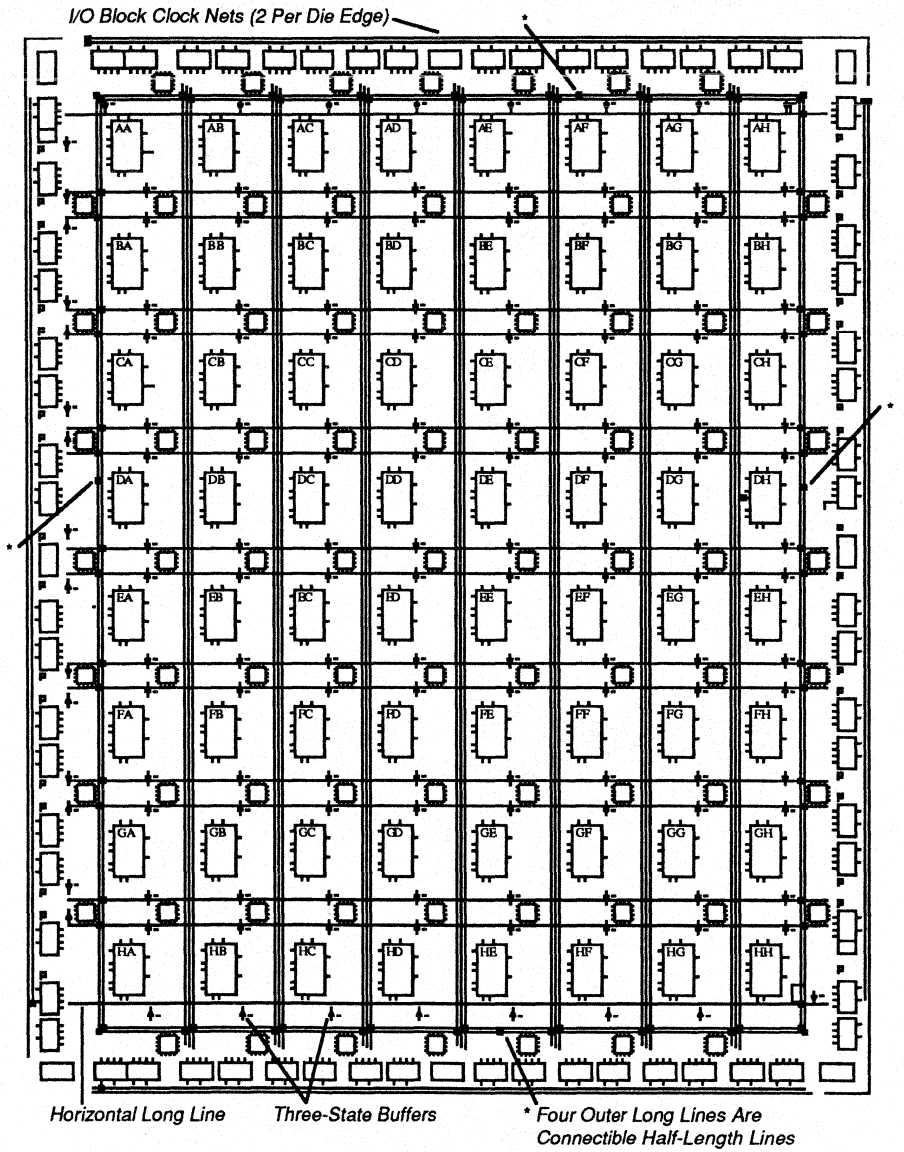


Figure 15. Interconnection of Long Lines

A buffer in the upper left corner of the LCA chip drives a global net available to all .k inputs of logic blocks. Using this global buffer for a clock signal provides a skew free, high fan-out, synchronized clock for use at any, or all, of the I/O and logic blocks. Configuration bits for the .k input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net can also be programmed to drive the die edge clock lines for IOB use. TCLKIN is an enhanced speed, CMOS threshold, direct access to this buffer that is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal long line, which can drive programmed connections to a vertical long line in each interconnection column. This alternate buffer also is low skew and high fan-out. The network formed by this alternate buffer's long lines can be selected to drive the .k inputs of the logic blocks. The CMOS threshold, high-speed access to this buffer, BCLKIN, is at the third pad from the bottom of the right die edge.

Internal Busses

A pair of three-state buffers are located adjacent to each CLB. These let logic drive the horizontal long lines. Any three-state buffer input can be selected to drive the horizontal long line bus by applying a low logic level on its three-state control line. Logical operation of the three-state buffer controls lets them implement wide multiplexing functions. When data drives the inputs, and separate signals drive the three-state control lines, these buffers form multiplexers (three-state buses), as shown below. In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line.

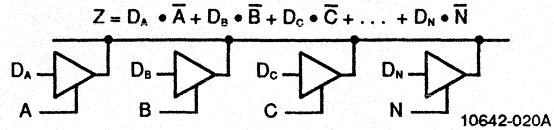


Figure 16. Three-State Buffers Implement a Multiplexer

Control of the three-state input by the same signal that drives the buffer input creates an open drain wired-AND function, as shown below. A logical HIGH on both buffer inputs creates a high impedance with no contention. A logical LOW enables the buffer to drive the long line low. Pull-up resistors are available at each end of the long line to provide a HIGH output when all connected buffers are non-conducting.

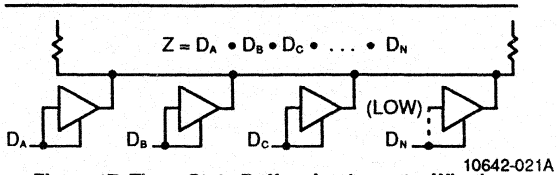


Figure 17. Three-State Buffers Implement a Wired – AND Function

These buffers allow fast, wide gating, optimum speed, and efficient routing of high fan-out signals. The following figure shows three-state buffers, long lines, and pull-up resistors.

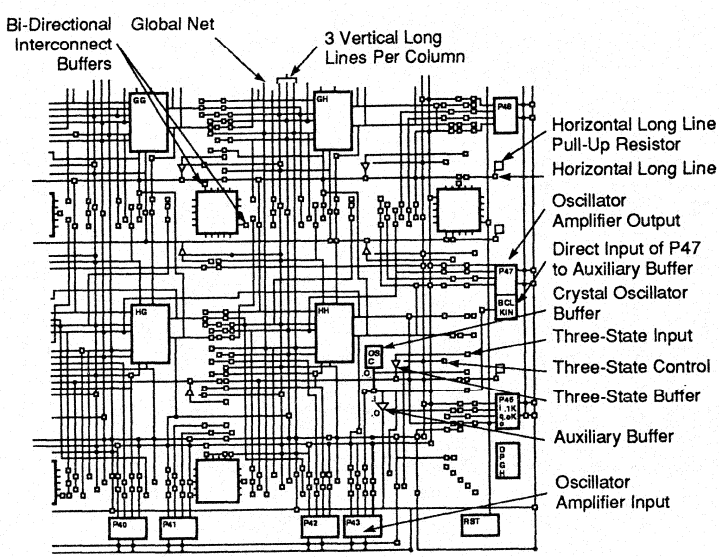


Figure 18. Possible Interconnections in the Lower Right Corner of the Am3020

Preliminary

Am1736/Am1765

Serial Configuration PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- One-time programmable 36,288 or 65, 536 x 1-bit serial memories designed to store configuration patterns for Logic Cell™ Arrays.
- Simple interface to the AMD LCA™ requires only one user I/O pin on the LCA.
- A single Am1736 supports all members of the Am2000 family and members of the Am3000 family as large as Am3042. The Am1765 supports all Am2000 and Am3000 family members. Both Serial Configuration PROMs support multiple patterns for daisy-chained configurations.
- Low power CMOS EPROM process.
- Cascadable to provide more memory for additional configurations or high-density arrays.
- Storage for multiple configurations for a single Logic Cell Array.
- Space-efficient, 8-pin ceramic DIP package
- Programming supported by leading programmer manufacturers.

GENERAL DESCRIPTION

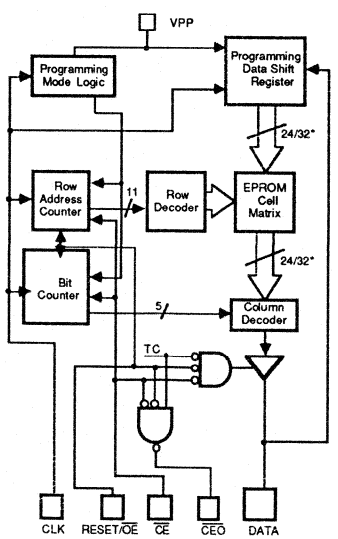
The Am1736 and Am1765 Serial Configuration PROMs (SCP) provide easy-to-use, cost-effective configuration memories for the AMD family of programmable gate arrays Packaged in an economical 8-pin DIP package, the devices use a simple serial access procedure to configure one or more Logic Cell Arrays (LCA). The 36,288 x 1-bit organization of the Am1736 supplies enough to configure any of the following devices: Am2064, Am2018, Am3020, and Am3042. The Am1765, with its 65,536 x 1-bits, in addition to the parts listed above, also supports the Am3040, Am3064 and Am3090 devices.

Multiple configurations for a single LCA device can be loaded from either SCP. Multiple SCPs can also be cascaded to provide larger memory for more configurations.

The Am1736/65 can be programmed on programming machines supplied by leading manufacturers, including Am081 from AMD. The LCA design file is first compiled into a standard HEX format with the PC-based Design System (AmPGA021). It can be transferred to the programmer through a serial port.

4

BLOCK DIAGRAM

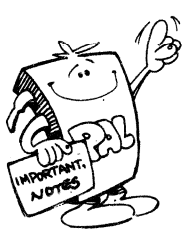


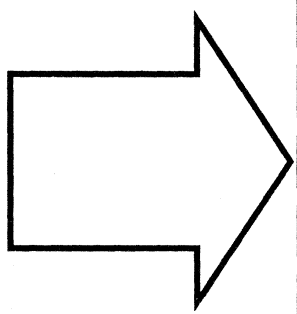
*24-bit word for Am1736
32-bit word for Am1765

10867-001A

Logic Cell Array and LCA are trademarks of Xilinx Corporation.

Publication # 10867 Rev. B Amendment /0
Issue Date: August 1989


IMPORTANT
NOTES



General Information

Military PAL Devices

Advanced Micro Devices' Military Programmable Array Logic (PAL) devices provide state machine and combinatorial logic solutions processed to military criteria. We offer the largest number of Standard Military Drawing PAL products in the industry.

Applications for our configurable PAL architectures include counters, shift registers, accumulators, control sequence generators, decoders, multiplexers, adders, memory mapped I/O and much more. These designs go into radar systems, missile guidance, avionics, airport graphic terminals, parallel processors, military computer hardware, and product obsolescence solutions, just to name a few.

Military PAL devices go where you need:

High Speed	A Series	B Series	D Series	-12 Series
	30 ns	20 ns	15 ns	12.5 ns
Power Savings		Half Power		Quarter Power
		90 mA		50 mA

Military PAL® Device/ Sequencer/FPGA Menu

STANDARD PAL DEVICES

FAMILY	PART NUMBER	PACKAGE	TECHNOLOGY	INPUTS	I/O	OUTPUTS	PRODUCT TERMS/OUTPUT	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
16R8	PAL16L8-12 PAL16R8-12 PAL16R6-12 PAL16R4-12	/BRA, /B2A	TTL	10 8 8 8	6 Comb – 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	12.5	43.4	180
	PAL16L8D PAL16R8D PAL16R6D PAL16R4D	20L,J,W	TTL					15	37	180
	PAL16L8B PAL16R8B PAL16R6B PAL16R4B	20L,J,W	TTL					20	28.5	180

Continued on next page.

PACKAGE DESIGNATORS					
MMI Devices	AMD Devices	Package	MMI Devices	AMD Devices	Package
J	BRA/BJA	Ceramic DIP	L	B2A/B3A	Leadless Chip Carrier
JS	BLA/BXA	Ceramic SKINNYDIP	–	G/BZA	Pin Grid Array
			W	BSA/BKA	Ceramic Flatpack

"MMI" devices are those produced by Monolithic Memories, Inc. before the companies merged.

STANDARD PAL DEVICES (continued)

FAMILY	PART NUMBER	PACKAGE	TECHNOLOGY	INPUTS	I/O	OUTPUTS	PRODUCT TERMS/OUTPUT	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
16R8 (cont'd)	PAL16L8B-2 PAL16R8B-2 PAL16R6B-2 PAL16R4B-2	20L,J,W	TTL	10 8 8 8	6 Comb – 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	30	20	90
	PAL16L8A PAL16R8A PAL16R6A PAL16R4A	20L,J,W	TTL					30	20	180
	PAL16L8B-4 PAL16R8B-4 PAL16R6B-4 PAL16R4B-4	20L,J,W	TTL					50	13.3	55
	PAL16L8A-2 PAL16R8A-2 PAL16R6A-2 PAL16R4A-2	20L,J,W	TTL					50	13.3	90
20R8	PAL20L8-12 PAL20R8-12 PAL20R6-12 PAL20R4-12	/BLA, /B3A	TTL	14 12 12 12	6 Comb – 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	12.5	43.4	210
	PAL20L8-15 PAL20R8-15 PAL20R6-15 PAL20R4-15	/BLA, /B3A	TTL					15	35.7	210
	PAL20L8B PAL20R8B PAL20R6B PAL20R4B	24JS,W, 28L	TTL					20	28.5	210
	PAL20L8A PAL20R8A PAL20R6A PAL20R4A	24JS,W, 28L	TTL					30	20	210
	PAL20L8A-2 PAL20R8A-2 PAL20R6A-2 PAL20R4A-2	24JS,W, 28L	TTL					50	13.3	105
20X10/ 20L10	PAL20L10A PAL20X10A PAL20X8A PAL20X4A	24JS,W, 28L	TTL	10 10 10 10	10 Comb – 2 Comb 6 Comb	– 10 RegXOR 8 RegXOR 4 RegXOR	3 4 3,4 3,4	35	15.4	165 180 180 180

UNIVERSAL PAL DEVICES

FAMILY	PART NUMBER	PACKAGE	TECHNOLOGY	INPUTS	I/O	PRODUCT TERMS/OUTPUT	FEATURES	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
22V10	PAL22V10-15 PAL22V10-20 AmPAL22V10A AmPAL22V10	/BLA,/B3A, /BKA	TTL	12	10 Macro	8-16	Varied Term Distribution	15 20 30 40	50 31.2 22 16.5	200 200 180 180
	PALCE22V10H-25 PALCE22V10H-30		EE CMOS					25 30	25 25	90 90
20V8	PALCE20V8H-20 PALCE20V8H-25	/BLA,/B3A	EE CMOS	12	8 Macro	8	GAL® device equivalent	20 25	33.3 28.6	90 90
16V8	PALCE16V8H-20 PALCE16V8H-25	/BRA,/B2A	EE CMOS	8	8 Macro	8	GAL device equivalent	20 25	33.3 28.6	90 90

ASYNCHRONOUS PAL DEVICES

FAMILY	PART NUMBER	PACKAGE	TECHNOLOGY	INPUTS	MACROCELLS	PRODUCT TERMS/OUTPUT	CLOCK	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
20RA10	PAL20RA10	24JS,W,28L	TTL	10	10	4	Programmable	35	16.7	200

MEMORY/INSTRUCTION-BASED SEQUENCERS

FAMILY	PART NUMBER	PACKAGE	TECHNOLOGY	INPUTS	OUTPUTS	ARRAY SIZE	FEATURES	f_{MAX} MHz	I_{CC} mA
Field-Programmable Controllers	Am29CPL151H-25 Am29CPL154H-25	/BXA,/B3A	UV CMOS	8 7	16 Reg	64 x 32 512 x 36	Instruction-based with Counter and Stack	25 25	130 140

FIELD-PROGRAMMABLE GATE ARRAYS

FAMILY	PART NUMBER	PACKAGE	TECHNOLOGY	I/O BLOCKS	CONFIGURABLE LOGIC BLOCKS	FLIP-FLOPS	EQUIVALENT GATES	f_{MAX} MHz	I_{CC} mA
Logic Cell™ Array 2000 Series	Am2018-70 Am2018-50 Am2018-33	/BTC	CMOS RAM	74	100	174	1800	70 50 33	15
	Am2064-70 Am2064-50 Am2064-33	/BZC	CMOS RAM	58	64	122	1200	70 50 33	10
Logic Cell Array 3000 Series	Am3020-70 Am3020-50	/BZC	CMOS RAM	64	64	256	2000	70 50	TBD
	Am3030-70 Am3030-50	/BZC	CMOS RAM	80	100	360	3000	70 50	TBD
	Am3042-70 Am3042-50	/BZC	CMOS RAM	96	144	480	4200	70 50	TBD
	Am3064-70 Am3064-50	/BZC	CMOS RAM	120	224	668	6400	70 50	TBD
	Am3090-70 Am3090-50	/BZC	CMOS RAM	144	320	928	9000	70 50	TBD

JAN 38510 and Standard Military Drawing Program

AMD is an active participant in the JAN 38510 and Standard Military Drawing (SMD) Program. The idea behind the SMD Program is to standardize MIL-STD-883, Class B microcircuits where fully qualified JAN product is not available. The advantage to the user is that SMDs are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Standard Military Drawings should always be considered to improve availability over source control drawings. It is standard practice at AMD to convert our 883, Class B processing to SMDs for all products which we are approved to supply. AMD then dual marks these devices with both the SMD number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and Distributor channels.

The following cross reference will allow you to determine the appropriate SMD and JAN Drawing for each PAL device. AMD will continue to work closely with DESC, generating new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

MIL-M-38510 Slash Sheet Cross Reference for AMD Generic Part Number

M38510	01	02	03	04	05	06	07	08	09	10
503	10H8	12H6	14H4			10L8	12L6	14L4		
504	16L8A	16R8A	16R6A	16R4A			16L8A-2	16R8A-2	16R8A-2	16R4A-2
505	20L8A	20R8A	20R6A	20R4A						

Military SMDs

MILITARY DRAWING	AMD PART NUMBER	MILITARY DRAWING	AMD PART NUMBER
8103501RA	PAL10H8MJ/883B	84129033A	PAL20R6AML/883B
81035012A	PAL10H8ML/883B	8412903KA	PAL20R6AMW/883B
8103501SA	PAL10H8MW/883B	8412904LA	PAL20R4AMJS/883B
8103502RA	PAL12H6MJ/883B	84129043A	PAL20R4AML/883B
81035022A	PAL12H6ML/883B	8412904KA	PAL20R4AMW/883B
8103502SA	PAL12H6MW/883B	8412905LA	PAL20L10AMJS/883B
8103503RA	PAL14H4MJ/883B	84129053A	PAL20L10AML/883B
81035032A	PAL14H4ML/883B	8412905KA	PAL20L10AMW/883B
8103503SA	PAL14H4MW/883B	8412906LA	PAL20X8AMJS/883B
8103504RA	PAL16H2MJ/883B	84129063A	PAL20X8AML/883B
81035042A	PAL16H2ML/883B	8412906KA	PAL20X8AMW/883B
8103504SA	PAL16H2MW/883B	8412907LA	PAL20X10AMJS/883B
8103505RA	PAL16C1MJ/883B	84129073A	PAL20X10AML/883B
81035052A	PAL16C1ML/883B	8412907KA	PAL20X10AMW/883B
8103505SA	PAL16C1MW/883B	8412908LA	PAL20X4AMJS/883B
8103506RA	PAL10L8MJ/883B	84129083A	PAL20X4AML/883B
81035062A	PAL10L8ML/883B	8412908KA	PAL20X4AMW/883B
8103506SA	PAL10L8MW/883B	8412909LA	PAL20L8A-2MJS/883B
8103507RA	PAL12L6MJ/883B	84129093A	PAL20L8A-2ML/883B
81035072A	PAL12L6ML/883B	8412909KA	PAL20L8A-2MW/883B
8103507SA	PAL12L6MW/883B	8412910LA	PAL20R8A-2MJS/883B
8103508RA	PAL14L4MJ/883B	84129103A	PAL20R8A-2ML/883B
81035082A	PAL14L4ML/883B	8412910KA	PAL20R8A-2MW/883B
8103508SA	PAL14L4MW/883B	8412911LA	PAL20R6A-2MJS/883B
8103509RA	PAL16L2MJ/883B	84129113A	PAL20R6A-2ML/883B
81035092A	PAL16L2ML/883B	8412911KA	PAL20R6A-2MW/883B
8103509SA	PAL16L2MW/883B	8412912LA	PAL20R4A-2MJS/883B
8103607RA	PAL16L8AMJ/883B	84129123A	PAL20R4A-2ML/883B
81036072A	PAL16L8AML/883B	8412912KA	PAL20R4A-2MW/883B
8103607SA	PAL16L8AMW/883B	8506501RA	PAL16L8A-4MJ/883B
8103608RA	PAL16R8AMJ/883B	85065012A	PAL16L8A-4ML/883B
81036082A	PAL16R8AML/883B	8506501SA	PAL16L8A-4MW/883B
8103608SA	PAL16R8AMW/883B	8506502RA	PAL16R8A-4MJ/883B
8103609RA	PAL16R6AMJ/883B	85065022A	PAL16R8A-4ML/883B
81036092A	PAL16R6AML/883B	8506502SA	PAL16R8A-4MW/883B
8103609SA	PAL16R6AMW/883B	8506503RA	PAL16R6A-4MJ/883B
8103610RA	PAL16R4AMJ/883B	85065032A	PAL16R6A-4ML/883B
81036102A	PAL16R4AML/883B	8506503SA	PAL16R6A-4MW/883B
8103610SA	PAL16R4AMW/883B	8506504RA	PAL16R4A-4MJ/883B
8103612RA	PAL16R8A-2MJ/883B	85065042A	PAL16R4A-4ML/883B
81036122A	PAL16R8A-2ML/883B	8506504SA	PAL16R4A-4MW/883B
8103612SA	PAL16R8A-2MW/883B	5962-8515501RA	PAL16L8BMJ/883B
8103613RA	PAL16R6A-2MJ/883B	5962-85155012A	PAL16L8BML/883B
81036132A	PAL16R6A-2ML/883B	5962-8515501SA	PAL16L8BMW/883B
8103613SA	PAL16R6A-2MW/883B	5962-8515502RA	PAL16R8BMJ/883B
8103614RA	PAL16R4A-2MJ/883B	5962-85155022A	PAL16R8BML/883B
81036142A	PAL16R4A-2ML/883B	5962-8515502SA	PAL16R8BMW/883B
8103614SA	PAL16R4A-2MW/883B	5962-8515503RA	PAL16R6BMJ/883B
8412901LA	PAL20L8AMJS/883B	5962-85155032A	PAL16R6BML/883B
84129013A	PAL20L8AML/883B	5962-8515503SA	PAL16R6BMW/883B
8412901KA	PAL20L8AMW/883B	5962-8515504RA	PAL16R4BMJ/883B
8412902LA	PAL20R8AMJS/883B	5962-85155042A	PAL16R4BML/883B
84129023A	PAL20R8AML/883B	5962-8515504SA	PAL16R4BMW/883B
8412902KA	PAL20R8AMW/883B	5962-8515505RA	PAL16L8B-2MJ/883B
8412903LA	PAL20R6AMJS/883B	5962-85155052A	PAL16L8B-2ML/883B

Military SMDs (Cont'd)

MILITARY DRAWING	AMD PART NUMBER	MILITARY DRAWING	AMD PART NUMBER
5962-8515505SA	PAL16L8B-2MW/883B	5962-8680405KA	PAL20L2MW/883B
5962-8515506RA	PAL16R8B-2MJ/883B	5962-8680406LA	PAL20C1MJS/883B
5962-85155062A	PAL16R8B-2ML/883B	5962-86804063A	PAL20C1ML/883B
5962-8515506SA	PAL16R8B-2MW/883B	5962-8680406KA	PAL20C1MW/883B
5962-8515507RA	PAL16R6B-2MJ/883B	5962-8753001LA	PAL20S10MJS/883B
5962-85155072A	PAL16R6B-2ML/883B	5962-87530013A	PAL20S10ML/883B
5962-8515507SA	PAL16R6B-2MW/883B	5962-8753001KA	PAL20S10MW/883B
5962-8515508RA	PAL16R4B-2MJ/883B	5962-8753002LA	PAL20RS10MJS/883B
5962-85155082A	PAL16R4B-2ML/883B	5962-87530023A	PAL20RS10ML/883B
5962-8515508SA	PAL16R4B-2MW/883B	5962-8753002KA	PAL20RS10MW/883B
5962-8515509RA	PAL16L8DMJ/883B	5962-8753003LA	PAL20RS8MJS/883B
5962-85155092A	PAL16L8DML/883B	5962-87530033A	PAL20RS8ML/883B
5962-8515509SA	PAL16L8DMW/883B	5962-8753003KA	PAL20RS8MW/883B
5962-8515510RA	PAL16R8DMJ/883B	5962-8753004LA	PAL20RS4MJS/883B
5962-85155102A	PAL16R8DML/883B	5962-87530043A	PAL20RS4ML/883B
5962-8515510SA	PAL16R8DMW/883B	5962-8753004KA	PAL20RS4MW/883B
5962-8515511RA	PAL16R6DMJ/883B	5962-8753902LA	PALC22V10H-30MQS/883B
5962-85155112A	PAL16R6DML/883B	5962-8753903LA	PALC22V10H-40MQS/883B
5962-8515511SA	PAL16R6DMW/883B	5962-87671101LA	PAL20L8BMJS/883B
5962-8515512RA	PAL16R4DMJ/883B	5962-87671013A	PAL20L8BML/883B
5962-85155122A	PAL16R4DML/883B	5962-8767101KA	PAL20L8BMW/883B
5962-8515512SA	PAL16R4DMW/883B	5962-87671102LA	PAL20R8BMJS/883B
5962-8605301LA	AmPAL22V10A/BLA	5962-87671023A	PAL20R8BML/883B
5962-86053013A	AmPAL22V10A/B3A	5962-8767102KA	PAL20R8BMW/883B
5962-8605301KA	AmPAL22V10A/BKA	5962-8767103LA	PAL20R6BMJS/883B
5962-8605302LA	AmPAL22V10/BLA	5962-87671033A	PAL20R6BML/883B
5962-86053023A	AmPAL22V10/B3A	5962-8767103KA	PAL20R6BW/883B
5962-8605302KA	AmPAL22V10/BKA	5962-8767104LA	PAL20R4BMJS/883B
5962-8605304LX	PAL22V10-20/BLA	5962-87671043A	PAL20R4BML/883B
5962-86053043X	PAL22V10-20/B3A	5962-8767104KA	PAL20R4BMW/883B
5962-8605304KX	PAL22V10-20/BKA	5962-8851501RA	PAL16L8B-4MJ/883B
5962-8680301LA	PAL20RA10MJS/883B	5962-88515012A	PAL16L8B-4ML/883B
5962-86803013A	PAL20RA10ML/883B	5962-8851501SA	PAL16L8B-4MW/883B
5962-8680301KA	PAL20RA10MW/883B	5962-8851502RA	PAL16R8-4MJ/883B
5962-8680401LA	PAL18L4MJS/883B	5962-88515022A	PAL16R8B-4ML/883B
5962-86804013A	PAL18L4ML/883B	5962-8851502SA	PAL16R8B-4MW/883B
5962-8680401KA	PAL18L4MW/883	5962-8851503RA	PAL16R6B-4MJ/883B
5962-8680402LA	PAL12L10MJS/883B	5962-88515032A	PAL16R6B-4ML/883B
5962-86804023A	PAL12L10ML/883B	5962-8851503SA	PAL16R6B-4MW/883B
5962-8680402KA	PAL12L10MW/883B	5962-8851504RA	PAL16R4B-4MJ/883B
5962-8680403LA	PAL14L8MJS/883B	5962-88515042A	PAL16R4B-4ML/883B
5962-86804033A	PAL14L8ML/883B	5962-8851504SA	PAL16R4B-4MW/883B
5962-8680403KA	PAL14L8MW/883B	5962-8867002LA	PALC22V10H-30MJS/883B
5962-8680404LA	PAL16L6MJS/883B	5962-88670023A	PALC22V10H-30ML/883B
5962-86804043A	PAL16L6ML/883B	5962-8867002KA	PALC22V10H-30MW/883B
5962-8680404KA	PAL16L6MW/883B	5962-8837003LA	PALC22V10H-40MJS/883B
5962-8680405LA	PAL20L2MJS/883B	5962-88670033A	PALC22V10H-40ML/883B
5962-86804053A	PAL20L2ML/883B	5962-8867003KA	PALC22V10H-40MW/883B

Product Introduction Procedures

All new products released by the Military Products Division must successfully pass Mil-Std-883 Class B processing prior to new product announcement. This practice allows us to do checkout of bonding diagrams, electrical test tapes and burn circuits in a manufacturing environment. Programmability is checked when applicable. Our Military Engineering Department reviews electrical data to insure performance and yields to military data sheet limits are acceptable, prior to new product release. This procedure allows MPD to keep manufacturing start-up problems to a minimum on new product orders.

Standard Processing Flows

MPD Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows for the Military Products Division include:

MPD Modified Level S
JAN 38510 Class B
Standard Military Drawing Program
Mil-Std-883 Class B

In addition, these flows are expanded to provide for factory programming on PAL circuits, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost—no price adders for custom processing.
- Improved lead time—no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

For your reference, we have included our Modified Level S flow and our Mil-Std-883 Class B flow.

It is the policy of AMD, to always operate to the most current revision of Mil-M-38510 and Mil-Std-883.

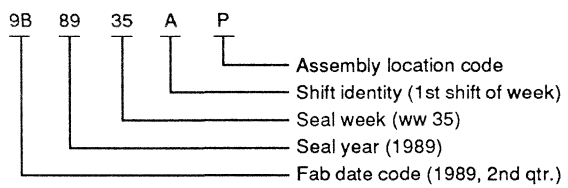
Manufacturing and Screening Locations

JAN Products, MPD Modified Level "S", and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified lines in Sunnyvale and Santa Clara, California.

MIL-STD-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by AMD Quality Department, as well as by many of our customers, to manufacture MIL-STD-883 Class B product. Conformance to MIL-STD-883 requirements is routinely monitored through audits at the Penang facility.

Assembly location as well as fabrication and seal date codes are included in AMD's part marking.

Example:



Assembly Location Codes:

Blank	Sunnyvale
M	Manila
P	Penang

5

STANDARD MILITARY FLOW CHART

Screening	Modified Level S	Requirement	Class B	Requirement
	(Per Customer SCD)		MIL-STD-883 Method 5004	
S.E.M.	2018	Sample		
Assembly	USA assembly		Typically offshore assembly	
Non-destruct bond pull	2023	100%		
Die shear/ Destruct bond pull	2019 (sample)	SS = 2 REJ = 0		
Internal visual	2010 cond. A (modified)	100%	2010 cond. B	100%
Temperature cycling	1010	100%	1010	100%
Constant acceleration	2001 test cond. D or E Y1 orientation only	100%	2001 test cond. D or E Y1 orientation only	100%
Particle impact noise detection (PIND)	2020 cond. A only	100%		
Interim electrical parameters	Per application device specification T_A = 25°C only	100%		
Serialization		100%		
X-Ray	2010 two views X and Y axis only	100%		
Interim electrical (1) parameter	Per applicable device specification T_A = 25°C only	100%	Per applicable device (1) specification T_A = 25°C only	100%
Burn In	1015 Cond. D T_A = +125°C (min) Time = 240 hrs	100%	1015 Cond. C or D	100%
Freeze Out	Option			
Post electrical parameters	Per applicable device specification T_A = 25°C only (delta's when required)	100%	Per applicable device specification T_A = 25°C only	100%
Delta calculations (when applicable)	Per applicable device specification			
Percent defect allowable	DC Parameters PDA = 5% or 1 device whichever is greater Functional Parameters PDA = 3% or 1 device whichever is greater		DC Parameters PDA = 5% or 1 device whichever is greater	

(1) Programming and verification are performed at 25°C only.

Standard Military Flow Chart (Cont'd.)

SCREENING	MODIFIED LEVEL S	REQUIREMENT	CLASS B	REQUIREMENT
	PER CUSTOMER SCD		MIL-STD-883 METHOD 5004	
Final electrical parameters (hot and cold extremes)	Per applicable device specification	100%	Per applicable device specification	100%
Seal A) Fine B) Gross	1014 cond, A or B cond C	100%	1014 cond, A or B cond C	100%
Group A lot	Level S	Per applicable device specification	5005 Class B	Sample every lot
Group B inspection lot Group C Group D External visual	Level S not applicable Level S 2009	As required As required 100%	5005 Class B 5005 Class B 5005 Class B 2009	Every lot Every 4 qtrs of fab date code Every 52 weeks 100%

(1) Programming and verification are performed at 25°C only.

Programming Inputs for ProPAL and HAL Devices

1. All patterns require customer approval. Order of preference:
   - Mag Tape* and one master
   - Floppy Disk* and one master
   - 2 masters and equation printout or truthtable

*2. The following is a list describing the different types of Mag Tapes and Floppy Disks that Software Support currently can accept:
   - Standard 8 Inch Floppy Disks formatted RX01/IBM0 (Single-Sided, Single Density) or RX02/IBM2 (Single-Sided, Double Density) or RX03/IBM3 (Double-Sided, Double Density).
   - IBM 5-1/4 Inch Floppy Disks formatted Single-Sided, Double Density or Double-Sided, Double Density

     or
   - Magnetic Tape (Created on VAX/VMS System): Mag Tapes must be in IBM compatible (800 or 1600 BPI) nine track in blocked, unlabeled (card image) format of Files-11 or VAX/VMS Backup format.

   - In all cases, the Tapes or Disks must contain a label indicating all data such as the density, the format, the operating system, the command used to write the files and/or to remove the data from the Tape or Disk, and a listing of the filenames.

DC/AC Parametric Testing

1. VIL/VIH Parametric Information

VIL/VIH parameters are, in effect, input conditions of DC tests and are not directly tested. Functional tests are performed at VIL = 0.4 V and VIH = 2.4 V. VIL is specified at ≤ 0.8 V, and VIH is specified at ≥ 2.0 V.

2. AC Testing/Programming

Advanced Micro Devices offers a large selection of programmable products. For those devices which must be programmed prior to AC Tests and are ordered unprogrammed, Advanced Micro Devices must perform an AC Sample to "guarantee" their AC Performance.

Since the guaranteeing of parameters can be a serious concern for the Military user, we have outlined several approaches to address the AC screening issue.

Option 1. Advanced Micro Devices can pull a Sample from a lot using our own Standard patterns (designed to blow in excess of 50 percent of the fuses) and perform AC testing at 25°C, 125°C, and -55°C.
   - PAL products processed to Military drawings include programmability samples and AC testing at 25°C, 125°C, and -55°C.

Option 2. Advanced Micro Devices can program PAL devices using custom patterns submitted by the customer. AC testing is performed as follows:

   - 100% AC at 25°C, –55°C and 125°C and on-line sample for Group A, Subgroups 9, 10, and 11.

On PAL products where custom programming is performed and AC testing is required, additional vector generation and fault coverage analysis is required, as well as AC program generation and checkout. This will result in additional upfront lead time.

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"
Mil-Q-9858, "Quality Program Requirements"
Mil-I-45208, "Inspection System Requirements"

AMD facilities in Sunnyvale and Santa Clara are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Bipolar PROMs and PAL circuits in accordance with MIL-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of MIL-M-38510.

Quality Assurance

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of MIL-STD-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 slash sheet sample plans and approved SMD sample plans.

Product Qualification/Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with MIL-STD-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that AMD, as a minimum, conduct qualification testing per Company Policy specification on Product Reliability Qualification (00-019). Once qualified, each package type (from each assembly line) and device (by technology group as delineated in MIL-M-38510) are incorporated into AMD Quality Conformance Inspection program which utilizes the requirements of MIL-STD-883.

When military programs do not require that QCI data be run on the specific lot shipped, AMD Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and destruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following product data is available:

Group B – Package Related Tests

- QCI is performed in line on each inspection lot.
- Purpose: To monitor assembly and device package integrity.

Group C – Product/Process Related Tests

- Group C is performed based on fab date code, at least every four quarters.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and the parametric performance for each product technology.

Group D – In-Depth Package Related Tests

- QCI is conducted every 52 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, (self audits) by the Quality Assurance Department.

Electrostatic Discharge Control Procedures

The Military Products Division of AMD fully employs static control procedures throughout its facilities.

All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

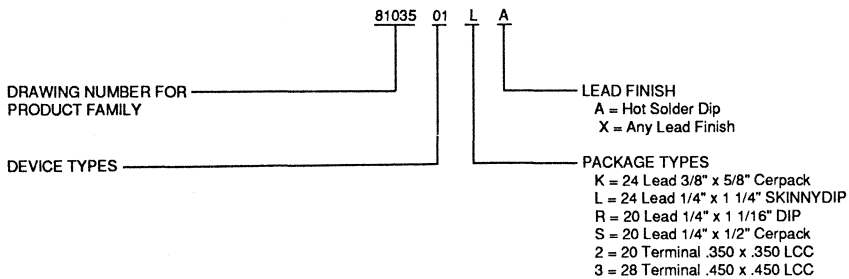
All product is moved throughout our facilities and shipped to customers in static shielded containers.

In addition, MPD distributors must demonstrate that they meet the same stringent standards regarding ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by MPD's Quality Assurance Department.

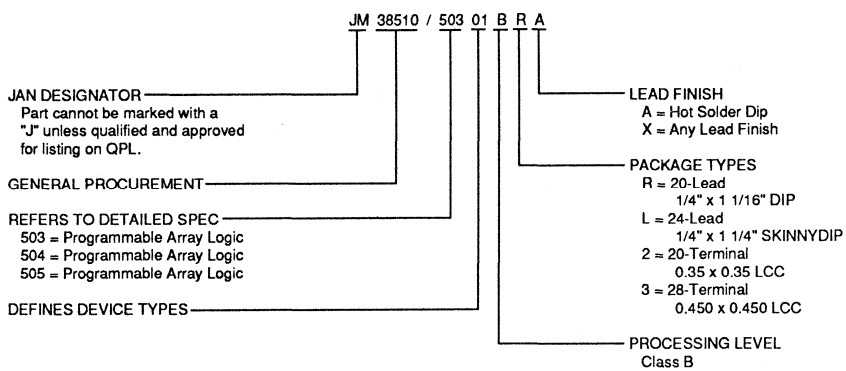
An ESD identifier is marked on all products per MIL-STD-883 1.2.1 b (30). All shipping containers are labeled with an ESD Caution Message. ESD procedures are continually reviewed, to ensure that our customers receive only the highest quality product from the Military Products Division.

JAN 38510 and STANDARD MILITARY DRAWING PROGRAM

STANDARD MILITARY DRAWING NUMBERING SYSTEM



JAN PART NUMBERING SYSTEM



PART NUMBER INTERPRETATION:

When ordering to JAN 38510 and Military Drawing numbers, the lead finish designator (last letter in part number) is commonly called out as "X". This is a way of stating that the customer will accept the standard manufacturer's lead finish for the package orders. "X" is not a lead finish designator in itself, therefore, when product is shipped, the actual lead finish designator will be marked on the devices.

Electrical Characteristic Definitions

	PARAMETER NAME	PARAMETER DEFINITION
TIMING		
t_{APR}	Asynchronous Preset Recovery Time	The minimum time after the asynchronous preset becomes inactive to the next input clock triggering edge.
t_{APW}	Asynchronous Preset Width	The minimum pulse width required for the asynchronous preset signal.
t_{H}	Hold Time	The minimum time a valid data level is held after clock triggering edge.
t_{HP}	Hold Time for Preload	The minimum delay time for data to remain stable after the preload signal becomes inactive. This only applies to TTL-level preload.
t_{SRR}	Synchronous Reset Recovery Time	The minimum time between the synchronous reset going inactive and the next input clock triggering edge.
t_{S}	Setup Time, Input or Feedback to Clock	The minimum time a valid data level of input or feedback is stable before the next clock triggering edge.
t_{SP}	Data Setup Time for Preload	The minimum time for input data to be stable prior to the preload signal becoming inactive.This only applies to TTL-level preload.
t_{WH}	Clock Width High	The minimum width of the clock high from rising edge to the next falling edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WL}	Clock Width Low	The minimum width of the clock low from falling edge to the next rising edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WP}	Preload Pulse Width	The minimum pulse width required to preload the registers. This only applies to TTL-level preload.
t_{AP}	Asynchronous Preset to Output	The maximum time required to preset the register output after the preset signal is asserted.
t_{AR}	Asynchronous Reset to Output	The maximum time required to reset the register output after the reset signal is asserted.
t_{CF}	Clock to Feedback	The maximum delay between the time the clock triggering edge is asserted and the signal appears on the feedback.
t_{CO}	Clock to Register Output (or Feedback)	The maximum time it takes to obtain a valid data level on the output pin after an input clock triggering edge is applied.
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration; Output Mux Select 1 to 0	The minimum time from input or feedback to registered output as output mux selection changes from combinatorial to registered output (1 to 0).
t_{EA}	Output Enable Time, Clock to Output	The minimum delay between when an input is asserted and the output switches from a high-impedance state to HIGH or LOW logic state.

Electrical Characteristic Definitions

	PARAMETER NAME	PARAMETER DEFINITION
t_{ER}	Output Disable Time, Input to Output	The minimum delay between when an input is asserted and the output switches from a HIGH or LOW logic state to a high-impedance state.
t_F	Fall Time	The minimum time for a signal to fall from 80% to 20% of its stabilized high value.
t_{PD}	Propagation Delay, Input or Feedback to Combinatorial Output	The time for a signal to propagate from input or feedback to output.
t_{PR}	Power-up Reset Time	The minimum time for a registered output signal to be reset after the power is applied.
t_{PXZ}	Output Disable Time, OE to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a HIGH or LOW logic state to a high-impedance state.
t_{PZX}	Output Enable Time, OE to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a high-impedance state to a HIGH or LOW logic state.
t_R	Rise Time	The minimum time for a signal to rise from 20% to 80% of its stabilized high value.
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration; Output Mux Select 0 to 1	The minimum time from input or feedback to combinatorial output as output mux selection changes from registered to combinatorial output (0 to 1)
VOLTAGE		
V_{CC}	Supply Voltage, Positive Potential	The voltage required across supply and ground terminals of a TTL or CMOS integrated circuit.
V_{EE}	Supply Voltage, Negative Potential	The voltage required across supply and ground terminals of an ECL integrated circuit.
V_I	Input Clamp Voltage	The maximum input clamp voltage limit on every input pin.
V_{IH}	High-Level Input Voltage	The minimum high-level input voltage that is guaranteed to represent a high logic level.
V_{IL}	Low-Level Input Voltage	The maximum low-level input voltage that is guaranteed to represent a low logic level.
V_{OH}	High-Level Output Voltage	The minimum high logic level guaranteed for all outputs.
V_{OL}	Low-Level Output Voltage	The maximum low logic level guaranteed for all outputs.

Electrical Characteristic Definitions

	PARAMETER NAME	PARAMETER DEFINITION
CURRENT		
I_{CC}	Supply Current, Corresponding to V_{CC}	The maximum current into the V_{CC} terminal of a TTL or CMOS integrated circuit.
I_{EE}	Supply Current, Corresponding to V_{EE}	The maximum current into the V_{EE} terminal of an ECL integrated circuit.
I_I	Input Current with Maximum Input Voltage	The maximum current into an input pin when the input voltage is applied to the input pin.
I_{IH}	High-Level Input Current	The maximum current into an input pin when a logic-high level is applied to the input pin.
I_{IL}	Low-Level Input Current	The maximum current into an input pin when a logic-low level is applied to the input pin.
I_{OH}	High-Level Output Current	The maximum current into an output pin to guarantee an output logic-high level.
I_{OL}	Low-Level Output Current	The maximum current into an output pin to guarantee an output logic-low level.
I_{SC}	Output Short-Circuit Current	The current into an output when that output is short-circuited to ground (0.5 V).
I_{OZH}	High-Level Leakage Current	The maximum current into a high-impedance state output pin when a high logic level is applied to the output pin.
I_{OZL}	Low-Level Leakage Current	The maximum current into a high-impedance state output pin when a low logic level is applied to the output pin.
MISCELLANEOUS		
C_{IN}	Input Capacitance	The input pin capacitance at a specified voltage and frequency.
C_{OUT}	Output Capacitance	The output or I/O pin capacitance at a specified voltage and frequency.
T_A	Operating Free Air Temperature	The ambient homogeneous temperature of the environment during operation.
T_C	Operating Case Temperature	The maximum chassis temperature during operation.
f_{MAX}	Maximum External Frequency	The $f_{MAX,External}$ is the maximum clocking frequency with external feedback. It is the reciprocal of the clock period ($t_s + t_{CO}$).
f_{MAX}	Maximum Internal Frequency	The $f_{MAX, Internal}$ is the maximum clocking frequency with internal feedback. It is the reciprocal of the clock period ($t_s + t_{CF}$).
f_{MAX}	Maximum Frequency without Feedback	The $f_{MAX, No\ Feedback}$ is the maximum clocking frequency with no feedback. It is the reciprocal of the sum of the data setup time (t_s) and the data hold time (t_h).

5

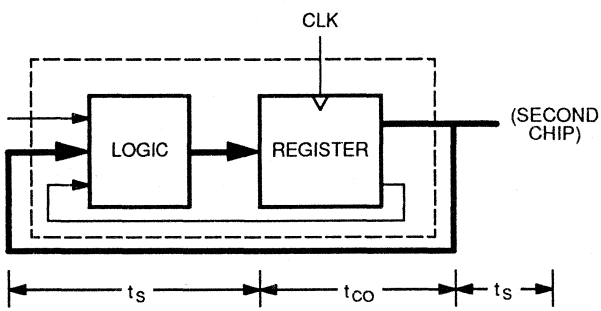
f_{MAX} Parameters

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

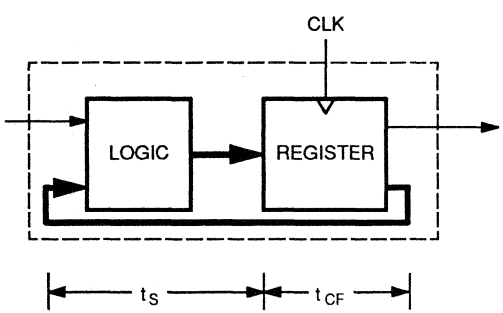
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal".

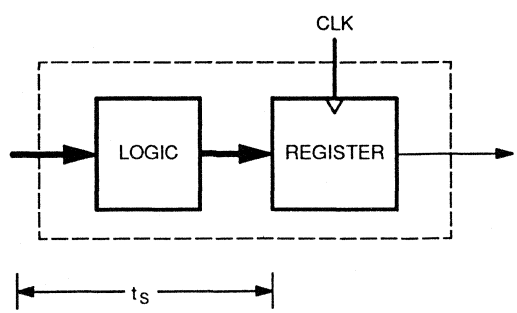
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".



f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal; $1/(t_S + t_{CF})$



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

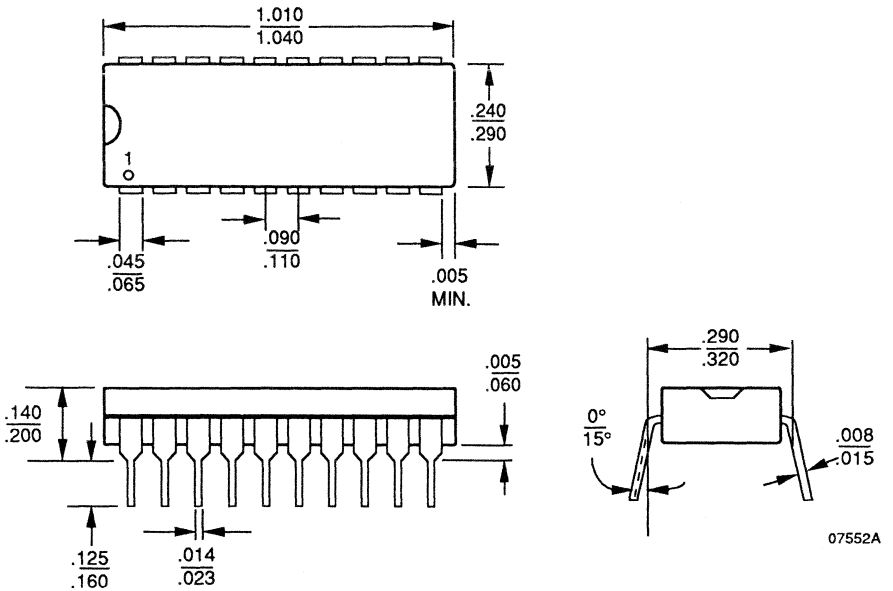
12350-022A

Publication #	Rev.	Amendment	Issue Date
12468	A	/0	1/90

Physical Dimensions*

Advanced Micro Devices

PD 020
20-Pin Plastic DIP



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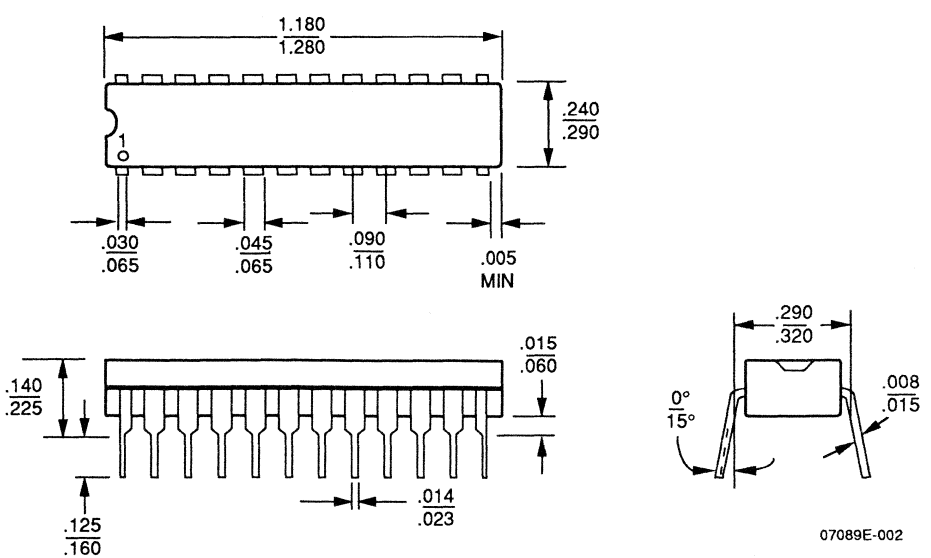
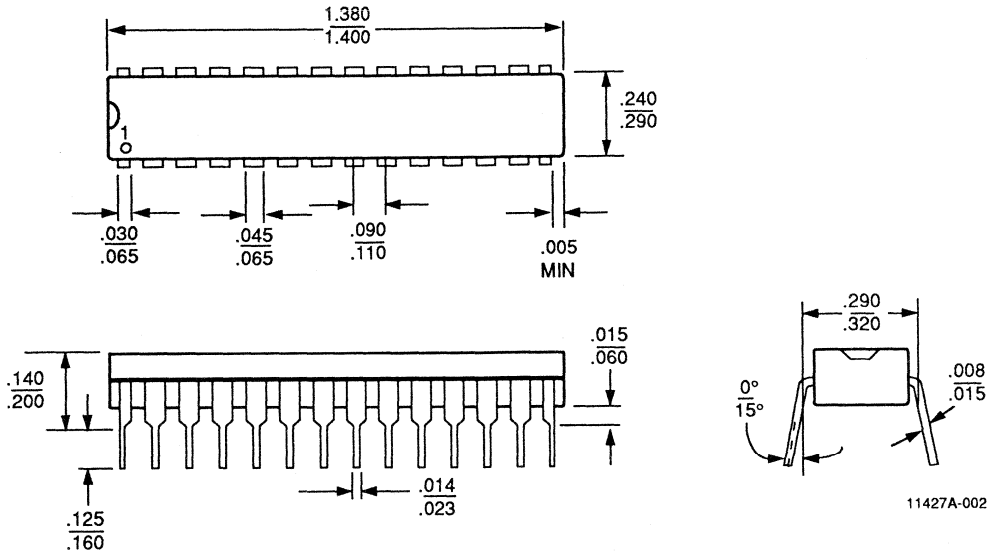
PD 3024
24-Pin 300-mil Plastic SKINNYDIP

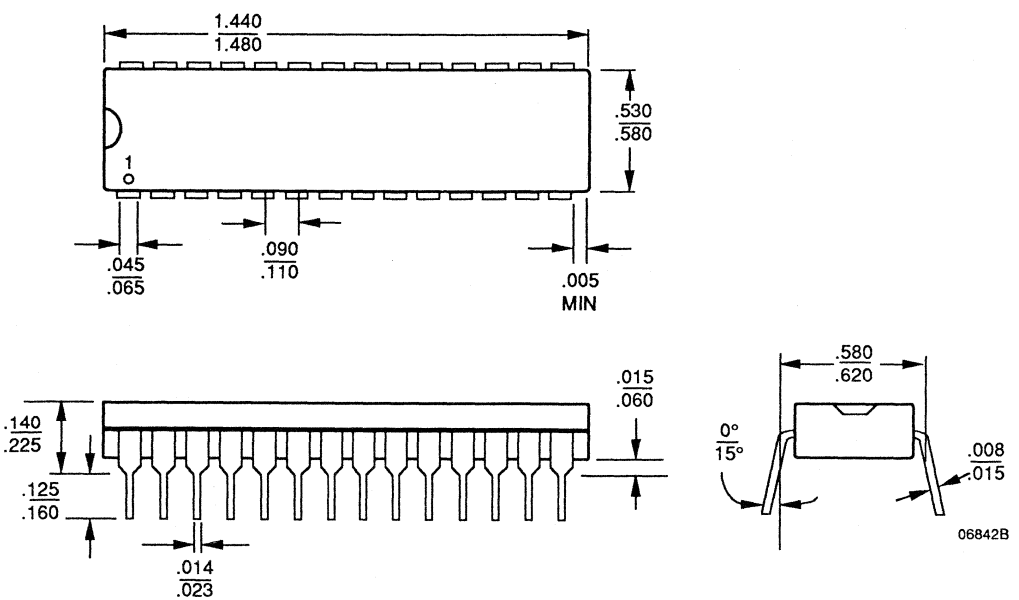


* For reference only. All dimensions measured in inches. BSC is an ANSI standard for basic space centering.

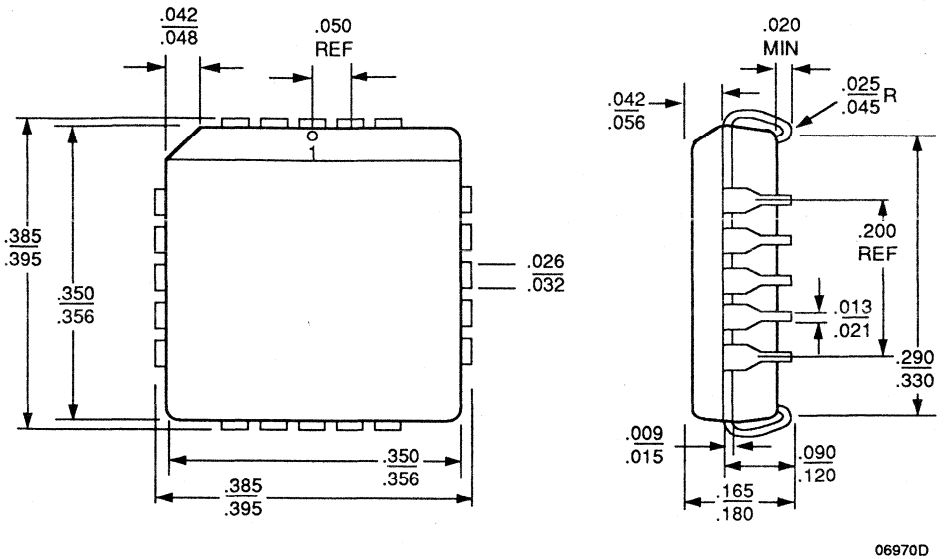
PD3028
28-Pin 300-mil Plastic SKINNYDIP



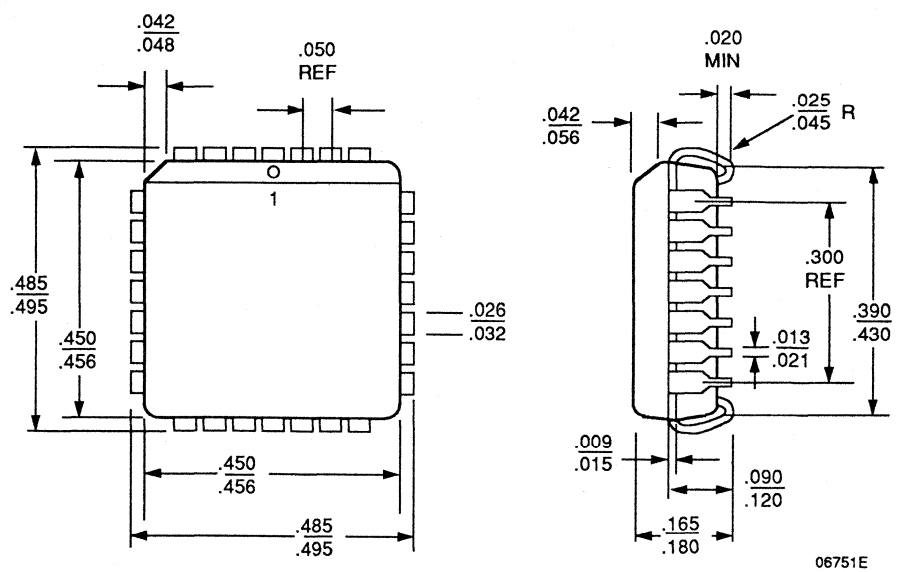
PD 028
28-Pin Plastic DIP



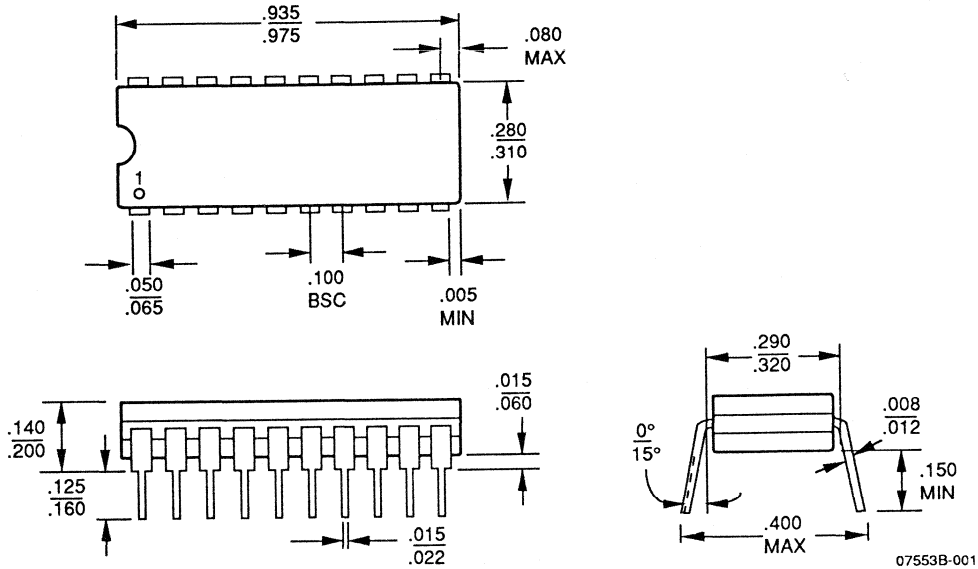
PL 020
20-Pin Plastic Leaded Chip Carrier



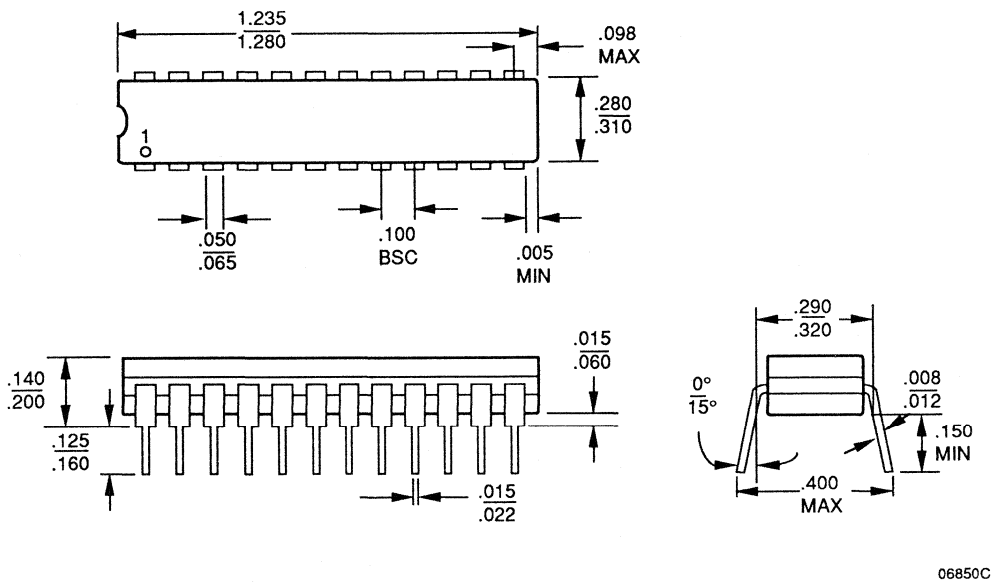
PL 028
28-Pin Plastic Leaded Chip Carrier



CD 020
20-Pin Ceramic DIP



CD3024
24-Pin 300-mil Ceramic SKINNYDIP



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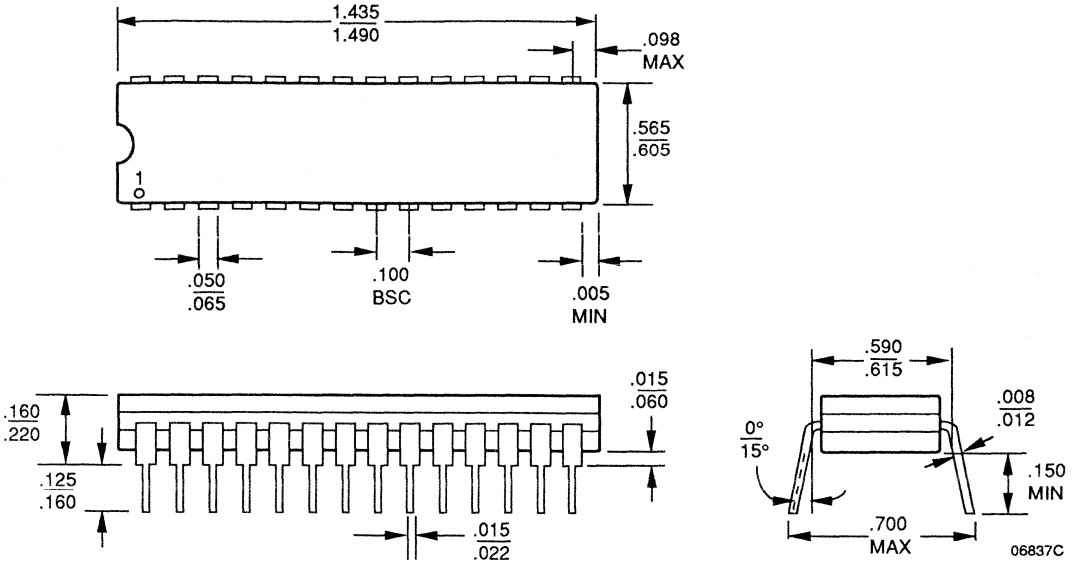
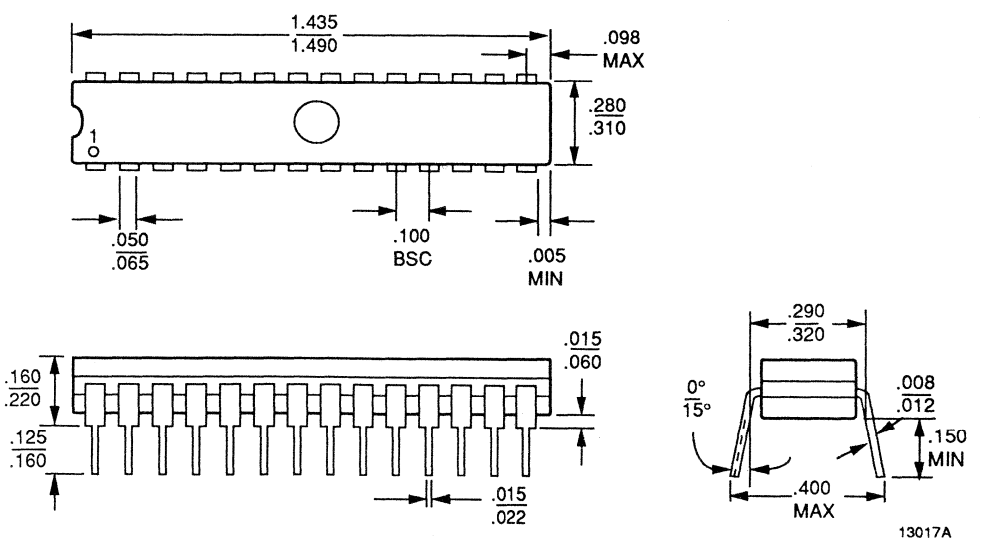
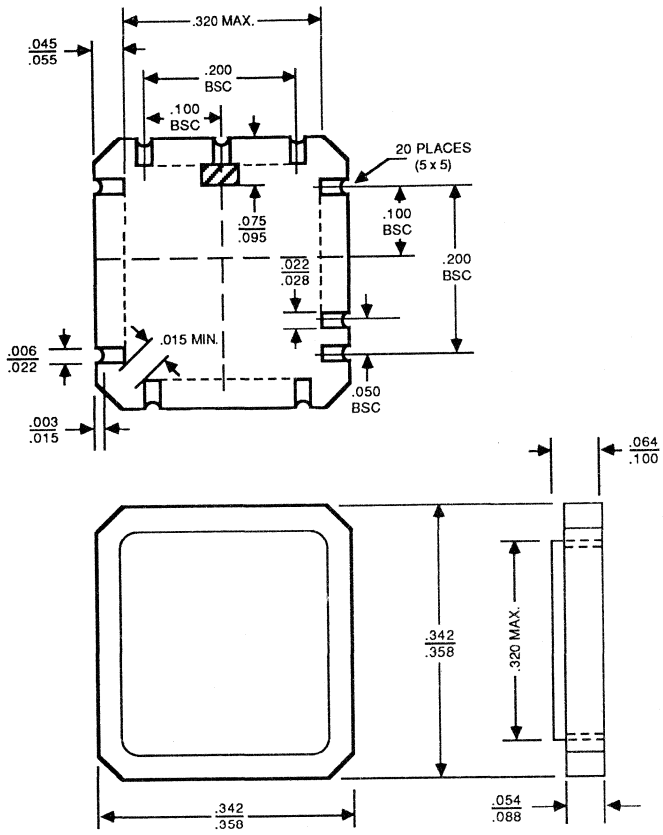
28-Pin Ceramic DIP



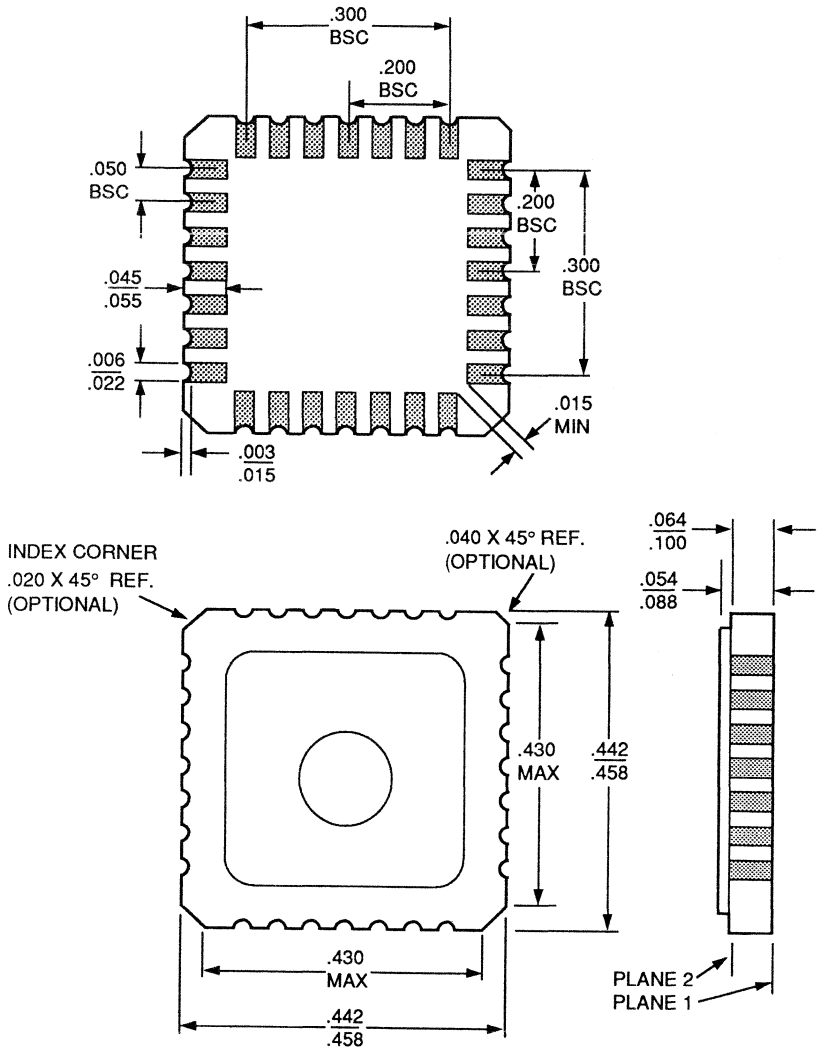
CDE028
28-Pin 300-mil Ceramic Windowed SKINNYDIP



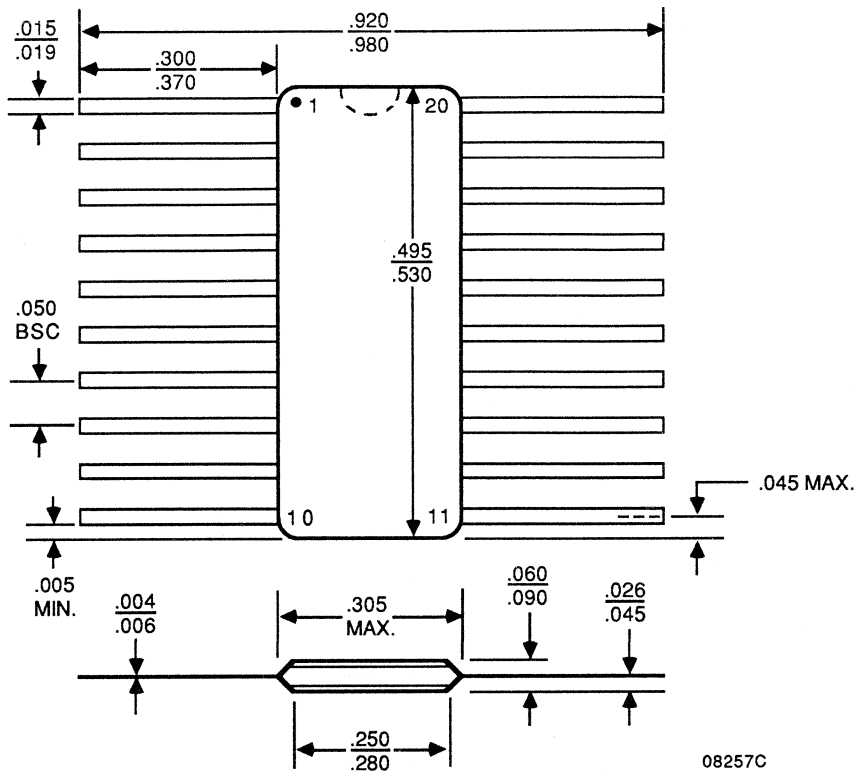
CL 020
20-Pin Ceramic Leadless Chip Carrier



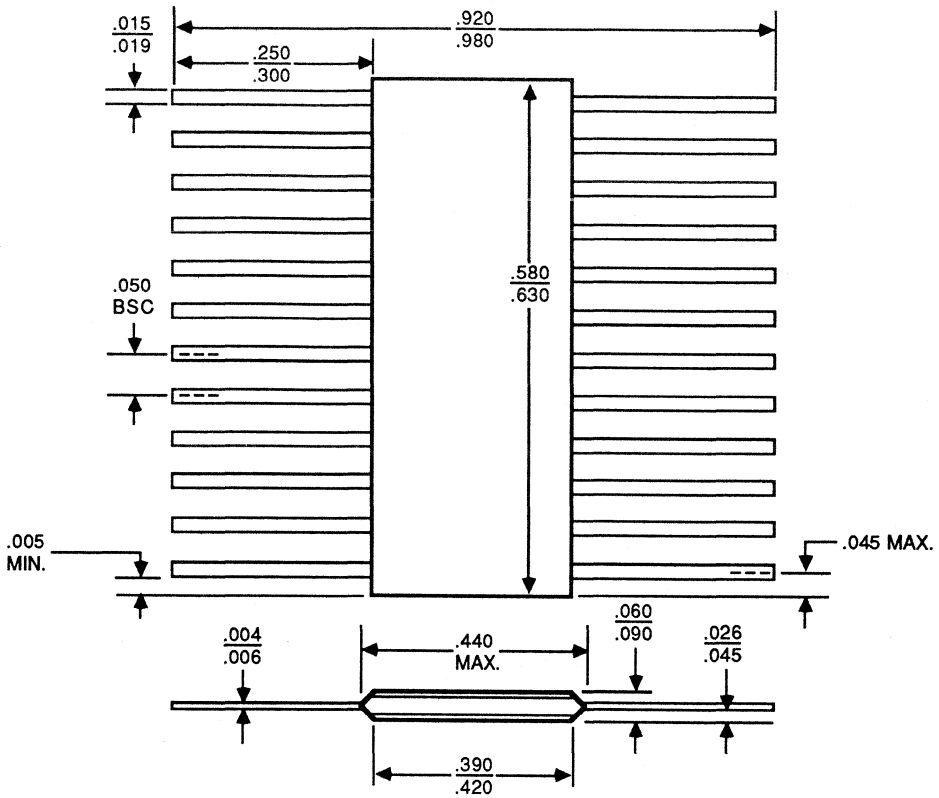
CL 028
28-Pin Ceramic Leadless Chip Carrier



CF 020
20-Pin Ceramic Flatpack



CFL024
24-Pin Ceramic Flatpack



5

Package Thermal Characteristics

Abstract

Determination of the Thermal Resistance of Packaged Devices is of concern to the designer of new devices and to AMD customers. The Advanced Package and Material Development group has undertaken the task of characterizing current AMD products and quantifying package-related influences on Thermal Resistance. This report describes some of these effects and the technique used to measure Thermal Resistance.

Definition of Thermal Resistance

The reliability of an integrated circuit is largely dependent on the maximum temperature which the device will attain during operation. Because the stability of a semiconductor junction declines with increasing temperature, knowledge of the thermal properties of the packaged device becomes an important factor during device design. In order to increase the operating lifetime of a given device, the junction temperatures must be minimized. This demands knowledge of the thermal resistance of the completed assembly and specification of the conditions in which the device will function properly. As devices become both smaller and more complex and the requirement for high speed operation becomes more important, heat dissipation will become an ever more critical parameter.

Thermal resistance is defined as the temperature rise per unit power dissipation above some referenced condition. The unit of measure is typically °C/watt. The relationship between junction temperature and thermal resistance is given by:

$$T_J = T_X + P_D\ \theta_{JX} \qquad (1)$$

where: T_J = junction temperature
T_X = reference temperature
P_D = power dissipation
θ_{JX} = thermal resistance
X = some defined test condition

In general, one of three conditions is defined for measurement of thermal resistance:

θ_{JC} – thermal resistance measured with reference to the temperature at some specified point on the package surface.

θ_{JA} (still air) – thermal resistance measured with respect to the temperature of a specified volume of still air.

θ_{JA} (moving air) – thermal resistance measured with respect to the temperature of air moving at a specified velocity.

The relationship between θ_{JC} and θ_{JA} is

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{CA} is a measure of the heat dissipation due to natural convection (still air) or forced convection (moving air) and the effect of heat radiation and mounting techniques. θ_{JC} is dependent solely on material properties and package geometry; θ_{JA} includes the influence of the surface area of the package and environmental conditions. Each of these definitions of thermal resistance is an attempt to simulate some manner in which the package device may be used.

The thermal resistance of a packaged device, however measured, is a summation of the thermal resistances of the individual components of the assembly. These in turn are functions of the thermal conductivity of the component materials and the geometry of the heat flow paths. Like other material properties, thermal conductivity is usually temperature dependent. For alumina and silicon, two common package materials, this dependence can amount to a 30% variation in thermal conductivity over the operating temperature range of the device. The thermal resistance of a component is given by

$$\theta = \frac{L}{K(T)A} \qquad (2)$$

where: L = length of the heat flow path
A = cross sectional area of the heat flow path
K(T) = thermal conductivity as a function of temperature

and the overall thermal resistance of the assembly (discounting convective effects) will be:

$$\theta = \Sigma\theta_n = \Sigma\ \frac{L_n}{K_n A_n}$$

but since the heat flow path through a component is influenced by the materials surrounding it, determination of L and A is not always straightforward.

A second factor that affects the thermal resistance of a packaged device is the power dissipation level and, more particularly, the relationship between power level and die geometry, i.e., power distribution and power density. By rearrangement of equation 1 to

$$P_d = \frac{1}{\theta_{JX}}(T_J - T_X) = \frac{1}{\Sigma\theta_N}(T_J - T_X) \qquad (3)$$

the relationship between P_d and T_j can be more clearly seen. Thus, to dissipate a greater quantity of heat for a given geometry, T_J must increase and, since the individual θ_n will also increase with temperature, the increase in T_J will not be a linear function of increasing power levels.

A third factor of concern is the quality of the material interfaces. In terms of package construction, this relates

specifically to the die attach bond, and for those packages having a heatsink, the heatsink attach bond. The quality of the die attach bond will most severely influence the package thermal resistance as this is the area which first impedes the transfer of heat out of the silicon die. Indeed, it seems likely that the initial thermal response of a powered device can be directly related to the quality of the die attach bond.

Experimental Method

The technique for measurement of thermal resistance involves the identification of a temperature-sensitive parameter on the device and monitoring this parameter while the device is powered. For bipolar integrated circuits the forward voltage of the substrate isolation diode provides a convenient parameter to measure and has the advantage of a linear dependence on temperature. MOS devices which do not have an accessible substrate diode present greater measurement difficulties and may require simulation through use of a specially designed thermal test die. Choice of the parameter to be measured must be made with some care to ensure that the results of the measurement are truly representative of the thermal state of the device being investigated. Thus measurement of the substrate isolation diode which is generally diffused across the area of the die yields a weighted average of the condition of the individual junctions across the die surface. Measurement of a more local source would yield a less generalized result.

For MOS devices, simulation is accomlished using the thermal test die. The basis for this test die is a 25 mil square cell containing an isolated diode and a 1 KΩ resistor. The resistors are interconnected from cell to cell on the wafer before it is cut into mulitple arrays of the basic unit cell. In use the device is powered via the resistors with voltage or current adjusted for the proper level and the voltage drop of the individual diodes is monitored as in the case of actual devices.

Prior to the thermal resistance test, the diode voltage/temperature calibration must be determined. This is done by measuring the forward voltage at 1 mA current level at two different temperatures. The diode calibration factor is then:

$$K_f = \frac{T_2 - T_1}{V_2 - V_1} = \frac{\Delta T}{\Delta V} \qquad (4)$$

in units of °C/mV. For most diodes used for this test the voltage/temperature relationship is linear and these two measurement points are sufficient to determine the calibration.

The actual thermal resistance measurement has two alternating phases: measurement and power on. The device under test is pulse powered with an ON duty cycle of 99% and a repetition rate of < 100 Hz. During the brief OFF states the device is reverse-biased with a 1 mA current and the voltage drop is measured. The series of voltage readings are averaged over short periods and compared to the voltage reading obtained before the device was first powered ON. The thermal resistance is then computed as:

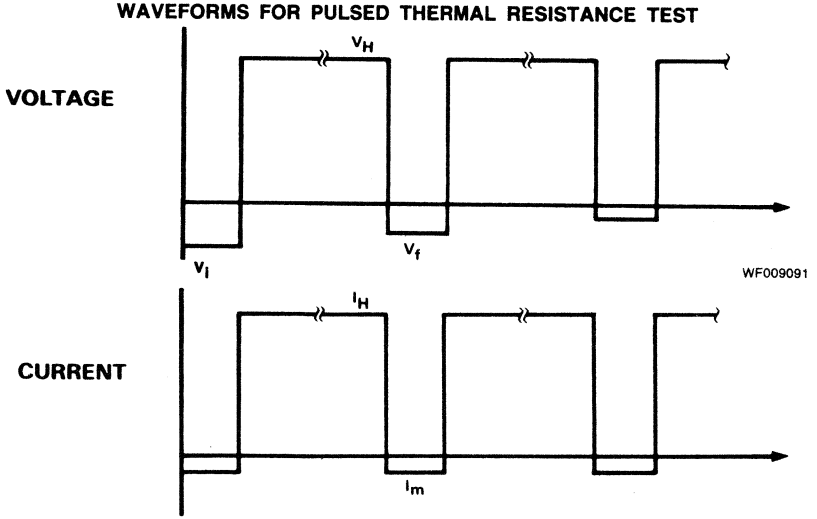
$$\theta_{jx} = \frac{K_F(V_F - V_I)}{V_H I_H} = \frac{K_f \Delta V}{P_D} \qquad (5)$$

where: K_F = calibration factor
V_I = initial forward voltage value
V_F = current forward voltage value
V_H = heating voltage
I_H = heating current

The pulsing measurement is continued until the device has reached thermal equilibrium and the final value measured is the equilibrium thermal resistance of the device under test.

When the end result desired is θ_{JA} (still air), the device and the test fixture (typically a standard burn-in socket) are enclosed in a box containing approximately 1 cubic foot of air. For θ_{JC} measurements the device is attached to a large metal heatsink. This ensures that the reference point on the device surface is maintained at a constant temperature. The requirements for measurement of θ_{JA} (moving air) are rather more complex and involve the use of a small wind tunnel with capability for monitoring air pressure, temperature and velocity in the area immediately surrounding the device tested. Standardization of this last test requires much careful attention.

WAVEFORMS FOR PULSED THERMAL RESISTANCE TEST



Experimental Results

The thermal resistance data included in the attached table was extrapolated from data collected using the procedure outlined in the preceding section. This data has resulted from an ongoing program undertaken by members of the Material Technology Development group.

Updated data will replace the data in this table as each device is measured or revised data becomes available.

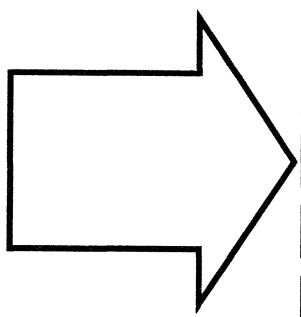
Thermal Resistance of AMD Products

(Notes 1, 2 and 3)

Package	Pin Count	Material	Type	Device	$\varnothing_{JA}$	$\varnothing_{JC}$
PD 020	20	Plastic	DIP	Typical AmPAL23S8	61 56	30 CR
PL 020	20	Plastic	PLCC	Typical	CR	CR
CD 020	20	Ceramic	DIP	Typical AmPAL18P8 AmPAL23S8 AmPAL23S8-30	60 65 59 63	11 9 5 5
CL 020	20	Ceramic	LCC	Typical	61	CR
CFL020	20	Ceramic	Flatpack	Typical	56	CR
PD3024	24	Plastic	SKINNYDIP	Typical AmPAL22V10 PAL22V10-15	60 58 63	CR CR CR
CD3024	24	Ceramic	SKINNYDIP	Typical AmPAL22V10 PAL22V10-15	57 56 58	15 15 8
CFL024	24	Ceramic	Flatpack	Typical AmPAL22V10	85 85	9 4
PD3028	28	Plastic	SKINNYDIP	Typical	CR	CR
PD 028	28	Plastic	DIP	Typical	CR	CR
PL 028	28	Plastic	PLCC	Typical AmPAL22V10 PAL20L8A	58 60 60	CR CR CR
CDE028	28	Ceramic	Windowed SKINNYDIP	Typical	CR	CR
CD 028	28	Ceramic	DIP	Typical	CR	CR
CL 028	28	Ceramic	LCC	Typical AmPAL22V10	CR 63	CR CR

Notes:

1. Representative values for each package type — for information only.
2. Any given device may differ from these values. Consult local AMD sales office for specific device information.
3. CR = Consult local AMD Representative
4. DIP = Dual-In-Line Package
   LCC = Leadless Chip Carrier
   PLCC = Plastic Leaded Chip Carrier



Design and Programming

Design Software for Programmable Logic

Introduction

Programmable logic design software translates a custom logic design specification into a format which can be accepted by a programmer (Figure 1).

Programmable logic software is also an excellent tool for design simulation and documentation. Simulation assists in debugging an initial design and helps to ensure that a device will operate as intended the first time instead of requiring multiple design iterations. Documentation is essential for someone other than the original designer to understand a custom programmable logic specification.

This overview will describe the basic components of PLD design software packages, including assistance in logic simulation and testing. Several software packages are available; some are listed at the end of this overview.

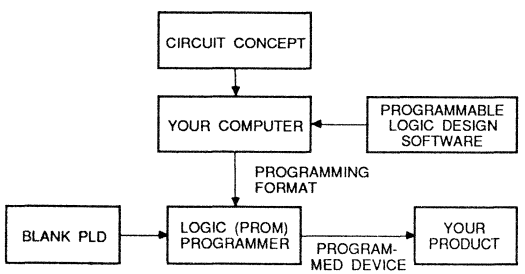


Figure 1. The Programmable Logic Development Cycle

Design Software for Programmable Logic

PLD design software lets the designer write logic descriptions at a high level, that is, at a level that accurately reflects the design concept. This type of software increases productivity while producing designs that are thoroughly documented.

The software should support all programmable logic device types, all popular logic (PROM) programmers, and a large number of popular development computers. In addition, software products offer a variety of input design formats such as state machines, high-level Boolean equations, truth tables and logic schematics.

A compiler's syntax offers a general and easy description of the desired configuration of the chosen programmable logic device.

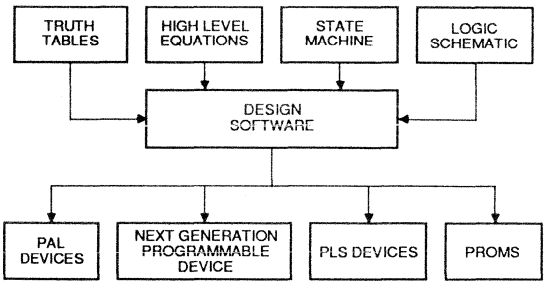


Figure 2. The Compiler

In addition, the high-level description of the design provides flexibility in changing the design if so desired. A designer might initially use a particular type of PLD. Later, when fixes or enhancements are made, the design can be quickly re-compiled for the same device. If the changes require more product terms or an architectural configuration that the chosen PLD cannot support, the function can easily be placed in an alternate device. In many cases this will allow design modifications without altering printed circuit boards which may have already been manufactured.

Logic Simulation

Most of the PLD software design tools also offer logic simulation. Logic simulation is typically performed to verify the logical design prior to programming an actual device. This may save some of the time spent trouble-shooting a programmable logic design using conventional techniques, using an oscilloscope and logic analyzer.

A simulation file consists of stimulus patterns applied to inputs and response patterns expected at outputs. The simulator compares each stimulus/response pattern, or vector, with the logic equations to verify that the expected response agrees with that produced according to the equations.

Not simulating may be of little consequence for simple designs, but for complex designs, especially complex sequential logic, it is well worth the time.

Testing Programmable Logic

PLD software design tools also assist the designer in testing the PLD after it has been programmed.

Before shipping a PLD, programmability may be verified by the manufacturer by exercising the device's address and programming circuitry on redundant test sites.

Publication #	Rev.	Amendment	Issue Date
14087	A	/0	1/90

After the device has been received and programmed by the user, the logic programmer will read the states of all the fuses in the device and compare them with the data stored in the programmer's memory to check the status of the programming matrix, in its verify cycle. If any mismatches are detected, the device is rejected.

However, a correct fuse verify does not guarantee that the device will work properly, since the fixed logic of the device has not been fully tested (Figure 3). To ensure proper operation the device must be functionally tested.

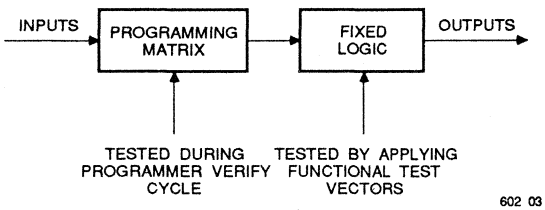
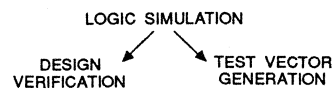


Figure 3. Programmable Logic Device Testing

Functional testing of PLDs involves applying stimulus patterns to a device while looking for the expected response. The test sequence consists of a table of stimulus/response patterns similar to those used to perform a simulation. PLD software design tools offer the capability of generating these test vectors.

Test vectors are produced by creating a simulation input file containing stimulus/response patterns. After running the simulator to verify the integrity of the vectors, they are appended to the JEDEC down-loadable file which already contains the programming patterns for the particular target device.

We can now see that there are two distinct benefits of logic simulation in working with PLDs:



Software Tools

Many different programmable logic design aid software programs are available. Table 1 lists some current suppliers of these design tools. Contact the indicated companies for the status of their particular product.

SOFTWARE	VENDOR
PALASM® 90 Software (PAL and PLS devices) Am29CPL100 Software (Am29CPL151/4) PEGPDS™ (Am2971) Programmable Gate Array Software (Am2000/3000 Series)	Advanced Micro Devices Contact local sales office
ABEL™ and PLDlinx™ FutureDesigner™ PLDtest® and PLDtest Plus™ (Vector Generation)	Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444
CUPL™	Logical Devices 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405
LOG/iC®	ISDATA 800 Airport Road Monterey, CA 93940 (408) 373-7359
PLDesigner®	Minc Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155
OrCAD/PLD™	OrCAD Systems Corporation 1049 S.W. Baseline Street, Suite 500 Hillsboro, OR 97123 (503) 640-9488
Anvil ATG™ (Vector Generation)	Anvil Software, Inc. 427-3 Amherst Street, Suite 391 Nashua, NH 03063 (603) 891-1995
Test Generator (Vector Generation)	ATG Associates 3415 Merrill Road Aptos, CA 95003 (408) 475-5717

Table 1. Software Support

PALASM® 90 Software

High-Performance Support Tools

PALASM 90 CAD software is an integral part of the AMD programmable logic solution. As PAL devices and other PLDs have grown more powerful and complex, our team of software engineers has added major enhancements to PALASM software. The goal is to provide timely, state-of-the-art software support for every new PAL device at market introduction. The result is software that enables you to configure a PLD quickly, easily, and effectively.

Freedom to Express Your Designs in Different Forms

PALASM 90 software offers you increased design flexibility. You have the option of creating your design file with Boolean or State equations. The powerful PAL device design specification syntax has the advantage of being flexible enough for complex designs, without compromising ease-of-use. The basic operators INVERT, AND, OR, and EXCLUSIVE-OR can be used to describe any logic function using Boolean equations. The high-level constructs IF-THEN-ELSE and CASE have been added to the Boolean syntax, along with support of vectored expressions. The syntax for State equations is equally easy to use.

Powerful Simulator Provides Automatic Testing

PALASM 90 software has a powerful, event-driven simulator that cuts down the margin of design error significantly. It enables simulation of the design before the chip is programmed. This means you can go back and edit the design as many times as you want without wasting a single chip. The simulator's English-like commands allow you to describe functions easily. It performs a validation of your design, and generates vectors from a test sequence that you specify. PALASM 90 software's simulation makes testing of the design an integral part of creating the design. This means that every time you insert a PAL device into the programmer, you can be sure it will be accurately programmed.

Automatic Logic Reduction for Cost-Effective Design

PALASM 90 software gives you the option of automatically reducing your logic equations, enabling you to utilize your PAL device fully. Now you don't have to go through tedious manual reduction and DeMorganization. The software does the work for you. Reduced logic leads to cost-effective design, since less device space is used. By conserving space, design efficiency is increased, as more complex logic can be packed into the device.

Edit Programmed Device Designs

PALASM 90 software offers you the unique ability to edit programmed device designs. Its time-saving JEDEC manipulator enables you to read a fuseplot directly from a programmed device, and disassembles the fuse information back to Boolean equations. If you wish to alter the design, you can edit the Boolean equations that the JEDEC manipulator generates.

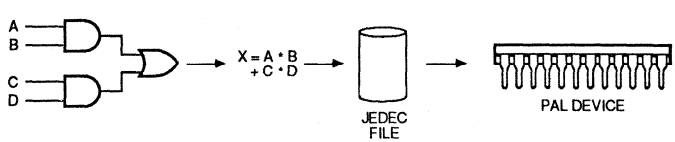
Easy-to-Use Windowed Interface

The power of PALASM 90 software has been harnessed by a powerful new user interface. Pull-down menu options allow you to modify, assemble, and simulate your design; view any data, including simulation waveforms; and download JEDEC files to a programmer. And, all of the assembly and simulation processes can be chained together so that one command completes the entire process. Errors are flagged on-screen and in a log file for examination later. The result is a smooth, integrated design environment that allows you to design logic easily and efficiently.

Hardware Support

PALASM 90 software is supported on the following systems:

- IBM-PC/XT/AT, PS/2, and compatibles
- VAX-VMS
- Sun workstations
- Apollo workstations



14088-001A

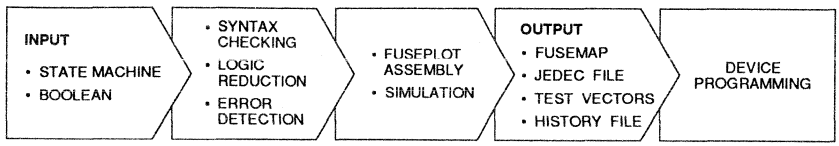
Publication #	Rev.	Amendment	Issue Date
14088	A	/0	1/90

Documentation

PALASM 90 software is fully documented in its own User's Manual. In addition, a free hotline is provided to answer any questions you may have about the software or about AMD devices. The hotline number is (800) 222-9323.

Design Software for PLDs

We believe that PALASM 90 software and AMD PLDs are firmly linked. From immediate device support to documentation to field service: PLD support and software support are one and the same. It is through this philosophy that PALASM software has become the world's most widely-used PLD design package, and a natural complement to AMD PLDs.



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The Field-Programmable Controller devices (Am29CPL151 and Am29CPL154) are supported by dedicated software that takes advantage of the instruction-based nature of the devices.

ASM14X is the name of the assembler program that accepts the user's design description and creates a programming file. The SIM14X simulator can be used to verify the design before actually programming the device.

ASSEMBLER FEATURES

The ASM14X Assembler provides high-level microprogramming support for the Am29CPL151/4 Field-Programmable Controllers. High-level language constructs such as IF-THEN-ELSE and WHILE allow the programmer to write microcode in a logical and more conversational syntax. This enhances code documentation because the microcode is expressed in a readable and easy-to-follow format.

Assembler features include:

- Binary, octal, decimal, and hexadecimal numbers are recognized
- Jump/branch to labels
- Logic equations for control outputs
- Error detection and diagnosis
- Default test condition
- JEDEC standard fuse map output
- Symbol table output

Statement Formats

The assembler recognizes four statement formats:

1. IF (<cond>) THEN <action> [ELSE <action>]
2. WHILE (CREG <> 0) <action> [ELSE <action>]
3. CONTINUE
4. CMP TM(<mask>) TO PL(<constant>)

The <cond> refers to the test condition that is evaluated before performing the <action> specified in the statement. The <action> can be opcodes such as GOTO, LOAD, and CALL. See the Am29CPL151/4 data sheets for more details on instruction syntax and device operation.

SIM14X SIMULATOR

The SIM14X simulator provides complete high-level software simulation for the Am29CPL151/4 devices. The SIM14X simulator uses a JEDEC fuse map file, generated by the ASM14X assembler, and a test-vector file as its inputs. The simulator then computes output signals and compares them against the expected output values specified in the test vector file. If any differences are detected, the simulator flags the errors by placing a "?" under the unmatched output signals.

The SIM14X simulator displays complete status information including all input pin signals, computed and expected output signals, and contents of all internal registers. You can use the interactive mode of operation to specify points in the program to stop and check operations. You can even execute another program during simulation, to run a DOS command that assists in your program development.

In addition to providing break-point and single-step capability, the SIM14X simulator allows you to preload or change all internal registers interactively. Figure 1 shows the simulator/test vector environment.

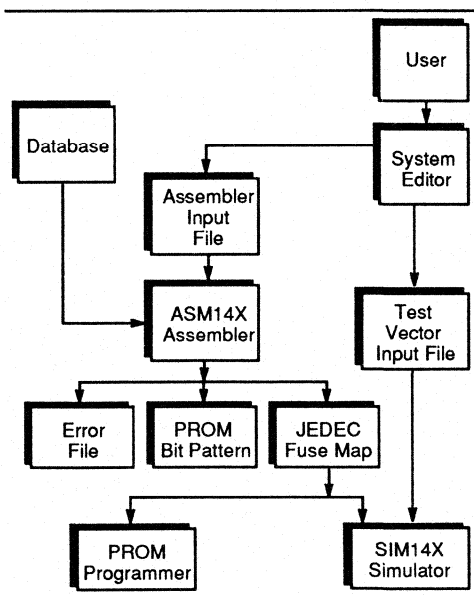

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Figure 1. Simulator/Test Vector Environment

Publication #	Rev.	Amendment	Issue Date
14089	A	/0	1/90

Simulator Output

Unless you choose otherwise, the simulator displays the contents of all internal registers, OPCODE mnemonics of the current OPCODE field in the pipeline register, and the source of the contents of pipeline register. Also displayed for the instruction in the pipeline register is the value of the condition being tested, whether the instruction passes or fails and T*M, wherever applicable.

Remember that all inputs, outputs and register values displayed in an output screen are values at a rising clock edge. Each <return> in the single step mode can be thought of as a rising clock edge.

System Requirements

You need the following hardware and software to use the Assembler and Simulator:

Hardware (minimum configuration):

- an IBM PC/XT or other PC compatible with at least 256K bytes of RAM memory
- PC-DOS Version 2.0 or higher or MS-DOS Version 2.11 or higher
- A word processor to create the assembler source file. Any word processor which produces standard ASCII output files is acceptable. For example, you can use Wordstar in non-document mode.

Programmable Gate Array Software from AMD

Programmable Gate Arrays (PGAs) from AMD offer you higher levels of system integration with the advantages of user-programmability. AMD also provides a complete range of software packages to support PGA designs.

PGAs incorporate flexible blocks of configurable logic in a matrix fashion interfaced with a network of programmable interconnections. This network of logic blocks is surrounded by a ring of programmable I/O blocks. This unique architecture offers the capability to implement logic designs efficiently and effectively. On-chip logic allows configuration data to be loaded automatically at power-up, or the device can be reconfigured on-the-fly.

Designing with PGAs is done quickly and easily with modular software packages that run on the IBM PC. The software allows you to enter a design, automatically place and route it, and verify function and timing, all within a matter of days. Once you are satisfied with the design, the appropriate configuration data can be created to personalize the device. Configuration data can reside in an EEPROM, EPROM, or ROM on the circuit board or on a floppy or hard disk.

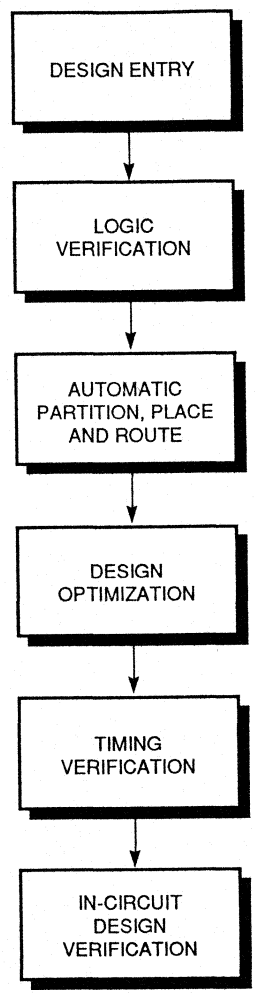
The discussion below outlines the tasks necessary to implement a PGA design. The complete range of software tools available from AMD allows you to accomplish gate array designs to 9000 equivalent gates at your desk, reducing design time, cost, and risk.

PGA Design Cycle

Designing with PGAs is a simple process, and AMD design tools are available for every phase in the design cycle. The diagram to the right shows the six steps in designing with PGAs.

Design entry can be accomplished by using the OrCAD/SDT™ III Schematic Design Tools, available as part of the PGA Bundled Development System (AmPGA151). For users with other schematic capture systems already in place, AMD also offers PGA interfaces to the Mentor™ and DAISY™ workstations and to the FutureNet® Design package. In addition to the interfaces available from AMD, Valid™ workstation interfaces are available from Valid Logic Systems. In all cases, you use the PGA symbol library that is part of your schematic capture interface package.

Logic verification is an optional step that can be done at this point in the design cycle through the use of a logic simulator. The PGA Development System with Simulation (AmPGA251) includes the OrCAD/VST™ simulation tool. PC-SILOS™ (AmPGA022) is also available from AMD for simulation. Simulation capabilities are also available from supported CAE systems.



PGA Design Flow

Automatic partitioning, place and route is performed by the Automatic Design Implementation (ADI) software, included in each of the bundled development systems. Unused and redundant logic is eliminated and the design is partitioned into PGA resources (logic and I/O blocks). Automatic reduction and partitioning allows designers to immediately determine the PGA size required, during design definition and entry. During the automatic place and route phase of design, users can define timing constraints through critical nets and automatically place and route the total design.

Design optimization can be done either by returning to your schematic capture software or through the use of the PGA Design Editor. With the design editor, you can perform such tasks as moving blocks, rerouting nets and adding or deleting logic. A timing calculator, part of the design editor, permits point-to-point timing determinations for critical path analysis.

Timing verification is an optional step that can be done once the design has been placed and routed to your satisfaction.

In-circuit design verification is done in one of three ways. An in-circuit emulator is available to simulate the circuit (AmPGA028). In addition, during design debug, designers can save time by using the download cable to transfer the configuration program from the PC directly into a PGA under development. Once the design is complete, a PROM file is created to be loaded into a PROM via a PROM programmer.

You iterate these steps until your design is correct. You can quickly correct design errors by making changes in your original design and repeating the subsequent steps. Even if you detect an error during in-circuit design verification, you can make corrections quickly and easily.

PGA Bundled Development System with Simulation (AmPGA251)

The PGA Bundled Development System offers complete capabilities for the implementation of a Programmable Gate Array design. Packaged together are the OrCAD/SDT III Schematic Design Tools, OrCAD/VST Verification and Simulation Tools, Automatic Design Implementation, and the PGA Development System.

Each part of a bundled PGA system is designed to perform one of the PGA design tasks described above. Below is a summary of the features of each of the components of AMD's bundled PGA software.

OrCAD Schematic Design Tools

OrCAD/SDT III is a complete schematic package, designed to place Computer Aided Engineering power at the desk of every engineer. Easy to use menu driven commands make it possible to create, edit, save, and print design schematics. The graphical editing capabilities allow single objects or groups of objects to be easily moved, replicated, or deleted. OrCAD/SDT III can store over 100 individual macros, each executed with a single keystroke.

Designs can be entered hierarchically to manage the complexity of large designs. Designers can flag critical timing paths to ensure that critical signals are routed with minimum delay. A wide range of graphics boards are supported, with an extensive selection of printers and plotters for output.

In addition to the OrCAD/SDT III software, all bundled systems contain the interface necessary to design for PGAs, and the PGA macro library of almost 300 TTL and SSI/MSI standard family equivalents.

OrCAD Verification and Simulation Tools

OrCAD/VST is a full-featured, 12-state, event-driven logic simulator, capable of handling designs of 14,000 gates at an evaluation speed of 10,000 events per second, and can simulate more than 2 billion time units. The package integrates a stimulus generator, design linker, and design compiler into a simulation environment. A netlist is all that is required to get started. The link and compile steps are automatically performed, and the stimulus is defined within an integrated pop-up editor, enabling you to initialize signals, generate any kind of clock signal, and perform test vector definition.

Definition of signals that are to be traced or displayed is performed by the Trace Editor. Displays can be defined as signals or buses. Buses can be displayed as binary, octal, decimal or hexadecimal. OrCAD/VST's logic analyzer style format simplifies data analysis. Signals and bus values are easily viewed, displayed as a window into the trace buffer. Four zoom levels enable you to magnify the traces. Up to three markers may be placed on the screen to measure time intervals quickly.

In addition to the OrCAD/VST software, all bundled systems contain the interface necessary to use Simulation and Verification with PGAs, and the PGA macro library of almost 300 TTL and SSI/MSI standard family equivalents.

Automatic Design Implementation

The Automatic Design Implementation package enhances the productivity of designers using PGAs by reducing design placement and routing time, and at the same time, maintaining flexibility. Designs that are developed incrementally can take advantage of automatic placement and routing by locking partial PGA layouts in place while automatically placing and routing design additions.

The automatic placement and routing program is extremely flexible. Through placement directives, the user can control the placement process to achieve the best arrangement for a particular design. Routing resources can be specified to minimize clock skews and signal delays for critical paths. The result is faster product development.

PGA Design System

The PGA Development System provides users with a complete design and development system for specification and implementation of designs using PGAs. Functional definition of configurable logic blocks (CLBs), input/output blocks (IOBs), and interconnections is performed with a menu-driven interactive graphics editor. Functions are specified by CLB and IOB definitions plus their interconnections. The macro library and user-defined macros enable the user to easily implement complex functions. The check for logic connectivity and design rule violation is easily performed. All unused internal nodes are automatically configured to minimize power dissipation.

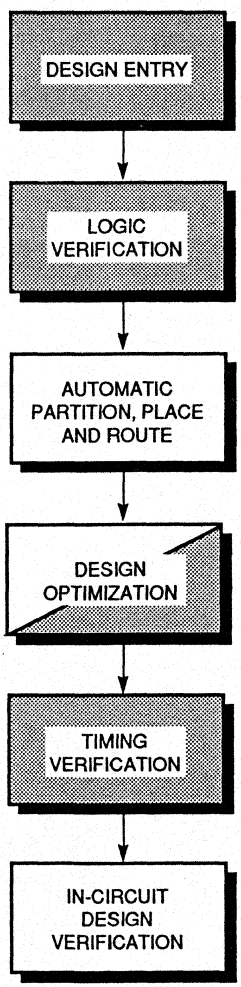
Interactive point-to-point timing delay calculation is provided for timing analysis and critical path determination. This ability enables the user to quickly identify and correct timing problems while the design is in progress.

A bundled development system without simulation (AmPGA151) is also available. Each piece of a bundled system may also be purchased individually. In addition, for those users who already have OrCAD software, a package containing only the PGA interface and library provides the necessary components to produce PGA designs using OrCAD tools (AmPGA035 and AmPGA045).

Workstation Support

With the AmPGA151 and AmPGA251 bundled development packages, AMD provides a complete, PC-based environment in which to design for PGAs. However, support is also available for a variety of CAE workstation products. In using one of these workstations, you move from the workstation environment to the PC environment and back, depending on the task. Below, in the diagram of the PGA design tasks, the shaded boxes represent tasks performed on the workstation and the white boxes denote PC-based tasks.

Currently, AMD supports workstations from Daisy/Cadnetix, Inc. and Mentor Graphics Corporation. A package is available from AMD for each of these systems, containing the PGA interface and library necessary to design for PGAs. In addition, the PGA interface and library for Valid EDA Systems is available from Valid Logic Systems.



PGA Design Flow

Daisy Schematic Capture and Simulation Interfaces (AmPGA133)

The Daisy interfaces from AMD allow the Daisy workstation user to enter a PGA design. It includes the following features:

- Full support of timing verification through back-annotation to the CLB or gate level
- Macro library of over 100 TTL and standard logic family equivalents
- User control of flagging critical paths
- Use of familiar Daisy design entry methodology
- Output compatibility with PGA Development Software
- Hardware, software support

Hardware platforms:

- IBM PC-AT™
- Daisy

Software:

- DNIX Operating System
- ACE™/DED graphic schematic editors
- DLS™ Logic Simulator
- PGA library

Mentor Schematic Capture and Simulation Interfaces (AmPGA134)

The Mentor interfaces from AMD allow the Mentor workstation user to enter a PGA design. It includes the following features:

- Full support of timing verification through back-annotation to the CLB or gate level
- Use of familiar Mentor design entry methodology
- Macro library of over 100 TTL and standard logic family equivalents
- User control of flagging critical paths
- Output compatibility with PGA Development Software
- Hardware, software support

Hardware:

- All Apollo platforms

Software:

- Apollo Aegis Operating System
- IDEA Applications
- NETED™ Schematic Editor
- QuickSIM™ Logic Simulator

Valid Schematic Capture and Simulation Interfaces

The Valid/PGA interfaces from Valid Logic Systems allow the Valid EDA Systems user to enter a PGA design. It includes the following features:

- Full support of timing verification through back-annotation to the CLB level
- Use of familiar Valid design entry methodology
- Macro library of over 100 TTL and standard logic family equivalents
- Output compatibility with PGA Development Software
- Hardware, software support

Hardware:

- Sun
- Digital
- IBM PC-AT
- Valid

Software:

- ValidGED™ Graphics Editor
- ValidSIM™ Interactive Logic Simulator
- ValidTIME™ Timing Verifier

For more information about the Valid/PGA interface, contact

Valid Logic Systems
2820 Orchard Parkway
San Jose, California 95134
(408) 945-9400

Valid International
Valid House
39 Windsor Road
Slough Berkshire
SL1 2EE England
44 (75) 382 0101

Nihon Valid Logic Systems Co., Ltd.
Tokyo Building
2-16-8 Minami-Ikebukuro
Toshima-Ku, Tokyo 171, Japan
81 3 980 6421

Data I/O offers PLDlinx and ABEL (Advanced Boolean Expression Language); two design tools used to convert high-level design descriptions into optimized PLD implementations. The output of these tools is the JEDEC file (Standard 3A) used in all PLD programmer technology. The JEDEC file, which contains the fusemap (lists of binary values) that reflects the design to be implemented into the target PLD, does not have a format that is practical for describing the design. However, both PLDlinx and ABEL offer practical methods for describing designs to be implemented into one or more PLDs. PLDlinx provides for design entry through schematic diagrams and supporting text, and creates a source file that is passed to ABEL. ABEL also allows design entry, but through equations, state diagrams, and truth tables. In addition, ABEL provides design optimization through logic reduction, and allows simulation and testing of the design before generating the JEDEC file.

PLDlinx

The main function of PLDlinx is to process a design that is expressed as a schematic diagram to a form that is an acceptable source file for ABEL. To do this, PLDlinx translates the connectivity data produced from the schematic into Boolean equations that are correctly formatted for input to ABEL. The schematic diagram is drawn using the FutureNet® DASH™ Schematic Entry System (or DASH-PLD, a low-cost PLD-only version of DASH) and its logic symbol library. The resultant drawing file is then processed for application to PLDlinx as indicated in the flow diagram of Figure 1. Generic logic devices, and a subset of TTL devices, are expressed in a discrete function library of Boolean equations that is accessed by PLDlinx. Device descriptions can be added to the library at any time to include new and special devices. The discrete function library, in conjunction with the file produced by the drawing preprocessor, provides PLDlinx with all the information necessary to create Boolean equations that reflect the design. These equations can then be used by ABEL to develop the JEDEC file for the PLD programmer. A second library, containing descriptions of each PLD supported by PLDlinx, is used to verify input and output pin assignments, and to verify that the design is compatible with the chosen programmable logic device.

Hierarchical Designs

PLDlinx allows you to express designs in a hierarchical manner where designs are drawn as modular design functions by means of functional block symbols. Modularizing a design by function simplifies design management and reduces processing time when design changes occur. A hierarchical drawing method also allows you to use (include) some common logic functions in your design without the need to draw them repeatedly. In the following example, for instance, a logic function, such as a four-bit counter, or a T-type flip-flop, is entered once and then simply included in the next higher drawing in the hierarchy.

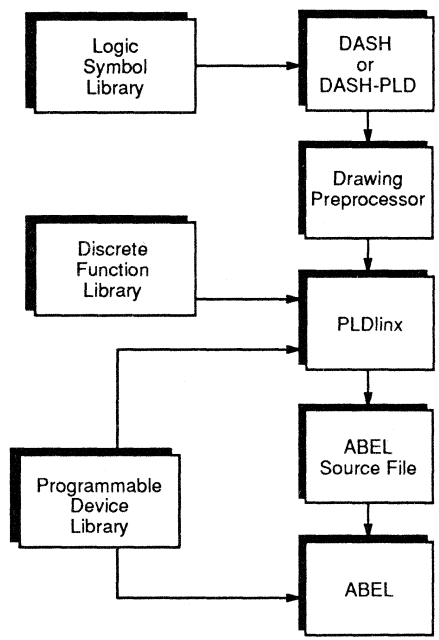
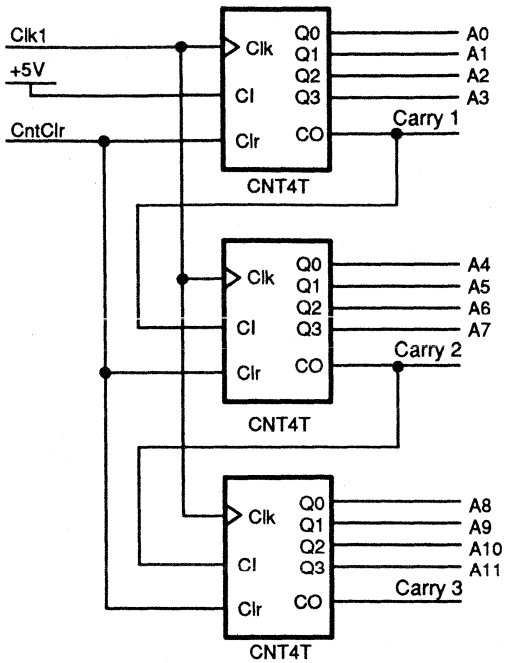


Figure 1. PLDlinx processes a design that is expressed as a schematic diagram to a form that is used as a source file for input to ABEL

An example of a hierarchical design is shown in Figure 2. This illustration shows a top level schematic for a simple 12-bit counter made up of three identical four-bit counters, and that resets to zero when a count of 3456 (decimal) is reached. The four-bit counters are represented by three identical functional blocks named CNT4T that show no internal circuit details, but only inputs, outputs, and interconnections. A declaration box lists the include box named cnt14.inc so that PLDlinx will process the equations and test vectors listed in that box.



DECBOX

```
mod:  _COUNTER;
title: Counter;
fusefile: cnt14;
dev: P29M16;

in:   Clk1,CntClr     =    1,2;
out:  [A0 . . A7]     =   [15 . . 22];
out:  [A8 . . A11]    =   [4 . . 7];
out:  Carry0, Carry1, Carry2  = 3,9,10;
out:  Terminal_Cnt    =   8;
set:  Count      =    [A11 . . A0];
inc:  cnt14.inc;
```

cnt14.inc

```
Equations
   Count.oe = !0;
   Terminal_Cnt = (Count = = 3456);
test_vectors  ([Clk1 ,  CntClr] ->     Count)
               [.C.   ,   1   ]  ->    ^h00;
               [.C.   ,   0   ]  ->    ^h01;
               [.C.   ,   0   ]  ->    ^h02;
               [.C.   ,   0   ]  ->    ^h03;
               [.C.   ,   0   ]  ->    ^h04;
               [.C.   ,   0   ]  ->    ^h05;
               [.C.   ,   0   ]  ->    ^h06;
               [.C.   ,   0   ]  ->    ^h07;
               [.C.   ,   0   ]  ->    ^h08;
```

Figure 2. A 12-bit counter consisting of functional blocks and declaration text

The second equation

Terminal_Cnt = (Count == 3456)

causes the counter to reset tozero at count 3456; otherwise the counter would achieve a count of 4095.

Figure 3 shows the next lower-level drawing. This drawing shows that each of the four-bit counters is made up of four T-type flip-flop functional blocks named TFFR_D and connected together in a serial fashion. Figure 4 shows the internals of each functional block that represents a T-type flip-flop. The T-type flip-flop is created from the commonly found D-type flip-flop, with feedback connected through an XOR gate. This simple example shows how basic circuit elements can be implemented in functional blocks and then used at a next higher level, which in turn can be implemented into "larger" functional blocks, and so on.

Mixing Text And Graphics

Figure 2 also shows how PLDlinx can process drawings that describe the design description in both graphics and text form. That is, text and graphics are used to express different aspects of the design, depending on which form is the more suitable when entering the design by means of the schematic entry system. In the example 12-bit counter that resets at a count of 3456, it is relatively easy to enter the major portion of the design using functional blocks and discrete elements, but not trivial to enter the necessary reset gating to achieve a reset at 3456. The ability to mix text and graphics in the drawings, and have PLDlinx supply the pertinent equations, allows the use of a text entry to declare the full count value of the counter instead of having to enter it graphically on the schematic. This method of declaring the counter using a mixture of graphics and text greatly simplifies the task of entering the design.

All drawings to be processed by PLDlinx contain a declaration box that names the design, the target device, input pin names, output pin names, etc. Text that describes the actual design is also placed in the declaration box, or in an "include" box which is then declared in the declaration box. For example, Figure 2 contains the declaration box named DECBOX which identifies the design and defines the inputs and outputs of the counter, the target device type, and the name of the design. DECBOX also lists the include box named cnt14.inc so that PLDlinx includes the equations and test vectors contained in this box in the ABEL source file.

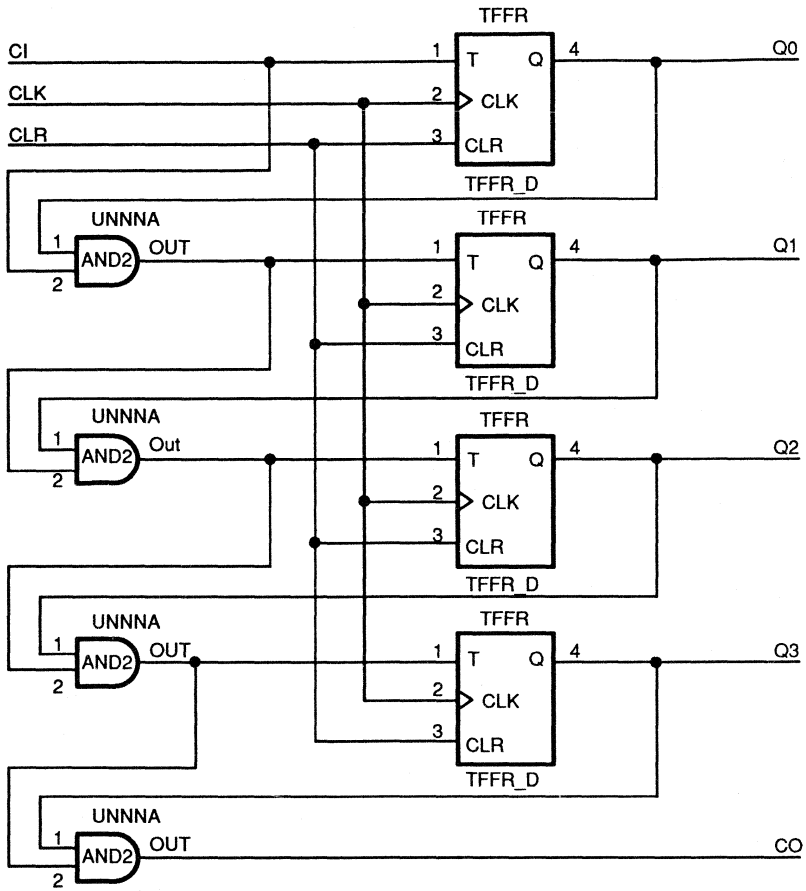


Figure 3. Each four-bit counter is made up of T-type flip-flops

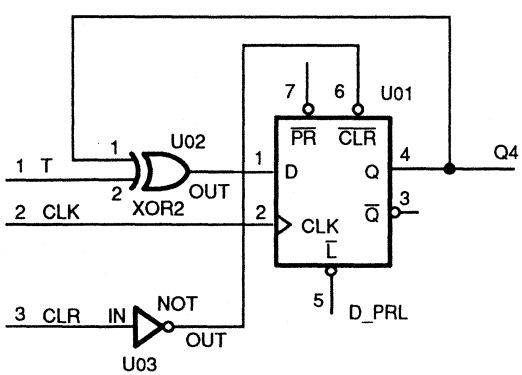


Figure 4. A D-type flip-flop performs T-type functions when the input is fed back through an XOR function

Partitioning Discrete Logic Into a PLD

PLDlinx can also be used to extract a portion of an existing schematic and place that logic in one or more PLDs. Figure 5 shows a 6809 microprocessor with control ROM, dynamic RAM, I/O decoding, and refresh logic. The non-shaded portion of the schematic shows the I/O and refresh logic which are to be placed in a single 16L8. By adding the following declaration box (Figure 6) to the schematic, the desired portion of the schematic is declared for processing by PLDlinx. The declaration box partitions the schematic by naming the target device and the input/output/bidirectional pin names and numbers. The declaration box also contains the name of a test vector file (decoder.vec) that will be used to test the design later in the simulation stage. When PLDlinx processes the 6809 schematic, it places only the declared portion of the drawing in the source file that will be passed to ABEL.

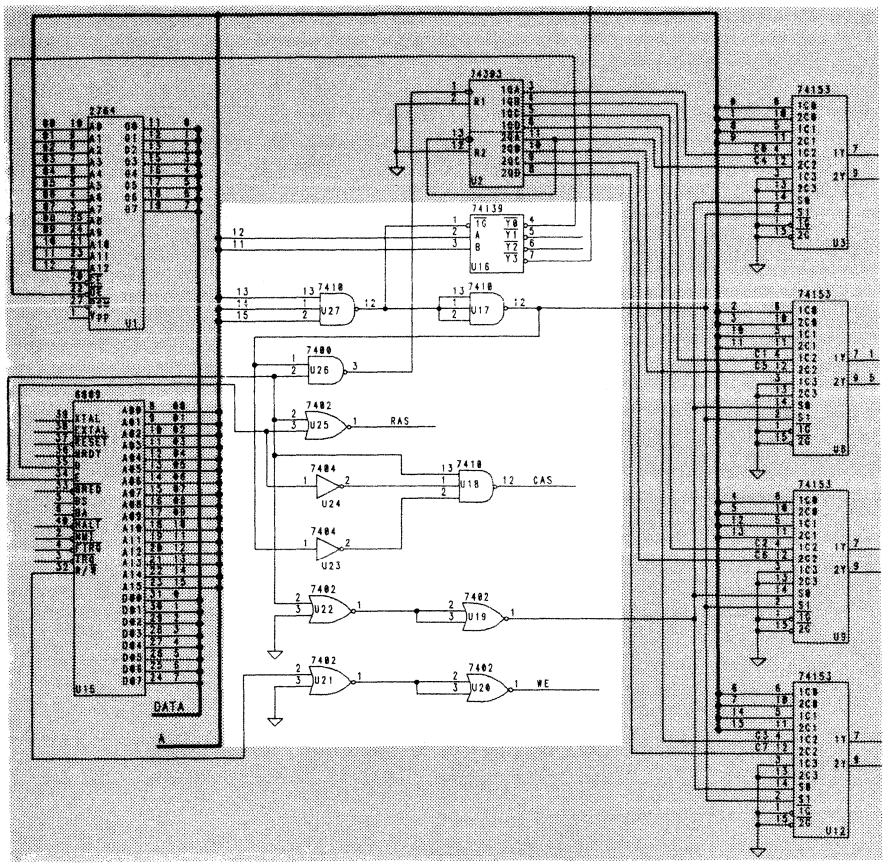


Figure 5. The unshaded I/O and refresh logic can be partitioned into a single PLD

DECBOX02

```
mod: decoder;
title; 6809 microprocessor system;
fusefile: u09;
dev:  p1618;
in:  [A15. . A10] = [1 . . 6];
in:  RW,E,Q = 7,8,9;
out: IO = 15;
out: ROM1 = 14;
out: COUNT = 12;
out: BE,CAS,RAS,WE = 13,17,18,19;
bid: DRAM = 16;
inc: decoder. vec;
```

U02

Figure 6. This declaration box defines that part of the overall schematic to be implemented in the 16L8 device

ABEL

ABEL (Advanced Boolean Expression Language) is a complete logic design tool for PAL devices, FPLAs, PROMs, FPLSs, etc., supporting over 200 different architectures, which translates to over 10,000 devices. ABEL incorporates a high-level design language and a set of programs that process logic designs to give correct and efficient designs that can be implemented in a wide variety of logic devices. Designs processed by ABEL are output in JEDEC file format, suitable for downloading to logic device programmers. ABEL will also read JEDEC files and convert them to design source files in its own format. This feature is useful in cases where a JEDEC file already exists for a design to be modified or built upon, and no ABEL source file exists.

How Designs Are Expressed

The ABEL design language allows the use of design structures that are familiar to designers; high-level equations, Boolean equations, state diagrams, and truth tables. The designer can choose any of these structures or combine them to describe a design. Macros and directives are also available for complex designs.

Design processing by ABEL includes source file syntax checking, automatic logic reduction, automatic design simulation, verification that a design can be implemented in a chosen device, and automatic generation of design documentation. The source file, written as an ASCII file, or generated by PLDlinx, can be edited by means of any text editor that produces ASCII files. The source file can also contain test vectors, or name a separate file of vectors to be "included", for simulation of the design. To perform simulation in a variety of programmable devices, ABEL constructs a software model of the PLD using the fuse information calculated from the reduced logic equations and detailed information about the specific PLD. If a design is too large for a single programmable device, you can use ABEL to split the design into multiple PLDs.

"COUNT = COUNT +1" Is Not a Boolean Equation

Figure 7 shows a portion of an ABEL source file that describes part of a design with Boolean equations. Figure 8 shows a portion of the same design expressed with a state machine, while Figure 9 shows a portion described with a truth table. The high-level equation feature of ABEL is shown in Figure 10, a design for a 16-bit counter, where the counter operation is defined by a single non-Boolean equation "count = count+1."

```
equations in muxadd

 Score    := Score $ Data $ CarryIn;

 CarryOut =  Data & Score # (Data # Score) & CarryIn;

 is_Ace   =  (Card == 1);

 Score.RE =  !Clr;
```

Figure 7. Expressing a portion of a design with Boolean equations

```
state_diagram in bjack Qstate
     State Clear:       Ace     := Low;
                        goto ShowHit;
     State ShowHit:     Ace     := Ace;
                        if (CardIn==Low) then AddCard else ShowHit;
     State AddCard:     Ace     := Ace;
                        if (is_Ace & !Ace) then Add_10 else Wait;
     State Add_10:      Ace     := High;
                        goto     Wait;
     State Wait:        Ace     := Ace;
                        if (CardOut==Low) then Test_17 else Wait;
     State Test_17:     Ace     := Ace;
                        if Hit then ShowHit else Test_22;
     State Test_22:     Ace    :=Ace;
                        case  !Bust        :ShowStand;
                        Bust & !Ace        :ShowBust;
                        Bust & Ace         :Sub_10;

                        endcase;
     State Sub_10:      Ace     := Low;
                        goto    Test_17;
     State ShowBust:    Ace     := Ace;
                        goto ShowBust;    "Loop until reset
     State ShowStand:   Ace     := Ace;
                        goto ShowStand;   "Loop until reset
```

Figure 8. Expressing a design with a state machine

```
" Digit separation macros

  binary            = 0;                "scratch variable
  clear    macro (a) {@const ?a=0};
  inc      macro (a) {@const ?a=?a+1;};

truth_table in binbcd
          ( Score -> [BCD2,BCD1])
  clear(binary);
  @repeat 32 {
          binary -> [binary/10,binary%10]; inc(binary);}

truth_table in binbcd
     ( Score -> [BCD2,BCD1])
        0   ->  [ 0  ,  0 ];
        1   ->  [ 0  ,  1 ];
        2   ->  [ 0  ,  2 ];
        3   ->  [ 0  ,  3 ];
        4   ->  [ 0  ,  4 ];
        5   ->  [ 0  ,  5 ];
        6   ->  [ 0  ,  6 ];
        7   ->  [ 0  ,  7 ];
        8   ->  [ 0  ,  8 ];
        9   ->  [ 0  ,  9 ];
        10  ->  [ 1  ,  0 ];
        11  ->  [ 1  ,  1 ];
        12  ->  [ 1  ,  2 ];
                  .
                  .
                  .
        29  ->  [ 2  ,  9 ];
        30  ->  [ 3  ,  0 ];
        31  ->  [ 3  ,  1 ];
```

Figure 9. Expressing a design with a truth table. The upper truth table uses macros and repeat directives to produce the "long-hand" truth table shown in lower portion of the illustration

```
module _cnt16eq

title '4-bit binary counter using equations
Data I/O Corp.  11 Jan 1989'

        cnt16eq device 'P16R8';

"Pins
        Clk,Clr,OE      pin 1, 2,11;
        Q3,Q2,Q1,Q0     pin 14,15,16,17;

"Sets
        Count     = [Q3..Q0];

"Constants for test vectors
        H,L,C,X,Z      = 1, 0, .C., .X., .Z.;

Equations
        Count := (Count + 1) & Clr;
```

Figure 10. An ABEL source file containing a high-level equation to express the operation of a counter

Automatic Polarity Selection

ABEL provides automatic polarity selection to accommodate devices having programmable polarity. When designing with one or more of these as the target device(s), such as the 22V10, ABEL will try to reduce the design using both polarities, and then use the polarity that results in the fewer number of product terms.

Automatic Fitting in XOR Devices

When designing with one or more XOR devices, ABEL will form new equations as necessary to accommodate these devices. For example, the equation !Q = !A $!B # !C # !D (where ! = not, $ = XOR, and # = OR) can be implemented in a 32VX10, but will not fit in a 20X8, since the latter device can only exclusive-OR two product terms with two product terms. When given a Boolean equation that contains more than the allowable XOR product terms, ABEL alters the equation to fit the target device. In this example, ABEL provides the equation !Q = A $ B & C & D (where & = AND), which can be implemented in the 20X8.

Viewing Internal Activity of the Design

ABEL also incorporates a "trace" feature that allows you to examine activity within the device. During simulation of the design, ABEL can be made to display a "graphic" representation of the logic levels occurring at various points within the macrocell of the chosen target device, as well as at external pins of the device. This visibility into the internal nodes of the device allows ABEL to serve as a macrocell debugger, displaying the logic levels within the macrocells for given input stimulus to the device. The display provided during this phase of ABEL operation is shown in Figure 11, which indicates the logic levels at the register inputs/outputs at specific times during operation of the design.

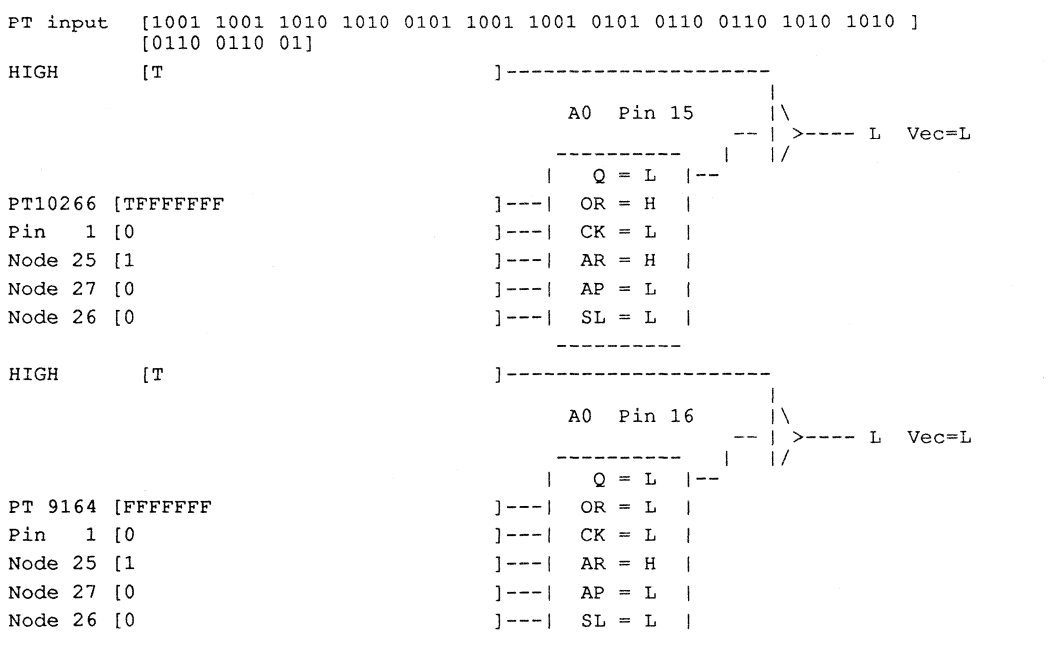


Figure 11. A built-in macrocell debugger provides visibility into the state of the nodes of each macrocell during design simulation (portion of a 29M16 shown)

The ABEL User Interface

The user interface for ABEL can be either command line oriented or menu driven if the features of Data I/O's Personal Silicon Foundry are used. The graphical interface provided by Personal Silicon Foundry allows you to work with various tools that comprise a complete design system. PLDlinx and various operating modules of the ABEL package are easily selected on the opening menu shown in Figure 12. PLDlinx is invoked by selecting "Schematic Translation" on the menu, while the different ABEL functions are chosen by means of the "Logic Synthesis" and "Text Editing" (a text editor to create and edit ABEL source files) selections.

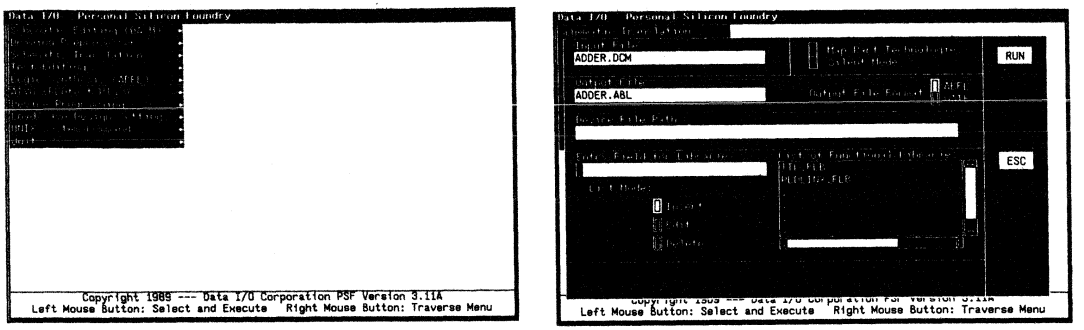


Figure 12. Personal Silicon Foundry Opening and Schematic Translation menus

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(800) 247-5700 or (206) 881-6444

6

FutureDesigner

FutureDesigner from Data I/O is an integrated design entry system which combines industry standard schematic capture, behavioral design entry, and logic synthesis capabilities. FutureDesigner allows the digital design engineer to use any combination of equations, truth tables or state diagrams to describe a design, independent of the target PLD or FPGA. Logic synthesis technology is used to automatically convert the high-level behavioral design description into the proper structural representation for multiple PLD and FPGA implementation.

FutureDesigner includes an interactive user interface, allowing entry errors to be caught immediately. Once a design is entered, it can be quickly verified, thus ensuring that design errors are caught up front. After design verification, reduction and factoring can be automatically performed to produce the most efficient design. Partitioning can also be employed to support multiple PLD or FPGA applications. As output, FutureDesigner produces design documentation and industry standard files for device implementation.

How A FutureDesigner Design Is Entered

Within FutureDesigner, designs can be entered either structurally with schematics, or behaviorally using equations. Structural descriptions can consist of any collection of generic gates and flip-flops, or any off-the-shelf part that has a Boolean equivalent, including most 7400 series TTL parts. Complex features like partitioning, layered text, and hierarchical design entry are all supported. Design Processing is performed automatically by tracing circuit paths and forming Boolean equations. Intelligent register configuration and utilization is also supported along with the generation of control logic terms.

FutureDesigner also allows behavioral design entry using a forms-based editor. The following entry forms are available:

Form	Purpose
Declarations	Enter set names, pin assignments, etc.
Equations	Aid entry of Boolean equations
Truth Table	Aid entry of truth tables
State Diagrams	Aid entry of state diagram
Simulation	Set parameters, perform simulation
Reduction	Set parameters, perform reduction
Factoring	Set parameters, perform factoring
Partitioning	Define partition, display partitioning data
Schematic	Set parameters, perform schematic generation
PLD Map	Set parameters, create JEDEC file

Each type of form has a predefined format and follows certain rules to make design entry easier, faster, and more accurate. For example, as an engineer enters an equation in the equations form, FutureDesigner checks each signal name against those entered on the declarations form. If a typing or assignment error occurs, an error message appears so the error can be corrected. For instance, entering an input on the output side of an equation would result in an error message, as would the use of an illegal operator or incorrect syntax.

The interactivity of the forms prevents design errors from accumulating in a design, only to be discovered later after much work. More than one form can be displayed on the screen at a time, and all forms are always "active"— that is, available to FutureDesigner for cross-checking of entries and collection of data for further processing.

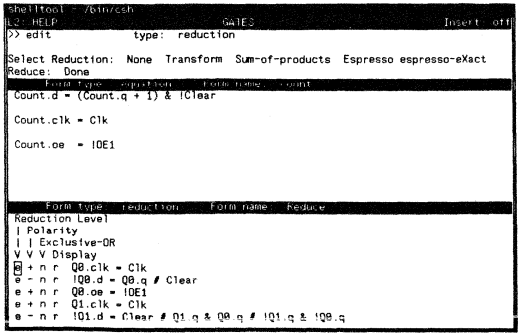

Figure 1. Split Screen Showing Original and Reduced Equations

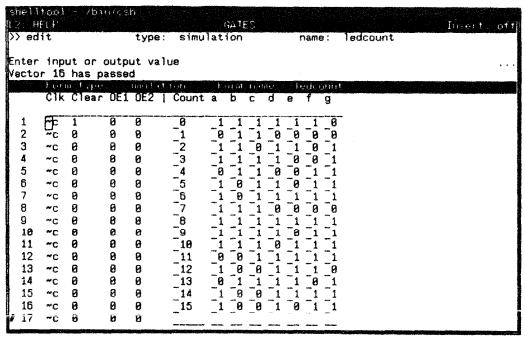

Figure 2. FutureDesigner Simulation In Progress

The top of Figure 1 shows an equation form with three equations that describe the COUNT function of the counter/LED decoder design example. The first equation, "Count.d = (Count.q +1) & !Clear", describes the count-up operation that takes place only when Clear is low. Note that a ".d" or ".q" has been appended to the set name. This notation allows the engineer to explicitly state whether the reference is to the D input or Q output of a D flip-flop. It also provides better control of multiple feedback paths.

The second equation, "Count.clk = Clk", describes the clocking operation, assigning the clock input of the flip-flops to the Clk signal. The third equation, "Count.or = !OE1", is for the output enable.

FutureDesigner Reduction

The lower half of Figure 1 shows reduced equations. Note that reduction parameters can be entered in the four columns to the left of each equation to be reduced.

FutureDesigner Simulation

A simulation form is shown in Figure 2 for the LED decoder portion of the design. FutureDesigner will fill in the output section of the form automatically. Once the input values are entered, the simulator goes to the design description forms, applies the inputs to the design, obtains output values, and inserts them into the simulation form. (Notice that in Figure 2 roughly half the simulation is complete, so half the values are filled in.) The engineer checks the values to make sure they are correct and can then make them "permanent," so they may be used for checking future iterations of the design.

Simulation takes place interactively and can be set to stop at the first error. An error message is displayed on the screen so corrections to the design can be made. In fact, because FutureDesigner can display more than one screen at a time, the engineer can simply call up the truth table for the decoder and make the appropriate change without leaving the simulation screen.

FutureDesigner Factoring

PLDs differ in the number of inputs to their AND and OR gates, the number of product terms, the existence of feedback paths and internal registers, the number of inputs and outputs, and many other items of interest to the engineer. FutureDesigner's factoring algorithm optimizes the design equations for the gate counts of the target device, creating intermediate equations and multiple levels of logic to do so. This is particularly useful for FPGAs and multi-level logic PLDs.

Figure 3 shows the counter equations before factoring; note that Q3.d requires five product terms. Figure 4 shows the factored equations for the counter outputs. During factoring, one intermediate equation, "cnt@0", was produced to reduce the number of product terms from five to four. If an internal signal or extra input is available, this intermediate equation can be used. Note also that the intermediate equation introduced one more stage or level into the design (indicated by the [3] next to the equation). In timing-critical designs, such a tradeoff may not work; in other designs, saving one product term may mean cost and/or power savings by allowing the use of a smaller PLD.

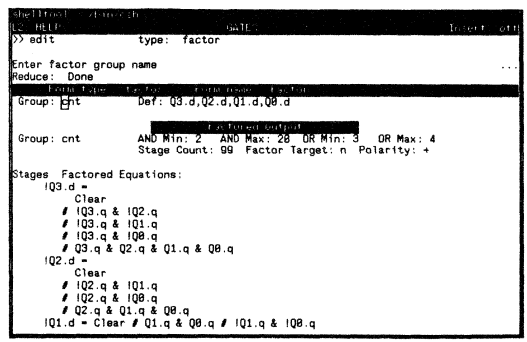

Figure 3. Screen Showing Original Equations

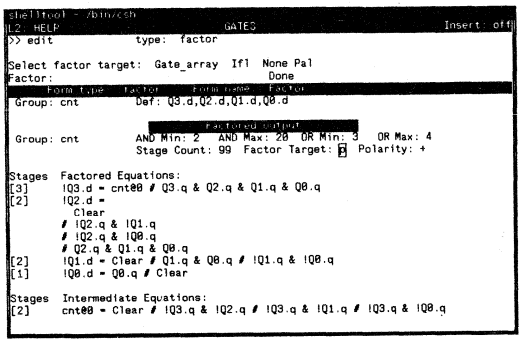

Figure 4. Screen Showing Factored Equations

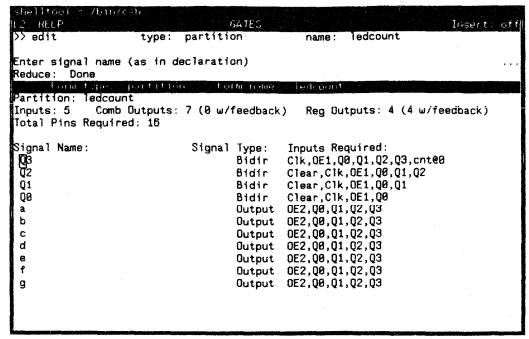

Figure 5. Partitioning Form Used to Partition Large Designs

FutureDesigner Partitioning

Manually partitioning a PLD design into more than one PLD can be a difficult task. The engineer must determine which inputs and outputs are common to equations to decide what makes a sensible partition. FutureDesigner's partitioning form provides assistance in this task. Figure 5 shows a partitioning form for the full LEDCOUNT design.

The engineer enters design outputs that he thinks are candidates for partitioning. FutureDesigner references the various declaration and design description forms and fills in the required inputs, the required number of combinational and registered outputs, and the total number of pins used by the partition. In this case, it is obvious that there is a natural partition between the count function that produces the Q0 through Q3 outputs, as well as the decoder function.

Pin and Device Assignment

To this point, the FutureDesigner design description has been completely "technology independent." In other words, the function of the design has been described without regard to the type of device used to implement it. This design could be part of a larger gate array or a complete program for a PLD. In this case, we have a partitioned design for two PLDs and must assign signals to the PLD pins. Figure 6 shows a device and pin assignment form.

SUMMARY

FutureDesigner is a powerful tool for designs using multiple PLDs or FPGAs. It supports mixed mode design entry, multi-level simulation, logic synthesis and optimization, partitioning and industry standard output formats. It is also completely compatible with Data I/O's entire suite of PLD tools, including ABEL™, PLDtest Plus™, MESA and UniSite™.

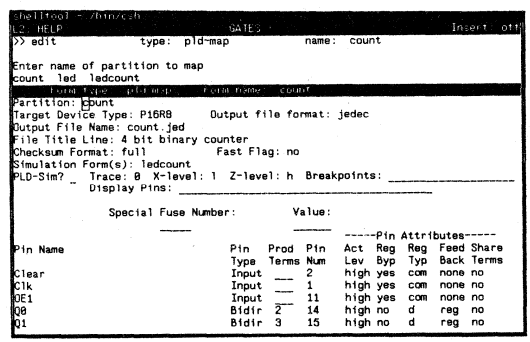

Figure 6. Device and Pin Assignment Form Used When a FutureDesigner Design is Programmed Into a PLD

For more information, contact:
Data I/O Corporation
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CUPL™ Universal Compiler for Programmable Logic

Logical Devices, Inc.

GENERAL

CUPL, the first high level universal development tool for programmable logic devices (PLDs), was initially developed by Assisted Technology, Inc., which was later bought out by P-CAD, Inc., in 1985. In July of 1988, Logical Devices, Inc., acquired the CUPL product line and immediately began updating and enhancing this widely used PLD compiler. In early 1989 Logical Devices released CUPL version 3.0, adding the following improvements:

- **A front end menu system** – A new menu-driven interface was added to the CUPL program to make the program easier to learn and use. The various phases of PLD design development can be stepped through without the need of memorizing command syntax. Menu selections are explained in an on-screen "Message Center," and a tutorial is provided that takes the user from design concept to custom chip.
- **Improved documentation** – The CUPL manual was redone in order to assist both new and experienced users of CUPL in accessing information effectively, and a separate CUPL User's Guide was created that covers the overall flow of data within the program, installation and customer support issues, and a history of CUPL and its improvements.
- **Improved syntax** – A MACRO command has been added which allows users to create their own macros that can define common logic constructs such as adders, decoders, counters, etc. These user-defined macros can be stored in a separate file and called into subsequent design files. A REPEAT command allows indexing of equations, which reduces many redundant statements to a simple indexed loop. CUPL's preprocessor provides string substitution, file inclusion, and conditional compilation.
- **Improved simulation** – CSIM, CUPL's simulation program, will correctly simulate a clock MUX and asynchronous architectures. Also, the simulation results can now be displayed in waveform output format, which is quite useful for design verification and documentation purposes.
- **Greater Device Support** – Device support is a key issue in the evaluation of a PLD development tool, and this is why CUPL users worldwide have responded so enthusiastically to the support and attention Logical Devices is giving to CUPL. As a major manufacturer of PLD programmers, we have been working closely with device manufacturers for years on device support issues, and this experience is put to good use for CUPL users, especially with all the new PLD offerings being introduced to the marketplace. In addition to the mainstream PLDs, CUPL supports the latest devices with advanced output macrocells such as the AMD PALCE29M16 and PALCE29MA16. CUPL supports all AMD PAL and PLS devices.
- **Compatibility to related CAE software** – CUPL can now be interfaced to schematic capture software such as P-CAD® (PC-CAPS), OrCAD/SDTIII™, Omation (Schema), Wintek (Hi-Wire), Racal-Redac (CADSTAR), CAD Software (PADS-logic), Protel-Schematic, and Phase-Three Logic (CAPFAST).
- **Platform availability** – In addition to standard PC, XT and AT machines, CUPL is also available for UNIX® and VAX®/VMS® installations, and runs on SUN®, HP®/Apollo® and DEC® workstations.
- **Customer Support** – The all-important area of technical support is expertly handled by Logical Devices. An Electronic Bulletin Board System is on-line 24 hours a day, 7 days a week to facilitate transfer of design files and retrieval of up-to-date information. Comprehensive update and maintenance programs are also available.

OVERVIEW OF DATA FLOW

Figure 1 gives a graphical overview of the flow of data within the CUPL program. Information about the devices supported by CUPL are kept in a device library file, CUPL.DL. First, you create a logic description source file (filename.pld) using the CUPL language to describe the logic you will assign to a PLD. The CUPL compiler generates files to download to a device programmer and files for documentation purposes, depending on the options specified in the source file.

You can also create a test specification file (filename.si) to verify the logic before programming the device. CSIM compares the expected values in the test file to the actual values in the absolute file (filename.abs) created by CUPL. When simulation is complete without any errors you can specify that the verified test vectors be appended to the download file generated by CUPL, for use with device programmers which handle test vectors. Note that CSIM is separate from the compiler, which means that you can run successive simulations on the same design file without having to re-compile each time. CSIM can optionally display the results of simulation in waveform output format.

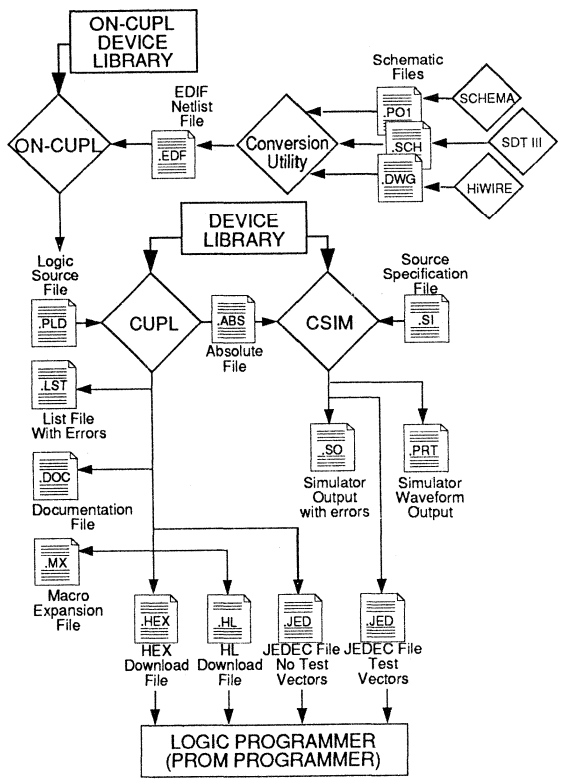


Figure 1

THE TEMPLATE FILE

TMPL.PLD is a template file provided with the CUPL program that you can use to build your logic source file. The structure of the template file is shown below.

```
Name        <filename>;
Partno      <for this function>;        (This section of the
Date        <date of last change>;       CUPL source file
Revision    <current rev. no.>;          contains keywords
Designer    <your name>;                 which identify the
Company     <your company>;              file for revision and
Assembly    <where PLD is used>;         archival purposes)
Location    <on PC board>;
FORMAT      <output option flags>;
DEVICE      <device mnemonic>;

/*****************************************************************/
/* This space is used for describing the function of the design  */
/* and allowable device types.  CUPL both promotes and provides  */
/* good documentation. Comments can be placed anywhere in the file*/
/*****************************************************************/
/*  Allowable Target Device Types:                               */
/*****************************************************************/

/**  Inputs  **/

Pin         =           ;     /* (This section is used for      */
Pin         =           ;     /* declaring pin numbers and      */
Pin         =           ;     /* assigning them variable names. */
Pin         =           ;     /*                                */
Pin         =           ;     /* The exclamation point (!) is   */
Pin         =           ;     /* used to define asserted low    */
Pin         =           ;     /* input and output signals, so   */
Pin         =           ;     /* with CUPL you can always write */
Pin         =           ;     /* equations in positive logic    */
Pin         =           ;     /* regardless of the polarity     */
Pin         =           ;     /* of the signals entering the    */
Pin         =           ;     /* device...                      */

/**  Outputs  **/

Pin         =           ;     /* ...or whether there are        */
Pin         =           ;     /* inverting buffers at the       */
Pin         =           ;     /* outputs.                       */
Pin         =           ;     /*                                */
Pin         =           ;     /*  When you negate an entire     */
Pin         =           ;     /*  expression, CUPL automati-    */
Pin         =           ;     /*  cally performs a DeMorgan     */
Pin         =           ;     /*  expansion.)                   */

/** Declarations and Intermediate Variable Definitions **/

(This section of the source file is used for making declarations
such as BIT FIELD and NODE declarations, and for writing inter-
mediate variable equations.  Bit Field statements allow you to
declare a group of bits to be equal to a single symbolic name which
can then be used in equations.  Node statements are used to declare
a variable name for buried state registers and functions.)

/**  Logic Equations  **/

(This section is for logic equations, which can be written in
state machine, high-level equation (boolean), and truth table
format.  The form for logic equations is as follows:
                    [!] var[.ext] = exp;
where var is a single variable or list of indexed or non-indexed
variables, ext is an optional extension to assign a function to
the major nodes inside a progammable device, and exp is an expression
consisting of variable names specified elsewhere in the source file.
The [!] symbol is the complement operator, which can be used on either
side of the assignment operator (=).
```

EXAMPLES

This example of a 10-state decade counter shows the power of the MACRO and REPEAT capability. By specifying an option flag when compiling this source file, CUPL will automatically generate the equivalent source file (filename.mx) without the MACRO and REPEAT functions (see Figure 2), which could be used for debugging purposes.

```
Name        COUNTER10;
Partno      CA0018;
Date        05/24/89;
Revision    01;
Designer    Baird;
Company     Logical Devices, Inc.;
Assembly    None;
Location    None;
Device      p16r4;
/*****************************************************************/
/*                                                               */
/* Decade Counter                                                */
/*                                                               */
/* This is a 10-state up/down decade counter with synchronous    */
/* clear capability.  An asynchronous ripple carry output is     */
/* provided for cascading multiple devices.  CUPL state machine  */
/* syntax is used.                                               */
/*****************************************************************/
/* Allowable Target Device Types :  PAL16RP4                     */
/*****************************************************************/
/**  Inputs  **/

pin 1     = clk;              /* Counter clock                   */
pin 2     = clr;              /* Counter clear input             */
pin 3     = dir;              /* Counter direction input         */
pin 11    = !oe;              /* Register output enable          */
/**  Outputs  **/

pin [14..17] = ![Q3..0];      /* Counter outputs                 */
pin 18 = !carry;              /* Ripple carry out                */

/** Macro Definition **/
$MACRO COUNTER num statebit up down clear
FIELD COUNT = [statebit{0}..{log2(num) - 1}];
sequence COUNT {
$REPEAT i = [{0}..{num-1}]
present 'b'{i}    if up       next 'b'{(i+1)%num};
                  if down     next 'b'{(num-1+i)%num};
                  if clear    next 'b'{0};
$REPEND
                              out carry;
}
$MEND

/** Declarations and Intermediate Variable Definitions **/
field mode = [clr,dir];       /* declare mode control field */
up = mode:0;                  /* define count up mode */
down = mode:1;                /* define count down mode */
clear = mode:[2..3];          /* define count clear mode */

/** Logic Equations **/

/* free running counter */
COUNTER(10, Q, up, down, clear);
```

Figure 1. Counter Using MACRO and REPEAT

```
Name        COUNTER10;
Partno      CA0018;
Date        05/24/89;
Revision    01;
Designer    Baird;
Company     Logical Devices, Inc.;
Assembly    None;
Location    None;
Device      p16r4;

/*****************************************************************/
/*                                                               */
/* Decade Counter                                                */
/*                                                               */
/* This is a 10-state up/down decade counter with synchronous    */
/* clear capability.  An asynchronous ripple carry output is     */
/* provided for cascading multiple devices.  CUPL state machine  */
/* syntax is used.                                               */
/*****************************************************************/
/* Allowable Target Device Types :  PAL16RP4                     */
/*****************************************************************/

/**  Inputs  **/

pin 1       = clk;              /* Counter clock                 */
pin 2       = clr;              /* Counter clear input           */
pin 3       = dir;              /* Counter direction input       */
pin 11      = !oe;              /* Register output enable        */

/**  Outputs  **/

pin [14..17] = ![Q3..0];        /* Counter outputs               */
pin 18 = !carry;                /* Ripple carry out              */


/** Macro Definition **/
/** Declarations and Intermediate Variable Definitions **/
field mode = [clr,dir];         /* declare mode control field */
up = mode:0;                    /* define count up mode */
down = mode:1;                  /* define count down mode */
clear = mode:[2..3];            /* define count clear mode */

/** Logic Equations **/

/* free running counter */
FIELD COUNT = [Q0..3];

sequence COUNT {

present 'b'0    if up      next 'b'1;
                   if down    next 'b'1001;
                   if clear   next 'b'0;

present 'b'1    if up      next 'b'10;
                   if down    next 'b'0;
                   if clear   next 'b'0;

present 'b'10    if up      next 'b'11;
                    if down    next 'b'1;
                    if clear   next 'b'0;
```

Figure 2. Equivalent File without MACRO and REPEAT

```
present 'b'11    if up      next 'b'100;
                   if down    next 'b'10;
                   if clear   next 'b'0;

present 'b'100    if up      next 'b'101;
                   if down    next 'b'11;
                   if clear   next 'b'0;

present 'b'101    if up      next 'b'110;
                   if down    next 'b'100;
                   if clear   next 'b'0;

present 'b'110    if up      next 'b'111;
                   if down    next 'b'101;
                   if clear   next 'b'0;

present 'b'111    if up      next 'b'1000;
                   if down    next 'b'110;
                   if clear   next 'b'0;

present 'b'1000    if up      next 'b'1001;
                   if down    next 'b'111;
                   if clear   next 'b'0;

present 'b'1001    if up      next 'b'0;
                   if down    next 'b'1000;
                   if clear   next 'b'0;
                              out carry;
}
```

Figure 2. Equivalent File without MACRO and REPEAT (continued)

HIERARCHICAL DESIGN

As you can see in the above examples, one line of code in the PLD file {COUNTER (10,Q,up,down,clear)} can implement a 10-state counter. You can build your own macro library file (macrolib.m) of basic circuit functions (counters, adders, multiplexers, decoders, etc.) and use them as building blocks for higher-level designs. For example, in the above count10.pld file the MACRO "COUNTER" could be stored in a separate file and then called into the .pld file by using the $INCLUDE command.

Example

```
$INCLUDE macrolib.m
COUNTER (10, Q, up, down, clear);
```

will cause CUPL to open the macrolib.m file and extract the COUNTER macro specification into the .pld file. Using the $INCLUDE command gives you access to all the macro functions defined in the specified macro library.

Documentation Output Files

The documentation output file (filename.DOC) provides the fully expanded product terms for both intermediate and output pin variables, and a fuse plot and chip diagram. A JEDEC file is created for downloading to a device programmer.

SIMULATION

An important part of the PLD design process is verifying your logic design before programming the chip. CSIM, the CUPL simulator, is a powerful tool for PLD design verification.

The input to CSIM (filename.si) is a file which contains an order statement and test vectors.

The order statement lists the input and output variables that you want to simulate. The % sign is used for formatting purposes. It inserts spaces between the variable name columns.

The vectors section is used to assign input values to each of the input variables and an expected value to each of the output variables. You can let CSIM determine the output value by assigning a "*" to the output variable.

After running CSIM a simulation output file (filename.so) will be created which shows the results of the simulation. The simulation results can be displayed in both table and waveform output format.

A hardcopy of the waveform display can be created, which is useful for documentation purposes.

```
Device      p16rp4;
Name        COUNTER10;
Partno      CA0018;
Date        05/24/89;
Revision    01;
Designer    Baird;
Company     Logical Devices, Inc.;
Assembly    None;
Location    None;
Device      p16r4;

/*****************************************************************/
/*                                                               */
/* Decade Counter                                                */
/*                                                               */
/*****************************************************************/

ORDER:clk,clr,dir,!oe,%2,Q3..0,%1,carry;

VECTORS:
      C 100  LLLL L          /* synchronous clear to state 0   */
      C 000  LLLH L          /* count up to state 1            */
      C 000  LLHL L          /* count up to state 2            */
      C 000  LLHH L          /* count up to state 3            */
      C 000  LHLL L          /* count up to state 4            */
      C 000  LHLH L          /* count up to state 5            */
      C 000  LHHL L          /* count up to state 6            */
      C 000  LHHH L          /* count up to state 7            */
      C 000  HLLL L          /* count up to state 8            */
      C 000  HLLH H          /* count up to state 9 - carry    */
      C 000  LLLL L          /* count up to state 0            */
      C 010  HLLH H          /* count down to state 9 - carry  */
      C 010  HLLL L          /* count down to state 8          */
      C 010  LHHH L          /* count down to state 7          */
      C 010  LHHL L          /* count down to state 6          */
      C 010  LHLH L          /* count down to state 5          */
      C 010  LHLL L          /* count down to state 4          */
      C 010  LLHH L          /* count down to state 3          */
      C 010  LLHL L          /* count down to state 2          */
      C 010  LLLH L          /* count down to state 1          */
      C 010  LLLL L          /* count down to state 0          */
      C 001  ZZZZ L          /* test tri-state                 */
      C 000  LLHL L          /* count up to state 2            */
      C 100  LLLL L          /* synchronous clear to state 0   */
```

Figure 3. Simulation

Logic Minimization

CUPL supports five levels of logic minimization–"NO-MIN," "Quick-Min," Quine-McCluskey, PRESTO, and enhanced Espresso–selectable by the designer on a pin-by-pin basis. This flexibility can be very important since it is sometimes desireable to maintain redundant logic terms in a design.

New Product Developments

Logical Devices is developing new products to complement the CUPL compiler. These include TestPLA, an automatic test vector generator, PLAdvisor, a device selection program that utilizes user-defined criteria, and PLPartition, which will partition a design too large for a single PLD.

For more information, contact:

Logical Devices, Inc.
(800) 331-7766 or (305) 491-7405

THE PLD COMPILER

With a Universal System...

The complexity and number of PLDs is constantly increasing and they are becoming increasingly easy to use as a result of numerous special functions. Only truly manufacturer-independent CAE software, such as LOG/iC, can support all of this. By regularly updating its PLD library, ISDATA® makes sure that you are always right up with the latest developments. The LOG/iC PLD compiler provides you with all the advantages of logic synthesis, i.e., circuit definitions independent of the final realization and automatic circuit generation. It is therefore easier to switch between different types and families of circuits.

...Optimal Solutions

The two PLD compiler optimizers make the best of your chips. This saves you money, space on the board and makes your circuits more reliable.

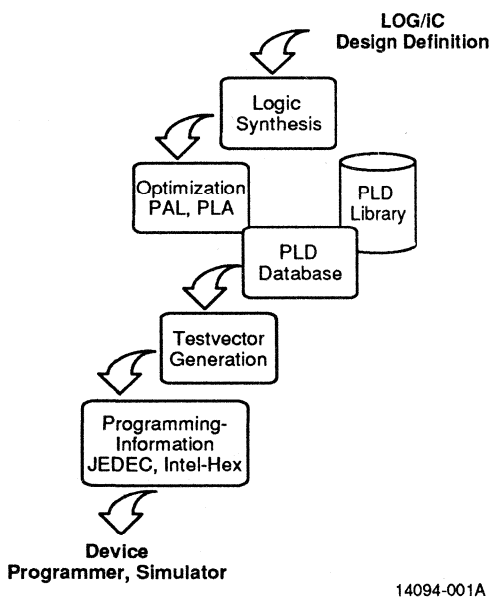


Figure 1. LOG/iC Design Definition

LOG/iC makes use of ISDATA's own algorithm *FACT* for PAL structures and the *ESPRESSO* algorithm for PLA structures. LOG/iC automatically computes the logical true and inverted of every function-we call it "*Auto de Morgan.*"

...and Design Safety

Of course, the automatic generation of *test vectors* belongs to the standards. A product term coverage of 100% has been achieved. The test vectors are automatically inserted into the programming file. LOG/iC produces current data formats, such as the JEDEC format or the Intel HEX format (for PROMs).

You Need Know Nothing More about PLDs than their Future Functions...

You design the circuit as a whole, regardless of whether this design is to be implemented in one or more devices. Existing designs can be incorporated into new designs. Every functional block can be described with the most suitable syntax. Designs which exist as circuit diagrams can easily be input in the LOG/iC system via the option "Schematic Macro Library (SML)." At this stage it is not necessary to commit yourself to a particular PLD type.

LOG/iC makes every step of the design transparent. The "*Optimization Summary,*" for example, tells you how many p terms each function needs. LOG/iC automatically configures the PLD's macro cells. You can, of course, also easily define *Preset, Output Enable, Clock* and other functions yourself.

After optimization you have to decide on one or more ICs. It is easy to partition the complete design onto suitable, individual ICs. The PLD Data Base, an option to the program, automatically suggests a selection of suitable chips. It is also a practical electronic reference "book."

PLDs are also easy to program. You can, for example, use menus to set all the interface parameters of your device programmer. You don't have to worry about *extensions* and *file names* - the interactive program offers you elegant support. LOG/iC automatically generates the test vectors for testing the circuit on the programmer. You can, of course, add your own test vectors or get test vector files from the Functional Verifier. By the way, with this interesting option you can already "breathe life" into your circuit before even having decided on which implementation to use.

Publication #	*Rev.*	*Amendment*	*Issue Date*
14094	A	/0	1/90

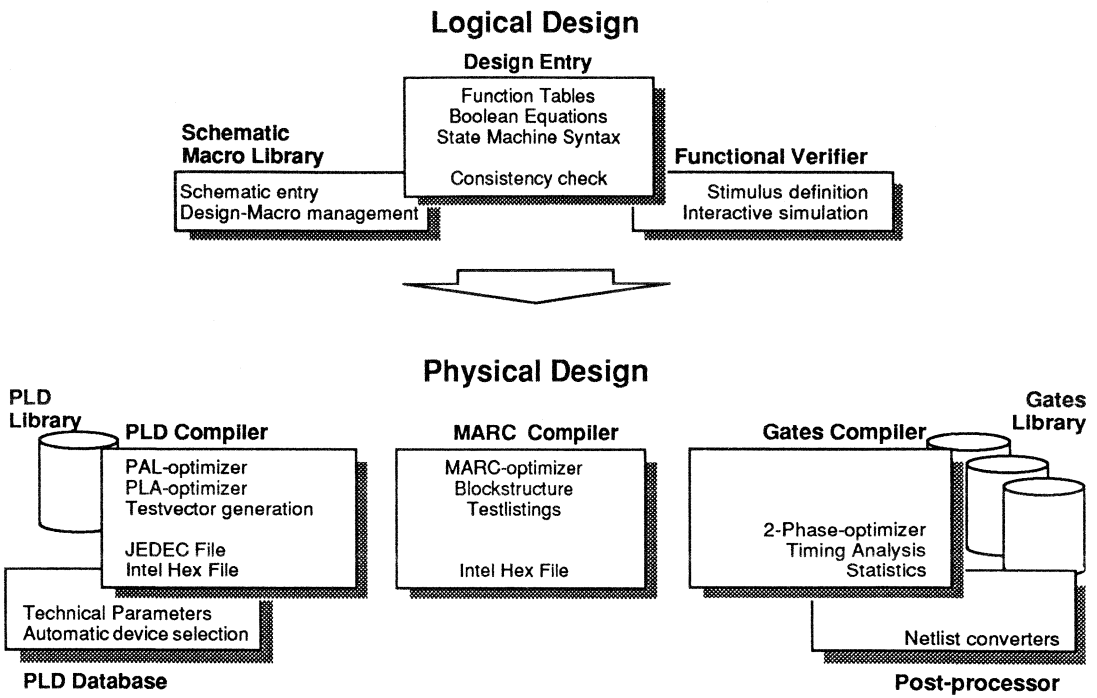


Figure 2: The LOG/iC Tool Box
LOG/iC's tool concept separates the design process into logical design and physical design.

Process of Development

LOG/iC is a universal design system for digital logic. It puts the emphasis on the logical description of the circuit rather than a specific device. LOG/iC allows you to run sophisticated designs without tying you down to a specific IC.

Circuit descriptions, as well as syntax and consistency checks, can be run without transforming the design into a specific device. This applies also to the circuit simulation performed by the "Functional Verifier," which verifies the logical functioning of the design. There is a specific optimization for each particular device family. The designer's choice of a device is based upon the results of this optimization. Additional support is offered by the "PLD Data Base" that helps select the best-suited type in case of a PLD implementation.

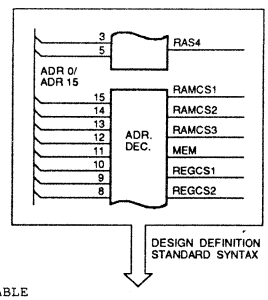
The described procedure allows the user to enter and optimize large designs even if they can't be implemented in one single IC. After optimization, LOG/iC helps to select the best-suited circuit technology and IC type, thus enabling the designer to make best use of the benefits of modern ICs.

Circuit Definition

LOG/iC offers specific description aids for various designs problems. Its standard syntax preferably describes combinatorial circuits, but it is also possible to describe sequential circuits by means of Boolean equations. The FSM (Finite State Machine) syntax has been created to make the definition of state machines more convenient. Special interface options enable circuits from third-party systems to be fed into LOG/iC in the form of circuit schematics. Together with LOG/iC, any text editor can be used to edit design files.

Standard Syntax

The basic elements of the standard syntax are Boolean equations and function tables. The format of the equations corresponds to the common standard. All common operators can be used. The equations can be nested in any order. They will automatically be converted into a Sum-of-Products (SOP) format. String substitutions considerably reduce the time spent on editing, and allow the design to be more clearly laid out.




```
*FUNCTION TABLE
$  (ADR[15..0]) :MEM, (RAMCS [1..3]), (REGCS [1..4]);
 ;-------------------------------------------------------
 0000H . . 3FFFH: 1 ,  100 , 0000 ; MEMORY NR.1
 4000H . . 7FFFH: 1 ,  010 , 0000 ; MEMORY NR.2
 8000H . . BFFFH: 1 ,  001 , 0000 ; MEMORY NR.3
     C037H      : 0 ,   -  , 1000 ; S-REGISTER
     CC03H      : 0 ,   -  , 0100 ; F-REGISTER
     D0F7H      : 0 ,   -  , 0010 ; G-REGISTER
     EFF3H      : 0 ,   -  , 0001 ; L-REGISTER
REST            : 0 ,   -  , 0000 ; NOT SELECTED

*END
```

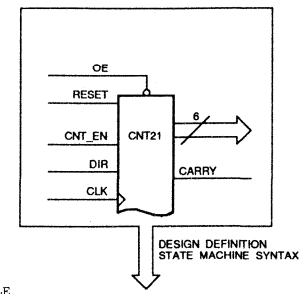
14094-003A

Design Definition Standard Syntax

Function tables, basically the most concise way of formatting, can be made even more concise through numbers in arbitrary numeric systems, which can then be merged (hex, decimal, octal, binary). It is possible to partition logical data into a subset of different function tables. In addition, equations and tables can be merged in order to define a circuit. The option "Rest-Definition" and the use of number fields make the function tables particularly concise. As a result, address decoders especially can be conveniently described.

FSM-Syntax

The FSM-syntax enables you to give a functional description of a synchronous state machine. LOG/iC supports the design of any state machine such as MEALY or MOORE or combinations of the two. Any diagram description can be used as a concept, e.g,. flow diagrams or bubble diagrams. These diagrams can easily be transformed into LOG/iC syntax. The basic entry syntax is close to hardware. A number of syntax aids, however, enable circuits to be defined on a high level. Thus you can define input and output vectors and make the design files more understandable by means of the macro-definition. The "range notation" also applies to state definitions so that counters and similar circuits can be conveniently defined. It is possible to select with a single statement the relevant variables out of a whole set of input variables.




```
* FLOW TABLE
;-------------------------------------------------------
S [1..21], 'CLEAR', 'CAR_0', F1; SYNCHRONOUS RESET

;COUNT UP
S [1..20], 'UP'   , 'CAR_0', F[2..21];
      S21, 'UP'   , 'CAR_1', F1;

;COUNT DOWN
S [21..2], 'DOWN' , 'CAR_0', F[20..1];
      S 1, 'DOWN' , 'CAR_1', F 21;
;-------------------------------------------------------
*STATE ASSIGNMENT
 BINARY
*END
```

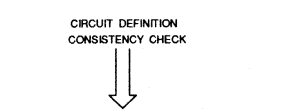
14094-004A

Design Definition State Machine Syntax

Consistency Check

In addition to the usual syntax check, LOG/iC verifies the logical consistency. At a very early stage of the design flow, inconsistencies are pointed out to the designer. The Consistency Checker reports its results in the form of information, warnings, and errors indicating the line where they occur.

Incompletely specified branches of a state or incomplete function tables are indicated as a warning. Ambiguous outputs of a table, on the other hand, as well as contradictory branches and outputs of a state machine are indicated as an error.The LOG/iC consistency check detects even complex error conditions, such as states that can't possibly be reached by the running circuit.



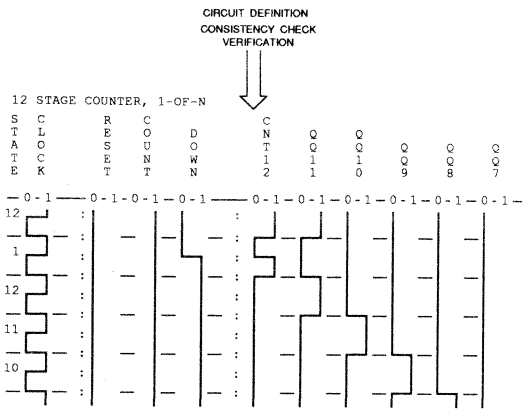

```
**  WARNING  ** STATE    1 INCOMPLETELY DEFINED
**  WARNING  ** STATE    4 INCOMPLETELY DEFINED
****  INFO ****   NO EXIT FROM STATE  4
****  INFO **** STATE    3 CANNOT BE REACHED FROM INITIAL STATE
****  INFO **** STATE    4 CANNOT BE REACHED FROM INITIAL STATE

INCONSISTENT NEXT-STATE ENTRIES IN LINE      1 AND LINE   2

INCONSISTENT CONTROL-VECTORS IN LINE      7 AND LINE   8

*** LOG/iC ERROR TERMINATION: CONSISTENCY-CHECK ***
```

14094-005A

Consistency Check

Verification

The option "Functional Verifier" is a simulator that applies stimuli to the circuit definition in order to verify its correct logical behavior. This simulation is not influenced by any devices and it provides a quick verification of the design definition. Its operation, similar to a Logic State Analyzer, is screen-based and therefore easy to run. The results of such a simulation are indicated in the form of waveforms. Inputs can be changed online in the interactive mode and the reaction of the simulated circuit will be indicated immediately.

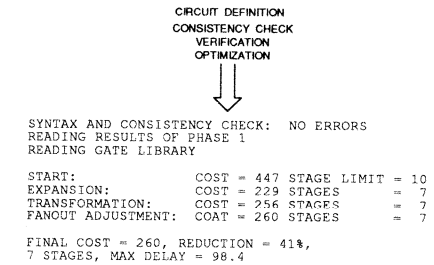


14094-006A

Verification

Optimization

The data input and consistency checks are completely independent of the device. Optimization, however, is tailored to each specific family of devices. Even during optimization, there is still no need to specify the type. PAL device designs are optimized by means of an exact procedure, called the "FACT Algorithm." PLA circuits, on the other hand, are optimized by means of a "bundle"-minimization. Multi-level gate logic for gate and cell arrays is optimized through a special procedure. For ROM-based controllers, the optimizer computes various possible solutions.



14094-007A

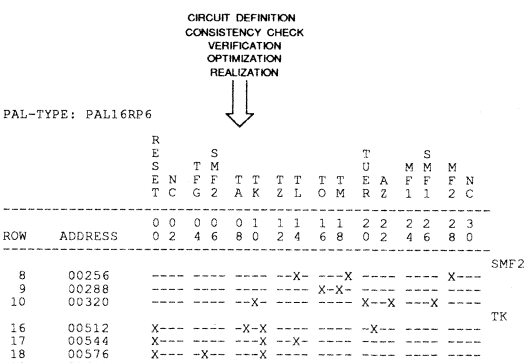
Optimization

By offering a choice of optimizers, LOG/iC enables the user to optimize a defined circuit for very different realizations in a short period of time. The optimization reports produced in this way are tailored to specific device families. They are decision aids for the designer when he wants to realize a particular circuit.

All the optimizers are described in more detail on their respective data sheets.

Realization

In the case of a PLD design, LOG/iC fits the optimized data into the device structure of a particular device and produces the programming and test data for the IC. The structural data are taken from the PLD library and the results are transferred to the programmer in the form of a JEDEC File.



14094-008A

Realization

Module package "Gates" produces the net lists of the design in various data formats so that it can be transferred to different CAE systems.

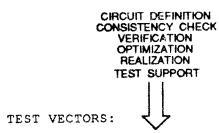
If a design is to be realized as a ROM-based controller, the designer chooses one of the seven solutions offered by the optimizer. The necessary programming and structural data are then produced. LOG/iC provides the programming data for PROMs in the Intel-Hex format.

In all module packages, partial designs can be combined in order to be realized in one circuit. But at the same time, LOG/iC also enables the user to partition a design into various devices.

Test Aid

LOG/iC is an effective tool for the design of circuits, but it also offers many test aids.

For PAL devices, module package 2 automatically generates test vectors for a product-term-oriented test on the programmer. LOG/iC guarantees 100% product term coverage. Module package 1 supports input of user-defined test vectors and includes them into the JEDEC File.




```
1: ;
1: ;          C          R
1: ;          A          E
1: ; C QQ QQR    O G G S          V
1: ; LXQQ QQR     EXN NXEM LRRL MMXC
1: ; K112 34YB AN2D D3TO OOUU UM4C
1: ;-------------------------------
1:   PN11 11NN NNNN PNNN NNNN NNNN ;
2:   01HH HHN0 101N 011H HNNH NL1N ;
3:   C1HH HHH0 101N C11N NNNN NN1N ;  1
4:   PN00 01NN NNNN PNNN NNNN NNNN ;
5:   00LL LHN1 000N 001L LHNN HN0N ;
6:   C0LL LLH1 000N C01N NNNN NN0N ;  2
```

14094-009A

Test Support

Gate array circuits undergo a timing analysis after optimization. The results are extensively documented and contain a critical-path analysis. In addition to the microprogram listing, LOG/iC generates additional test lists for MARCs.

Example of PAL32VX10 Support

The following example demonstrates the ability to use the T-type flip-flop in the PAL32VX10 directly though LOG/iC software. LOG/iC automatically emulates the T-type flip-flop as needed through specific programming of the XOR terms in the PAL32VX10. The following file fully describes a modulus-93 counter.

```
*IDENTIFICATION
 BIT STREAM COUNTER FOR 93 BITS (VER.2.1_T-FLIPFLOP)
 GUENTER BIEHL
 ISDATA KARLSRUHE, TEL. 0721 693092
*DECLARATIONS
 X-VARIABLES = 3
 Y-VARIABLES = 1
 Z-VARIABLES = 7
*X-NAMES
 RESET = 1, DOWN=2, COUNT=3;
*Y-NAMES
 CARRY = 1;
*Z-NAMES
 QQ[6..0] = [7..1];
*RUN-CONTROL
 LISTING = PINOUT, FUSE-PLOT, EQUATIONS;
 PROGFORMAT =JEDEC;
*Z-VALUES
 S[1..93] = [0..92];
*FLOW-TABLE
;COUNTER WITH 93 STATES AND CARRY SIGNAL
 S[1..93], X1--, Y0, F1;          RESET CONDITION
 S[1..93], X00-, Y0, F[1..93];    HOLD
 S[1..92], X010, Y0, F[2..93];    COUNT UP
 S93 ,     X010, Y1, F1;          CARRY
 S[2..93], X011, Y0, F[1..92];    COUNT DOWN
 S1 ,      X011, Y1, F93;         CARRY
*STATE-ASSIGNMENT
 Z-VALUES;
*PAL
 TYPE=PAL32VX10;
*PINS
 RESET=3, COUNT=4, DOWN=5,
 CARRY=22, QQ[0..6]=[15..21];
*FLI
 T-FLIPFLOP
*END
```

14094-0010A

PAL32VX10 Support

LOG/iC FUNCTIONAL VERIFIER

- Design verification in the logical design phase
- Logical simulation independent of the realization
- High-level language supported generation of stimulus files
- Automatic generation of functional test vectors for the use in the testing field
- Interactive simulation directly on the screen
- Simple, menu-controlled operation
- Circuit development and simulation on the same system with the same user interface
- Verifies synchronous and asynchronous logic

Realization-Independent Functional Verification

Conventional simulators simulate the function and, at the same time, the detailed timing behavior of the circuit. However, we know from experience that a large number of the errors made during development of a circuit are of purely logical nature. They can be discovered much faster and more easily using a simulation which is directly based on the functional circuit description.

The LOG/iC Functional Verifier operates on this principle. It allows the correct *logical behavior* of a circuit to be verified before the realization has been compiled. Logical errors are therefore discovered in an early stage of development and then it is only a short step to eliminating these errors. You work with this "early warning system" *like with a logic analyzer.*

Clear and Concise Documentation

The contents of the trace buffer or the parts thereof can be displayed on the screen (on PCs with EGA board, with up to 43 lines):

- as waveforms
- or as binary numbers.

You can print out the following documents:

- a protocol of the whole simulation,
- the list of test vectors,
- or any part of the contents of the trace buffer in varying degrees of detail and print format.

Interactive- or Program-Controlled Simulation

The LOG/iC Functional Verifier consists of three different parts:

- Design Compiler
- Stimulus Compiler
- Interactive Simulator

The Design Compiler analyzes the LOG/iC design definition and from this creates the *simulation model.* The results of the compilation are stored in intermediate files so that it is necessary to run the compiler only once when generating or changing the design entry.

In addition to the *interactive specification* of stimulus vectors, the LOG/iC Functional Verifier allows program-*controlled generation* of stimuli. A PASCAL-like high-level language supports this. The Stimulus Compiler checks this test program and compiles it into a binary form which can be read by the Interactive Simulator. This allows even large stimulus files to be quickly and easily generated. You can interrupt the program at any time with the command "PAUSE" and continue interactively. The results of the simulation run recorded in a circular trace buffer.

Technical Data

- Contents of trace buffer: 1024 events
- Number of I/O variables: max. 256 each (PC: 128)
- Supported special functions: Reset, Preset, Output Enable, etc.
- Number of iterations: 99, for simulation of asynchronous state machines

LOG/iC PLD DATA BASE

- Information about almost all available ROMs and PLD devices
- Structural specifications, parameters, extracts from the logic structure and pinouts are clearly displayed
- Automatic device selection for a given design
- Searches according to specified criteria. Search criteria include all device data. Easy to find second sources
- Menu-controlled operation
- Ideal electronic reference "book"

Detailed Information about Every Device

The rich selection of PLD devices is, of course, very welcome. The electronics developer is overwhelmed by the enormous range of choice of enticing technical possibilities. This multitude even makes it difficult for PLD insiders and old hands to find the most suitable device with respect to logical structure, electrical data, packaging, etc. for a particular circuit.

The PLD Data Base offers the designer valuable and easy-to-use support for this purpose. The electronic reference "book" saves you from having to leaf through innumerous data books. For every supported PLD device, the PLD Data Base displays the *structure data, physical parameters, manufacturer and technology* on the screen. It also displays an *extract of the fuse plot*, including the macro cell, as well as the *pinout*.

The PLD Data Base is an option to the CAE system LOG/iC. It adds a user interface and a compiler interface to the standard PLD library of the LOG/iC PAL® and PLD compilers. The user then has access to the greatly extended library which, in addition to the structure data, contains the technical parameters and technology of almost all available PLDs.

Automatic Device Selection

If the PLD Data Base is operated with the LOG/iC PLD optimizer, then the values necessary for the realization of the circuit, such as optimization results, pin number, number of bidirectional signals, reset or clock function, are automatically passed on to the data base. The data base then selects – based on the optimization results of the compiler – the most suitable devices and displays a list of all devices which might come in question. If you specify additional properties interactively, such as maximum supply current or switching frequency, then the selection is limited even more. In this way the device most suitable with respect to both its logical structure and its physical values is quickly found.

This automatic search for the optimal devices makes the PLD Data Base a unique tool for PLD development.

Search for Specified Properties

The parameters of all supported devices stored in the PLD Data Base can be used as search criteria by themselves or combined arbitrarily. For instance the desired properties could be specified as follows:

- number of in- and outputs
- nodes and feedbacks
- number of product terms
- polarity of the outputs
- number of pins
- number and type of special functions
- name of device (also incomplete)
- desired technical properties of a device such as its electrical data, delay times, technology, manufacturer

This also makes it easier to find compatible types: questions such as "Is there a type we can replace the PLD we are now using which uses less current and is packaged in a PLCC?" are immediately answered by the PLD Data Base.

All information about the stored devices can be quickly and easily accessed by the developer. If you select the name of a certain device, then the structural specifications and the parameters appear on two screens. On a third screen you can see an essential extract of the logical structure of the device (macro cell) and the fourth screen contains the pinout of the respective PLD.

Always up to Date

At present the PLD Data Base supports over 270 PAL/PLA devices and more than 1100 PROM devices. These numbers only include the *structures* of the devices and not the innumerous variants of the devices with respect to *power, speed* and *packaging*, which are also contained in the data base. As the data base is constantly being supplemented, the user is always up to date. We often offer the support of new devices before the ICs are even on the market.

LOG/iC SCHEMATIC MACRO LIBRARY (SML)

- Input of schematics via standard CAD
- Old designs can be easily used again
- Extendable library of standard devices
- Hierarchical design with graphics
- Automatic file exchange
- Simple, menu-oriented operation

Optional Design Entry: Schematic Input

The realization possibilities and methods of electronics have considerably improved in the last few years, but not the basics. Old designs can therefore still be used when clothed in new devices (PLD, arrays). Instead of a new development it is often better to continue to use the old, proven circuit either as a whole or part thereof.

However, a practical problem generally crops up: "How do I get my old designs or parts thereof into the PLD compiler?" This is where the *schematic entry* is the right aid:

"Schematic Macro Library" (SML) now also allows the input of net lists from the third-party systems into LOG/iC, for example from the widely-spread schematic editor, OrCAD.

The SML contains a large number of well-known TTL and CMOS circuits, but also manages the circuits you design yourself. A schematic editor allows industrial circuits as well as your own designs to be graphically connected to each other. LOG/iC then turns it into a PLD or an array. The Schematic Macro Library works with all LOG/iC packages from Release 3.2.

The Schematic Macro Library consists of three components:

- Net List Converter
- Standard Library
- Library Manager

It allows a circuit diagram which has been developed with a CAD system to be converted into a LOG/iC design file.

To do so, the user first draws the circuit design with his CAD system (e.g., OrCAD) into which he can integrate complete existing and new parts. From this, OrCAD then generates a net list of the circuit in *EDIF format*.

SML's net list converter converts this net list into a design file which the LOG/iC compiler "understands." The graphically described function blocks can also be linked to other blocks, making hierarchical designs possible. The same applies for other common schematic editors.

The current version of SML supports OrCAD's schematic editor SDT, and also the editors from Mentor and Viewlogic.

Extendable Standard Library

The Schematic Macro Library contains a library with a multitude of logical modules which are described in LOG/iC design files. These include almost all ICs from the TTL series 74xx, 74LSxx, 74HCxx, etc., as well as the most important ones from the series CMOS 4000.

The library manager forms the cross-references between devices with the same function but different names. It also manages function macros created by the user, e.g., a library of his old designs. This allows you to work block-oriented with graphics. The contents of the library can be displayed on the screen at any time.

Even without a CAD system, the library is a great help in practice. Even when it is not possible to represent the information graphically, the net lists can be transferred to the LOG/iC compiler.

Technical Data

- Contents of the library: at present about 1000 TTL and CMOS devices
- Your own designs can be added to the library as macros
- Number of in/outputs of a design: max. 256/256 (PC: 128/128) N.B.: Please note limitations imposed by the CAD system
- Number of blocks per design: max. 100

Automatic Correspondence with LOG/iC

The Schematic Macro Library is simple to use. It is operated with menus. For example, the CAD system can be *directly accessed* with cursor keys or the mouse from the LOG/iC main menu.

The individual files are automatically exchanged between the CAD system and LOG/iC. The correct net list version is also automatically generated.

Once the net list converter of the SML generates the LOG/iC design file, LOG/iC checks the data in the same way as for any other design entry. Serious errors can be eliminated at an early stage in development. For further work on the circuit design, all common test and processing aids of the LOG/iC system are available.

The schematic input can be arbitrarily mixed with other circuit definitions based on LOG/iC's syntax. In this way it is possible to describe every circuit or part thereof in the syntax most suitable. In addition to the circuit diagram input, LOG/iC "understands":

- function tables
- Boolean equations
- the FSM (finite state machine) syntax

PERFORMANCE OF THE LOG/iC CAE SYSTEM-SUMMARY

• Design Entry	Boolean Equations Truth Tables FSM Consistency Check	Schematics – Circuits – FSM Functional Verification
• Minimization	Proprietary, tailored Algorithms for: PAL: FACT optimizer PLA: BRUNO algorithm	Gates: Two stage optimization
• Transformation into Device Structures	PLD Library with over 275 PLD Architectures PLD Data Base with automatic Chip Selection	Support of all Gate Libs and also LCA devices Insertion of new Microprograms into existing MARC structures
• Support of Test	Automatic Generation of Testvectors for PLDs	Testlistings for MARCs Timing verification for Gates
• Documentation	Extent and Kind of Documentation selectable	Documentation tailored to chosen Device Family
• Integration into CAE Environment	Netlist-Interfaces for Input and Output of Design Data	Communication Module for controlling the Device Programmer Postprocessor Interface

LOG/iC HARDWARE PLATFORMS

Computer	Operating Systems (min. Rel.)	Storage Media
IBM-PC IBM PS/2	DOS (2.0)	5.25" 360 KB 3.5" 720 KB
VAX 730 up to 86xx	VMS (4.2) ULTRIX (2.2)	1600 bpi Magtape
VAX Workstation	mic. VMS (4.2) ULTRIX (2.2)	TK50 Cartridge 1600 bpi Tape
Apollo Workstation DN3xx, 5xx, 6xx DN3000, DN4000	AEGIS (9.5)	0.25" Cartridge Tape
HP9000-318 up	HP-UX (6.01)	0.25" Cartridge Tape
Sun 386i Sun series 3	SunOS SunView	0.25" Cartridge Tape

ISDATA
800 Airport Road
Monterey, CA 93940
USA
Tel: 408-373-7359
Telefax: 408-373-3622

ISDATA GmbH
Haid-und-Neu-Str.7
D-7500 Karlsruhe 1
West Germany
Tel: 07 21/69 30 92
Teletex: (17) 721170 ihkutb
Telefax: 07 21/17 42 63

Speed Your Logic Designs with Design Synthesis, Architecture Mapping, and Fully Automatic Multi-part Design Partitioning

AN OVERVIEW OF MINC's PLDESIGNER

MINC's PLDesigner can reduce the time you spend designing with PLDs. This unique, third-generation design system is different from older, compiler-type tools because:

- There is a single language for all types of devices. You can enter a design independent of the device or set of devices that will eventually be used to implement the design.
- PLDesigner can automatically select the device architecture that is best for implementing a design. This offers you solutions that you may not have considered, including the most sophisticated devices.
- PLDesigner shows you 10 different implementations of the same design. You can then choose the alternative that is best suited for your design.
- If more than one device is required in your design, PLDesigner will automatically divide the design across multiple parts.

The intelligence included with PLDesigner automatically implements a design once it has been functionally described. This allows you to concentrate *on the design* without becoming an expert on hundreds of device architectures. Since PLDesigner is a universal system, there is no need to learn a different language when using a new part.

As a result, PLDesigner makes it easy for designers that are new to PLDs to work with all types of architectures. PLDesigner drastically speeds up the design process for the experienced user by eliminating tedious tasks. And, by offering alternatives to the design implementation, you can be sure that your solution is optimal.

Design Entry

With the power of PLDesigner's expert system, you now spend most of the design time describing the design instead of searching for suitable devices. Since design entry is now of primary importance, PLDesigner provides many ways of describing the design.

- MINC's high-level Pascal-like language includes self-documenting constructs such as CASE and IF/THEN/ELSE. Truth tables, Boolean expressions, and powerful state machine commands are available for a wide variety of design structures. The same language is used for all PLDs, including PAL® devices, PROMs, and sequencers.
- Schematic entry supports OrCAD®, P-CAD®, and FutureNet® and other schematic capture systems with the EDIF 2.00 netlist format.
- With PLDesigner's patented waveform entry system, you can describe synchronous input and output waveforms; PLDesigner will synthesize the required implementation logic. This method is ideal for handshake control, glue logic, and any other design that can be described with a timing diagram.

These design methods can be combined to form a system. Using the most appropriate entry method, you can enter each section of the design. Each portion, then, is independently simulated and documented. When all the modules have been entered and verified, they can be combined and simulated as a system. At that point, the entire design can be handed to PLDesigner's expert system for architecture mapping.

For example, the front end of a PLD design could be entered using a schematic (perhaps "borrowed" from an existing discrete design). Control circuitry could be described in the language as a state machine, with handshaking to other devices described with waveforms. These modules would be combined together to form a system, then partitioned into multiple PLDs, if necessary.

With PLDesigner's unique ability to combine designs, portions of a design can be stored away as a "design library" for use on other projects!

Eight-bit Bidirectional Shift Register

As an example of the language entry method, consider the following design of an eight-bit bidirectional shifter. Notice the use of IF/THEN/ELSE statements to quickly define the function of the design.

This design requires two PLDs to implement because of the large number of inputs (14) and outputs (9). Your job, however, is simple. Since the design is entered independent of the eventual implementation, it is as easy to enter a 4-bit shift register that would fit into a single device, as it is to implement a 16-bit shift register that could require three devices.

```
TITLE          SHIFTER.SRC;
COMMENT        8-bit Bidirectional Shift Register;
FUNCTION       shift;
MACRO     left  1; "left is true
INPUT     d7..d0, shift_in;
INPUT     output_enable, parallel_load, no_shift, direction, reset;
OUTPUT    q7..q0, shift_out CLOCKED_BY sys_clock ENABLED_BY output_enable;
IF (reset)
    THEN
        [q7..q0] = 0; "reset outputs
    ELSE
        IF (parallel_load)
            THEN
                [q7..q0] = [d7..d0]; "load outputs with input data
            ELSE
                IF (no_shift)
                  THEN
                      [q7..q0] = [q7..q0]; "hold current value
                  ELSE
                      IF (direction = left)
                          THEN
                              [shift_out, q7..q0] = [q7..q0, shift_in]; "shift left
                          ELSE
                              [q7..q0, shift_out] = [shift_in, q7..q0]; "shift right
END shift; "end of function
```

Bus Arbiter

Another example of PLDesigner's high-level language is state machine entry. State machines are useful for designing controllers in systems, or any time a sequential algorithm must be implemented in hardware. The following example shows a bus arbiter that grants access to two controllers requesting a bus.

Many state machine designs start as a "bubble diagram." With PLDesigner's language, it is easy to take each bubble in the diagram, and convert it into states for a state machine design.

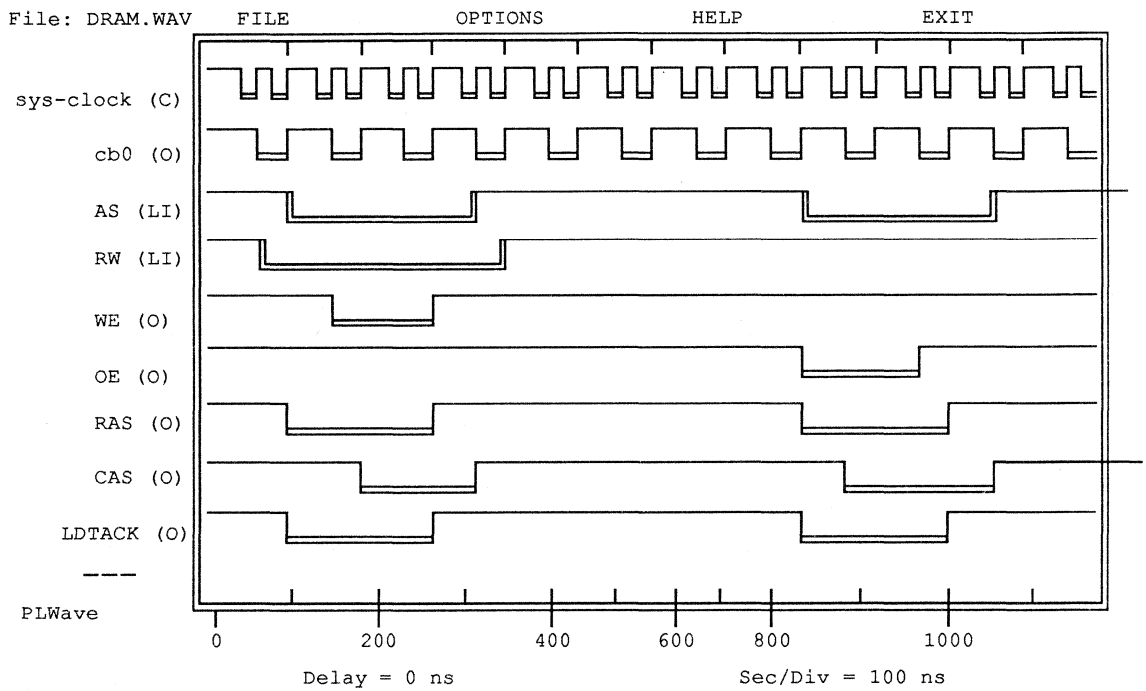
```
TITLE       ARBITER.SRC;
COMMENT     Bus arbiter to allow a bus to be shared between two processors.
            Processor A has priority in the case of simultaneous requests;
FUNCTION    arbiter;
LOW_TRUE INPUT  bus_rq_A, bus_rq_B; "bus request A & B
LOW_TRUE OUTPUT bus_grant_A, bus_grant_B; "bus grant A & B
STATE_MACHINE bus_arbiter;
  CLOCKED_BY   sys_clock;   "The state bits for this design will be clocked by
                            "sys_clock
STATE idle:
      bus_grant_A = 0;
      bus_grant_B = 0;
      IF (bus_rq_A)
        THEN
          GOTO A_has_bus;
        ELSE
          IF (bus_rq_B) "To get here, A has not requested the bus
            THEN
              GOTO B_has_bus;
            ELSE
              GOTO idle;    "To get here, neither processor has requested
                            "the bus
STATE A_has_bus:
      bus_grant_A = 1;
      bus_grant_B = 0;
      IF  (bus_rq_A)
        THEN
          GOTO A_has_bus; "A holds onto bus as long as needed
        ELSE
          IF (bus_rq_B) "To get here, A must be finished with the bus
            THEN
              GOTO B_has_bus;
            ELSE
              GOTO idle;    "To get here, A has finished with the bus and
                            "B has not requested it.
STATE B_has_bus:
      bus_grant_A = 0;
      bus_grant_B = 1;
      IF (bus_rq_B)
        THEN
          GOTO B_has_bus; "B holds onto bus as long as needed
        ELSE
          IF (bus_rq_A) "To get here, B must be finished with the bus
            THEN
              GOTO A_has_bus;
            ELSE
              GOTO idle;    "To get here, B has finished with the bus and
                            "A has not requested it.
END bus_arbiter;"end of state machine
END arbiter;     "end of function
```

DRAM Controller for a 68000 Microprocessor

In some cases, the behavior of hardware is in the form of timing diagrams. You will see this most often when interfacing a microprocessor to peripheral devices. When a hardware description is in the form of timing diagrams, PLDesigner's waveform entry method can make entry as easy as drawing the timing diagram!

This design example provides the DRAM control logic for a 68000 microprocessor. The "AS" and "RW" signals are from the microprocessor, "sys_clock" is the clock, the LDTACK signal is fed back to the 68000 to terminate the bus cycle, and all other signals are control lines required by the DRAM.

The waveforms are drawn on-screen with a mouse or by stepping along and designating "H" or "L" with the keyboard. PLDesigner's waveform compiler takes the waveforms you have drawn and converts them into the Boolean equations to be fit into PLDs.



Combining Multiple Designs

Using PLDesigner's unique capability of combining designs, you can merge the bus arbiter in the second example with the DRAM controller in the third example to fit them into a single device. To do this, the following file is created:

```
TITLE        COMBINE.SRC;
COMMENT      This combines a bus arbiter and DRAM controller into a single
system;
"Note: sys_clock is the clock used in both designs
FBINCLUDE    'dram';
FBINCLUDE    'arbiter';
```

The designs are automatically combined with the results placed in a single file. If desired, system test commands can be included with this file to simulate the behavior of the entire system. Once completed, the entire design process is automatically documented, as follows:

```
PLDesigner - (c) Copyright 1987, MINC Incorporated
EQUATIONS FOR SYSTEM
INPUT SIGNALS:
        LOW_TRUE GND
        HIGH_TRUE VCC
        HIGH_TRUE AS
        HIGH_TRUE RW
        LOW_TRUE BUS_RQ_A
        LOW_TRUE BUS_RQ_B
OUTPUT SIGNALS:
        LOW_TRUE CB0
        LOW_TRUE WE
        LOW_TRUE OE
        LOW_TRUE RAS
        LOW_TRUE CAS
        LOW_TRUE LDTACK
        LOW_TRUE BUS_GRANT_A
        LOW_TRUE BUS_GRANT_B
        HIDDEN HIGH_TRUE BUS_ARBITER7-S0
        HIDDEN HIGH_TRUE BUS_ARBITER7-S1
REDUCED EQUATIONS:
CB0.CLK  = sys_clock ;
    .D  = /CB0 ;
WE.CLK = sys_clock ;
    .D = /AS*/RW*/OE*/CAS*LDTACK + /CB0*WE ;
OE.CLK = sys_clock ;
    .D  = /AS*RW*/CAS + CB0*OE ;
RAS.CLK  = sys_clock ;
    .D  = /AS*/CAS + LDTACK*/CB0 + LDTACK*OE ;
CAS.CLK  = sys_clock ;
    .D  = /AS*/RW*WE + /AS*RW*LDTACK ;
LDTACK.CLK   = sys_clock ;
    .D  = /CAS*/AS + /CB0*LDTACK + CAS*OE ;
BUS_GRANT_A.EQN = BUS_ARBITER7-S0*/BUS_ARBITER7-S1 ;
BUS_GRANT_B.EQN = /BUS_ARBITER7-S0*BUS_ARBITER7-S1 ;
BUS_ARBITER7-S0.CLK = sys_clock ;
    .D = BUS_RQ_A*/BUS_RQ_B*/BUS_ARBITER7-S0 +
         BUS_RQ_A*/BUS_ARBITER7-S1 ;
BUS_ARBITER7-S1.CLK = sys_clock ;
    .D = BUS_RQ_B*/BUS_ARBITER7-S1*/BUS_RQ_A +
         BUS_RQ_B*BUS_ARBITER7-S1*/BUS_ARBITER7-S0 ;
```

Device Selection Criteria

After completing the design entry, you hand your design over to PLDesigner's expert system. PLDesigner does not blindly select devices for you; instead, you specify what a "best" solution is in your environment.

You can declare the criteria that each device must meet (logic family, temperature, speed, manufacturer, package, etc.). You also can select what is more important in the implementation (cost, speed, number of parts, current consumption, etc.).

Your design philosophy is passed to the partitioning system that performs the architecture mapping, selecting the best device architecture for the design. PLDesigner will select from PROMs, PAL devices, and sequencers in a combination that provides the best solution for your design problem.

PLDesigner----Partitioning Menu

```
  System File    :     COMBINE
Available File   :     MINCLIB.AVL

START PARTITIONING                    EDIT PARTITIONING
EXIT MENU                             EDIT DEVICE LIBRARY


                              Constraints          Priority (10 max)

Number of Devices  :              ---                    N/A
Logic Family       :              TTL                    N/A
Manufacturer       :              AMD                    N/A
Package Type       :              DIP                    N/A
Temperature        :              COM                    N/A
Total Price        :              N/A                    10
Total Size         :              N/A                    --
Max Prop Delay     :              ---                    --
Min Frequency      :              ---                    --
Max Current Usage  :              ---                    --
User Criteria 1    :              ---                    --
User Criteria 2    :              ---                    --
```

Implementation Selection

Based on the selection criteria you entered, PLDesigner automatically explores hundreds of combinations of devices to find the top ten solutions to your design problem. When finished, you select the implementation that best meets the project needs. If none of the solutions seem satisfactory, you can change your selection criteria and repeat the process until you're satisfied with the implementation, without modifying your original design.

By exploring different criteria, you are assured that the final implementation you select is the most rigorous solution to your design problem.

In this example, the P20RP8 was selected to provide an economical, one device solution. You might select another solution, based on what you have available in lab stock, or what parts are approved for manufacturing. Or you could select a larger part to allow an upgrade path without changing PC board layout.

PLDesigner-Partitioning Solution Menu

```
System Name : COMBINE EXIT
Possible Solutions:          Attempted : 594          Found : 47
==> 1    P20RP8                                    210ma 40ns $2.89
    2    P20XRP8                                   180ma 45ns $3.41
    3    P20RP6, P16R8                             300ma 55ns $4.84
    4    P20RP8, P16R6                             300ma 55ns $4.84
    5    P20RP10, P16R6                            300ma 55ns $4.84
    6    P20RP4, P16R6                             300ma 55ns $4.84
    7    P20RP6, P16R6                             300ma 55ns $4.84
    8    P20RP8, P16R4                             300ma 55ns $4.84
    9    P20RP10, P16R4                            300ma 55ns $4.84
   10    P20RP4, P16R8                             300ma 55ns $4.84
Possible Devices:                                Partitioning Completed
   P16R8 P16R6 P16R4 P16L8 P18P8 P20RP6 P20RP4 P20RP10 P20RP8
   P22P10 P20R4 P20L8 P20L10 P20R8 P20R6 P22XP10 P20XRP8 P20XRP6
   P20XRP4 P20XRP10 P22V10C P22V10R
```

Device Programming

After you select the final design solution, PLDesigner creates the fuse maps (JEDEC, or others) for the device programmer, including the test vectors created by your system simulation. PLDesigner will automatically partition the device test vectors when partitioning the design. No need to write a separate verification routine for each device. Then, the document file is updated to show the pinouts of the devices to be programmed.

The following figure shows the pinout documentation for the combined arbiter/DRAM controller design.

Note: On the P20RP8, pins 14 and 23 are the only combinatorial outputs. PLDesigner recognizes this and assigns these pins to the signals that must be combinatorial (the bus grant signals from the bus arbiter). All the other signals require clocked outputs, so PLDesigner assigns them to pins with D flip-flops. The "BUS_ARBITER7–S1" and "–S0" signals are state bits automatically created by PLDesigner to implement the arbiter state machine. These could be used as status bits in the design, or ignored as the designer sees fit.

This design nicely demonstrates the power of PLDesigner's architecture mapping, which selects a device with the correct mix of registered and combinatorial outputs to implement the design.

```
DOCGEN: COMBINE          PINOUT DIAGRAMS

                      Device 1 - P20RP8_0
                      ------\___/------
sys_clock  1 [ | CLK            Vcc  | ] 24
        AS 2 [ | Input        Biput  | ] 23  BUS_GRANT_A
        RW 3 [ | Input       Output  | ] 22  BUS_ARBITER7-S1
  BUS_RQ_A 4 [ | Input       Output  | ] 21  BUS_ARBITER7-S0
  BUS_RQ_B 5 [ | Input       Output  | ] 20  RAS
           6 [ | Input       Output  | ] 19  CB0
           7 [ | Input       Output  | ] 18  CAS
           8 [ | Input       Output  | ] 17  LDTACK
           9 [ | Input       Output  | ] 16  OE
          10 [ | Input       Output  | ] 15  WE
          11 [ | Input       Biput   | ] 14  BUS_GRANT_B
          12 [ | GND             OE  | ] 13  GND
               ------------------------
```

SUMMARY

If you're just starting with PLDs, PLDesigner's automatic device selection and architecture mapping allows you to design without a painful learning curve. And, this powerful toolset allows the experienced PLD designer to quickly evaluate alternatives in implementation.

By offering implementation-independent designs, you concentrate on the design, not the devices. A wide range of input methods actually makes the design process easier, because you are using the entry method that best suits the design. And, you can combine portions of a design to build up an entire PLD system.

Architecture mapping selects the top ten solutions for a design, using the optimal device architecture. This means you can confidently select the best possible implementation for your design. Fully automatic partitioning of the design and associated test vectors across multiple devices relieves the tedious and time-consuming task of manual dividing of circuits.

PLDesigner is available for the PC and most workstation environments. For more information on MINC design systems, contact:

MINC Incorporated
6755 Earl Drive
Colorado Springs, CO 80918
(719) 590-1155
FAX (719) 590-7330

INTRODUCTION

There are two common situations when a PAL device user wants to program parts:

1. The user has a master device and wants to program the master pattern into new unprogrammed parts from the same or from a different manufacturer.

2. The user has a file that is in JEDEC standard Programmable Logic Data Transfer Format and wants to send the file to a programmer and program parts to that pattern.

All approved programmers can accomplish either of these tasks. You will have to refer to your programmer manual for detailed procedures, but here are some general guidelines:

Programming with the Use of a Master Device

Suppose you have a master device and you want to program a device of the same type with exactly the same pattern. The master device can be an MMI or AMD device or another manufacturer's functionally equivalent device. Follow these steps:

1. Set the programmer to read (or copy) the master device. This may require having a hardware adaptor for the master and entering a product code unique to the manufacturer and device type.

2. Install the correct adaptor (if required). Enter the appropriate product code information or select the device type from the menu. Then place the master device in the correct socket and read its fuse pattern into the programmer memory. Use whatever operating sequence is required by the programmer for this operation.

3. The pattern is now in the programmer memory and will remain there until the memory is cleared or the programmer power is turned off. Changing an adaptor or product code will not erase the memory. Usually at the end of a copy operation a checksum will be displayed. Make a note of this number. The checksum is a calculated hexadecimal code for the pattern loaded into memory. It can be very helpful in diagnosing any programming problems. If a part is to be re-used frequently as a master device it is a good practice to write the checksum on the top of the part. Never proceed with programming without checksum agreement after reading a master.

Error Detection

As a matter of curiosity take the part out of the socket once and read an empty socket. Also read a known blank part (using the right adaptor). Checksums from these two situations will be helpful in diagnosing two common problems when programming from masters:

- Forgetting to lock down the socket lever to make good contact after loading a part
- Loading an unprogrammed part as a master by mistake.

4. Now prepare the programmer for the device to be programmed with the master pattern loaded into memory. Some programmers require different adaptors for different manufacturer's parts. If the programmer being used has this requirement, be sure to use the proper adaptor for the exact part number to be programmed. Using the wrong adaptor can cause permanent damage to the parts. Always check for adaptor compatibility.

5. Everything's OK. You have the correct adaptor, the right device code (or have selected the device from the menu) and you wrote down the checksum that you got after loading the master. Now put the programmer in the mode used for programming from its memory and execute the programming operation.

There is some variation in the sequence of events carried out by different programmers during the programming cycle, but all of them program and verify the appropriate fuses to match the pattern in the programmer memory. Such operations as Blank Checks, Illegal Bit Checks, Test Vector Testing, and Security Fuse Programming can be a part of the programming sequence. Check the programmer manufacturer's manual for the availability and appropriate use of these features.

The essential part of the programming cycle is the programming and verification of each fuse followed by a verification of all fuses at both low and high Vcc. At the very end of the programming sequence you will see the checksum for the part you have just programmed. This checksum should agree with the master part checksum. You now have a programmed part that is functionally identical to the master.

Programming From a JEDEC File

A JEDEC standard file is the output of design software packages used to specify programming pattern information to a programmer. All approved programmers will accept JEDEC files. A JEDEC file is normally generated on a computer by PLD design software. The unique aspect of programming from a JEDEC file is the transfer of the file to the programmer. After the file has been transferred into the programmer, the programming task is identical to programming from a master with one exception. The exception is that design software may be used to prepare test vectors to be applied to a device immediately following the programming cycle. These vectors will be transmitted with the JEDEC fuse file and they have a JEDEC standard format of their own.

General guidelines for transfer of a JEDEC file and programming are as follows:

1. Make sure your file is in the standard JEDEC format. This will not be a problem if you are using software for file preparation that adheres to this standard.

2. Connect the JEDEC file source to the programmer with an RS232 cable. The programmer manual will describe the connection details.

3. Prepare the programmer for receiving a JEDEC file over a link. This will generally involve entering the product code information and putting the programmer in a ready-to-receive mode.

4. Transmit the file from the computer source using commercially available communications software or operating system commands.

5. After transmission a checksum should appear on the programmer display. Part of the JEDEC standard file is a checksum. If the displayed checksum is the same as the JEDEC file generated checksum transmission has been successful.

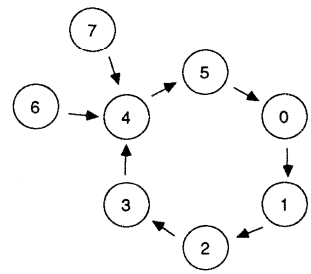
6. Program a PAL device by first installing the correct adaptor (if needed) and then entering the programming mode. Finally put a part in the socket and execute the programming operation.

Register Preload

Register preload is an aid to functional testing of registered PAL devices. Functional testing is usually performed after a device is programmed but before it is installed on the circuit board. Functional testing exercises the functional logic circuitry of a device that is not fully testable prior to programming, providing a higher final quality level for programmable products. For a more thorough discussion of functional testing and related quality issues see the ProPAL and HAL Devices section.

Using register preload, the registers of a device can be "preloaded" to any desired state value. The ability to set the registers to any arbitrary value is extremely useful for testing state machine designs where the output is fed back into the array as an input. It lets the user check for deadlock loops and proper recovery from illegal states. It also simplifies testing state transitions of states which may be difficult to reach through normal state transitions.

Consider the example of the 6-state counter illustrated in the state machine diagram of Figure 1.



14096-001A

Figure 1.

States 6 and 7 are illegal states, both transitioning to state 4. If the registers of the device are not preloadable, it is difficult to check for recovery from these states since they cannot be reached through normal state transitions. If register preload is available, however, it is a simple matter to write a set of vectors that sets the device to the illegal state and then clocks it and checks proper recovery.

If the device powers up in state 1 and you want to test the transition from state 0 → 1, the only way to check that transition is to write a series of vectors that cycle the device through the state sequence starting at state 1, until the desired state, state 0, is reached. With register preload, reaching state 0 is simply a matter of writing a vector that sets the device to that state.

In general, register preload simplifies the task of writing test vectors for functional testing, and is especially helpful in testing the conditions described in this discussion. However, test vectors written utilizing register preload can provide only a limited amount of functional coverage. Full coverage can only be achieved when the vectors used to test the device simulate actual operating conditions, and preload is not a normal operating condition.

Programmer Support

Not all programmers support register preload. The programmer guide lists the programmers that do support this feature. For more specific information regarding your programmer, contact the manufacturer.

Choosing the Right Programmer

Advanced Micro Devices has evaluated and approved several PAL device programmers, and choosing among them is not simple. You must consider many factors. Does the programmer handle all of the devices you will be using? Does it program PAL devices, sequencers, and PROMs? Does it program TTL, EPROM CMOS, EEPROM CMOS, and ECL technology products? How easily is it upgraded for future devices? Does it have provisions for test vectors, accepting JEDEC files, or a handler interface? And what about cost?

	AMD	Adams MacDonald		Data I/O			Digelec	Kontron	Logical Devices	Microprocess		Stag	
Programmer	LabPro	P11	Sprint+	US40	M60A/H	M29	860	EPP-80	ALLPRO	3000	5000	PPZ	ZL30
Features													
Price	V. Low	Low	Low	High	Low	Med.	Low	Med.	Low	Med.	Med.	Med.	Low
Standalone	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes	Yes
Handler	No	No	No	Yes	Yes	No	No	No	No	No	No	No	No
PLCC	No	No	No	Yes	Yes	Yes	Yes	No	No	No	No	No	Yes
Test Vectors	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Preload	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	No	No
Fingerprint	No	No	No	No	Yes	Yes	No	No	No	No	No	No	No
Fast Program	Yes	No	No	Yes	Yes	No	Yes	No	No	No	No	Yes	Yes
1 Pulse Prog	No	No	No	Yes	Yes	Yes	No	No	No	No	No	No	No
Updates	Pack	PROM	Disk	Disk	PROM	PROM	Pack	PROM	Disk	Disk	Disk	Card	PROM

Despite these variations in features, today's programmers fall into two broad categories, PC-based programmers and standalone programmers. PC-based programmers consist of a board (that plugs into a PC) and an external box with socket(s) for the device being programmed. The plug-in board contains the "intelligence" of the programmer, and, as the name implies, these programmers require a PC for use. Standalone programmers can perform all programming operations without a PC. PC-based programmers are usually lower cost and lower performance design and development tools that support a limited number of devices and have limited capabilities. Standalone programmers offer higher performance (e.g., faster programming), and are oriented to the production environment.

The chart above lists programmer features, as well as current support for some of the newer part types. This information should help you decide on the best programmer for your needs.

Approved Programmers

Advanced Micro Devices PAL devices are manufactured under strict processing procedures to provide our PAL device users with the highest-quality PAL devices available. We take the same approach in our programmer vendor approval process, and recommend that you choose an approved programmer for your PAL device programming needs.

The Benefits of Using Approved Programmers

When you choose an approved programmer you gain all the benefits of our thorough vendor evaluation. You can feel confident investing in equipment that will give you consistently reliable results and will be able to support current and future generations of programmable logic devices. When you select an approved programmer you get many benefits:

- Your programmed product is backed by our corporate warranty.
- New features and algorithm updates are quickly implemented.
- Any new programmer software and hardware releases are factory evaluated and approved before release.
- Your equipment will have a long "technical lifetime."
- Through our sales force and Field Applications Engineers you have a factory interface with the programmer vendors to deal with any issues or concerns that might arise.

The Approval Process

The Programmability Group at Advanced Micro Devices works closely with our programmer vendors to ensure that high-quality programming and testing support is available to all users of our PLDs.

To gain approval a programmer must pass a rigorous series of tests which include:

- Conformity to programming specifications.
- Devices programmed must pass all reliability tests. This reliability testing is performed by Advanced Micro Devices as part of the evaluation.
- Programmer must meet programming yield requirements for both array and security fuse programming.
- Programmer must be able to support JEDEC format files and communication standards.

Programmer vendors are encouraged to support structured test vector testing and preload capability, pin continuity and pre-programming security fuse checking.

New Product Support

Approved programmers must also provide timely support for new products and programming algorithm updates and revisions. This ensures PAL device users that no matter which approved programmer they choose, they can feel confident that it will support the latest and greatest PLDs we have to offer.

Additionally, we work closely with our approved vendors in the development of their new programmers and our new PLDs. This means that their new products will be able to support our future PLD offerings.

A Broad Range of Programmers

We work with a broad range of programmer vendors, so you can find a programmer to suit your engineering needs as well as your budget. Approved programmers cover the range from economical engineering/design prototyping tools to high-volume production units. We have a worldwide programmer vendor base, so programming support is available no matter where you use PAL devices. Approved programmers are available from American, British, French, German and Japanese vendors.

Our quality and reliability guarantees are made for products programmed with approved programmers only. Use of unapproved programmers voids our corporate warranty and may result in poor manufacturing yields and product performance. The Programmer Reference Guide is a valuable tool. The information it contains can help you obtain consistent, reliable high-quality programming results with your PLDs.

LabPro™ Programmer

The Complete and Affordable Programmable Logic System

Advanced programmable logic development tools have just become affordable. Advanced Micro Devices, the programmable logic leader, is proud to announce the LabPro Programmable Logic Development System. Dedicated to Advanced Micro Devices programmable logic devices, it is THE complete, easy-to-use development system, at a very affordable price.

The LabPro system is the programmable logic development system of the future as well as the present. Developed in conjunction with Digelec, Inc., it supports Advanced Micro Devices PLDs — in CMOS, ECL, and TTL technologies — from our state-the-art sequencers to our industry standard 24- and 20-pin architecture products, and is designed to be easily updatable for support of our future PLD offerings.

A COMPLETE DESIGN AND PROGRAMMING SYSTEM

The LabPro system is accompanied by PALASM® Software. Together, they let you go from a logic design idea to a final programmed and tested PLD.

PALASM software supports all Advanced Micro Devices PAL® devices. It accepts all logic design inputs in a variety of logic entry formats. Once your design has been assembled, you can simply transfer your design file to the LabPro system.

Easy to Use

The LabPro system can be used in the stand-alone mode or with any PC or PC-compatible system utilizing LOGILINK™ software from Digelec.

When used in the stand-alone mode, the LabPro system's 2-line by 16-character alphanumeric LCD display guides the user through all of the operating functions with clear and easy-to-follow instructions.

The four most frequently used functions — PROGRAM, VERIFY, READ and TYPE — can be directly accessed with a single key. The scroll up/down feature allows easy access to all other LabPro system functions.

Publication #	Rev.	Amendment	Issue Date
10279	C	/0	1/90

The on-board HELP function provides simple, immediate assistance during operation, minimizing the need to refer to the user's manual.

The SETUP function lets you set your own programmer setup values, which are stored in non-volatile memory.

Easy Programming

One keystroke programming makes programming a breeze. If you're operating the LabPro system in the remote mode, LOGILINK software provides a straightforward menu-driven operating mode.

The LabPro system can interface with any computer via its RS-232C serial port, and accepts data in both standard JEDEC and HEX formats.

Easy Logic Testing

The LabPro system performs a full range of tests before, during and after programming to ensure quality programming.

The built-in test (BIT) automatically checks the programmer when it is powered up. The continuity test checks to ensure that the device being programmed is correctly inserted into the programming socket. After programming, the array verify test automatically performs a fuse-by-fuse comparison check of the programmed device to ensure the correct pattern has been programmed. The functional testing option provides you with structured vector testing capability for up to 2500 test vectors. The LabPro system also supports register preload for preloadable devices.

Easy to Update

Take advantage of the LabPro System's innovative SOFTPACK™ algorithm update feature. When it's time for an update, simply remove the SOFTPACK cartridge from its slot at the rear of the programmer, replace it with the new one and you're ready to program the latest devices from Advanced Micro Devices.

Easy to Afford

All of this at a fraction of what you would expect to pay for a complete development system — at a price that's very easy on your budget!

Don't Settle for Less!

The LabPro system offers a complete solution to your PLD programming needs. The LabPro system is compact, easy-to-use, and versatile. Get the LabPro system from Advanced Micro Devices and get support for the broadest line of PLDs available, from Advanced Micro Devices — the market leader.

Upwardly Mobile

Should you want to expand your programming capabilities to include other PLD manufacturers, the LabPro system is easily upgradable to a full Digelec Model 860. The Model 860 supports PLDs from a wide range of manufacturers. Contact your Digelec representative for more information.

Specifications

RS-232C Serial Port
Baud rate: 50–19,200
Parity: None/Odd/Even
Bits: 5, 6, 7, 8
Handshake: XON/XOFF, DSR
Format: JEDEC, HEX

RAM
Standard: 64K bytes
Optional: 256K bytes

Device Testing
Blank/Illegal Bit Check, Misplaced/Reversed, Current Overload, Continuity, Checksum, Vector Test (up to 2500), Preload, Array Verify

Device Packages Supported
20-, 24-, and 28-pin DIPs

FUNCTIONS
Device
Program, Verify, Read, Type, Blank/Illegal Bit Check, Checksum, Security Fuse, Test Vectors

Edit
JEDEC Fuses
Test Vectors

Communication
Transmit
Receive

Bit
Built-in Test

Help
On-Board Help Menu

General
Dimensions (W x H x D):
37 x 11.5 x 28 cm
14.6 x 4.5 x 11 in
Weight: Net 4.3 kg (9.5 lb)
Shipping: 5.5 kg (12.1 lb)
Power: 110/220 VAC, 50/60 Hz

Final

AmPGA081

Configuration PROM Programmer

DISTINCTIVE CHARACTERISTICS

- **Allows uploading, downloading, and saving of PROM files**
- **Can program and verify patterns**
- **Programs AMD and Xilinx™ Serial Configuration PROMs**
- **Programs 36K and 65K Serial Configuration PROMs**
- **Connects to serial port of IBM® PC-XT™, PC-AT™ or compatible**
- **Operates from PC via menu-driven software provided with the programming unit**
- **Accepts data files in any of the three XACT™-supported formats, MCS86, Tekhex and ExorMax**

GENERAL DESCRIPTION

The AmPGA081 Configuration PROM Programmer is designed to support the Am1736 and Am1765 Serial Configuration PROMs, (SCPs) 8-pin SKINNYDIP® PROMs used to configure programmable gate arrays. In addition, the AmPGA081 can also program the XC1736 device from Xilinx Corporation.

The programming unit, controlled using menu–driven, PC-based software, is connected to the serial port of an IBM PC-XT, PC-AT, or compatible. The AmPGA081 software and programmer are self-contained, and can be installed on a system other than that used for design development, such as one in a manufacturing area.

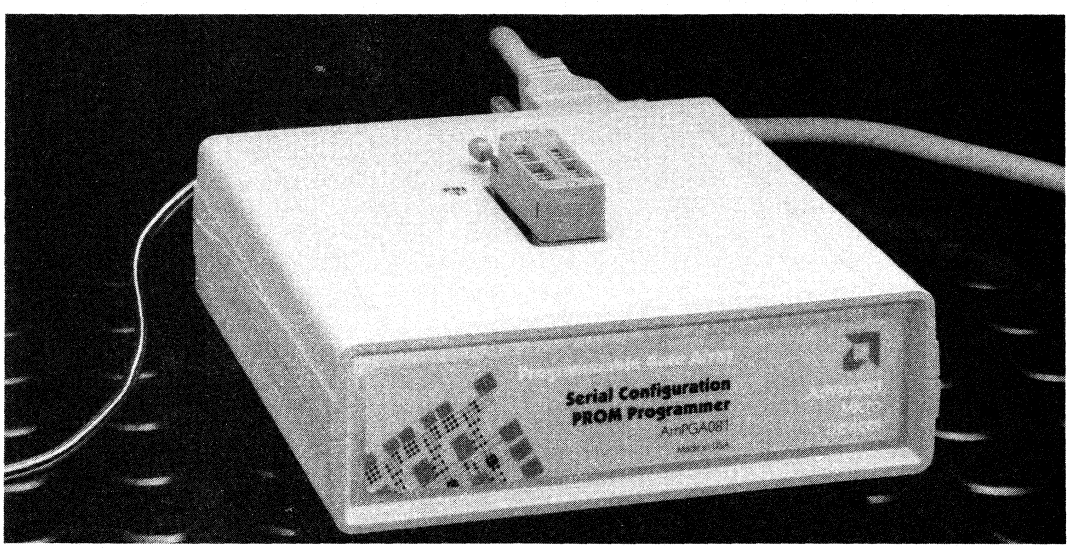
Designers compile their Logic Cell™ Array designs into a standard PROM format using the XACT Design System. The software provided with the AMPGA081 is then used to download the PROM file into the programming unit to program a SCP. PROM files can also be uploaded to the PC. SCPs already programmed can be verified, by comparing the device to a PROM file in RAM. The contents of the PROM can also be saved in RAM.

ORDERING INFORMATION

Further information is available from your local AMD sales office, authorized representative, or franchised distributor.

AmPGA081 **Configuration PROM Programmer**
Includes programming unit, power transformer, software and serial cable.

6



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Issue Date: August 1989

Advanced Micro Devices, Inc.
901 Thompson Place
Sunnyvale, CA 94088-3453
(800) 222-9323 or (408) 732-2400

LabPro™ Programmer

Architecture	Part Number	LabPro Revision
10H8	*PAL10H8	A1.0
10L8	*PAL10L8	A1.0
12H6	*PAL12H6	A1.0
12L6	*PAL12L6	A1.0
12L10	*PAL12L10	A1.0
14H4	*PAL14H4	A1.0
14L4	*PAL14L4	A1.0
14L8	*PAL14L8	A1.0
16C1	*PAL16C1	A1.0
16H2	*PAL16H2	A1.0
16H8	*AmPAL16H8	A1.0
16HD8	*AmPAL16HD8	A1.0
16L2	*PAL16L2	A1.0
16L6	*PAL16L6	A1.0
16L8	PAL16L8-7(-12Mil)	A1.1
	PAL16L8H-15/D/B	A1.0
	PAL16L8/B-2/B-4/A/A-2/A-4	A1.0
	PALC16L8Z	A1.1
	*PALC16L8Q	A1.0
	*AmPAL16L8	A1.0
16LD8	*AmPAL16LD8	A1.0
16R4	PAL16R4-7(-12Mil)	A1.1
	PAL16R4H-15	A1.0
	PAL16R4D/B	A1.0
	PAL16R4/B-2/B-4/A/A-2/A-4	A1.0
	PALC16R4Z	A1.1
	*PALC16R4Q	A1.0
	*AmPAL16R4	A1.0
16R6	PAL16R6-7(-12Mil)	A1.1
	PAL16R6H-15	A1.0
	PAL16R6D/B	A1.0
	PAL16R6/B-2/B-4/A/A-2/A-4	A1.0
	PALC16R6Z	A1.1
	*PALC16R6Q	A1.0
	*AmPAL16R6	A1.0
16R8	PAL16R8-7(-12Mil)	A1.1
	PAL16R8H-15	A1.0
	PAL16R8D/B	A1.0
	PAL16R8/B-2/B-4/A/A-2/A-4	A1.0
	PALC16R8Z	A1.1
	*PALC16R8Q	A1.0
	*AmPAL16R8	A1.0

Architecture	Part Number	LabPro Revision
16RA8	PAL16RA8	A1.0
16V8	PALCE16V8H/Q	A1.0
	16V8 as 10H8	A1.1
	16V8 as 10L8	A1.1
	16V8 as 12H6	A1.1
	16V8 as 12L6	A1.1
	16V8 as 14H4	A1.1
	16V8 as 14L4	A1.1
	16V8 as 16H2	A1.1
	16V8 as 16L2	A1.1
	16V8 as 16L8	A1.0
	16V8 as 16R4	A1.0
	16V8 as 16R6	A1.0
	16V8 as 16R8	A1.0
16X4	*PAL16X4	A1.0
18L4	*PAL18L4	A1.0
18U8	*PALC18U8	A1.1
20C1	*PAL20C1	A1.0
20L2	*PAL20L2	A1.0
20L8	PAL20L8-7(-12Mil)	A1.1
	PAL20L8-10(-15Mil)/B-2	A1.0
	PAL20L8B/A/A-2	A1.0
	PALC20L8Z	A1.0
20L10	PAL20L10A	A1.0
	AmPAL20L10	A1.0
	*PAL20L10	A1.0
20R4	PAL20R4-7(-12Mil)	A1.1
	PAL20R4-10(-15Mil)/B-2	A1.0
	PAL20R4B/A/A-2	A1.0
	PALC20R4Z	A1.0
20R6	PAL20R6-7(-12Mil)	A1.1
	PAL20R6-10(-15Mil)/B-2	A1.0
	PAL20R6B/A/A-2	A1.0
	PALC20R6Z	A1.0
20R8	PAL20R8-7(-12Mil)	A1.1
	PAL20R8-10(-15Mil)/B-2	A1.0
	PAL20R8B/A/A-2	A1.0
	PALC20R8Z	A1.0
20RA10	PAL20RA10	A1.0
	PAL20RA10-20	A1.0
	*PALCE20RA10Z	A1.1
20RS4	*PAL20RS4	A1.0
20RS8	*PAL20RS8	A1.0

Publication #	Rev.	Amendment	Issue Date
14097	A	/0	1/90

Advanced Micro Devices, Inc.

Architecture	Part Number	LabPro Revision
20RS10	*PAL20RS10	A1.0
20S10	*PAL20S10	A1.0
20V8	PALCE20V8H	A1.1
	20V8 as 14L8	A1.1
	20V8 as 16L6	A1.1
	20V8 as 18L4	A1.1
	20V8 as 20L2	A1.1
	20V8 as 20L8	A1.1
	20V8 as 20R4	A1.1
	20V8 as 20R6	A1.1
	20V8 as 20R8	A1.1
20X4	PAL20X4A	A1.0
	*PAL20X4	A1.0
20X8	PAL20X8A	A1.0
	*PAL20X8	A1.0
20X10	PAL20X10A	A1.0
	*PAL20X10	A1.0
22P10	*AmPAL22P10	A1.0
22V10	PAL22V10, AmPAL22V10	A1.0
	*PALC22V10	A1.0
29MA16	PALCE29MA16	A1.1
32VX10	PAL32VX10	A1.0
6L16	*PAL6L16A	A1.0
8L14	*PAL8L14A	A1.0

Notes:

*Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

Adams MacDonald Enterprises
800 Airport Road
Monterey, CA 93940
(408) 373-3607

P3 Programmer
P11 Programmer
SprintPlus Programmer

Architecture	Part Number	Revision		
		P3	P11	SprintPlus
10H8	*PAL10H8	3.0	1.09	3.2I
10L8	*PAL10L8	3.0	1.09	3.2I
12H6	*PAL12H6	3.0	1.09	3.2I
12L6	*PAL12L6	3.0	1.09	3.2I
12L10	*PAL12L10	3.0	1.09	3.2I
14H4	*PAL14H4	3.0	1.09	3.2I
14L4	*PAL14L4	3.0	1.09	3.2I
14L8	*PAL14L8	3.0	1.09	3.2I
16C1	*PAL16C1	3.0	1.09	3.2I
16H2	*PAL16H2	3.0	1.09	3.2I
16H8	*AmPAL16H8	3.1	1.09	3.2I
16HD8	*AmPAL16HD8	3.1	1.09	3.2I
16L2	*PAL16L2	3.0	1.09	3.2I
16L6	*PAL16L6	3.0	1.09	3.2I
16L8	PAL16L8H-15/D/B	3.0	1.09	3.2I
	PAL16L8/B-2/B-4/A/A-2/A-4	3.0	1.09	3.2I
	PALC16L8Z	—	2.0	3.2I
	*PALC16L8Q	—	2.0	3.2I
	*AmPAL16L8	3.1	1.09	3.2I
16LD8	*AmPAL16LD8	3.1	1.09	3.2I
16P8	PAL16P8A	3.0	1.09	3.2I
16R4	PAL16R4H-15	3.0	2.0	3.2I
	PAL16R4D/B	3.0	1.09	3.2I
	PAL16R4/B-2/B-4/A/A-2/A-4	3.0	1.09	3.2I
	PALC16R4Z	—	2.0	3.2I
	*PALC16R4Q	—	2.0	3.2I
	*AmPAL16R4	3.1	1.09	3.2I
16R6	PAL16R6H-15	3.0	2.0	3.2I
	PAL16R6D/B	3.0	1.09	3.2I
	PAL16R6/B-2/B-4/A/A-2/A-4	3.0	1.09	3.2I
	PALC16R6Z	—	2.0	3.2I
	*PALC16R6Q	—	2.0	3.2I
	*AmPAL16R6	3.1	1.09	3.2I
16R8	PAL16R8H-15	3.0	2.0	3.2I
	PAL16R8D/B	3.0	1.09	3.2I
	PAL16R8/B-2/B-4/A/A-2/A-4	3.0	1.09	3.2I
	PALC16R8Z	—	2.0	3.2I
	*PALC16R8Q	—	2.0	3.2I
	*AmPAL16R8	3.1	1.09	3.2I
16RA8	PAL16RA8	3.0	1.09	3.2I
16RP4	PAL16RP4A	3.0	1.09	3.2I
16RP6	PAL16RP6A	3.0	1.09	3.2I
16RP8	PAL16RP8A	3.0	1.09	3.2I
16X4	*PAL16X4	3.0	1.09	—
18L4	*PAL18L4	3.0	1.09	3.2I
18P8	AmPAL18P8	3.1	1.09	3.2I
18U8	*PALC18U8	—	2.0	3.2I

Adams MacDonald Enterprises

Archi-tecture	Part Number	Revision P3	Revision P11	Revision SprintPlus
20C1	*PAL20C1	3.0	1.09	3.2I
20L2	*PAL20L2	3.0	1.09	3.2I
20L8	PAL20L8-10(-15Mil)/B-2	3.0	2.0	3.2I
	PAL20L8B/A/A-2	3.0	2.0	3.2I
	PALC20L8Z	—	1.09	3.2I
20L10	PAL20L10A	3.0	1.09	3.2I
	AmPAL20L10	—	2.0	—
	*PAL20L10	3.0	1.09	3.2I
20R4	PAL20R4-10(-15Mil)/B-2	3.0	2.0	3.2I
	PAL20R4B/A/A-2	3.0	2.0	3.2I
	PALC20R4Z	—	1.09	3.2I
20R6	PAL20R6-10(-15Mil)/B-2	3.0	2.0	3.2I
	PAL20R6B/A/A-2	3.0	2.0	3.2I
	PALC20R6Z	—	1.09	3.2I
20R8	PAL20R8-10(-15Mil)	3.0	2.0	3.2I
	PAL20R8B/B-2/A/A-2	3.0	2.0	3.2I
	PALC20R8Z	—	1.09	3.2I
20RA10	PAL20RA10-20	3.0	1.09	3.2I
	PAL20RA10	3.0	1.09	3.2I
20RS4	*PAL20RS4	3.0	1.09	—
20RS8	*PAL20RS8	3.0	1.09	—
20RS10	*PAL20RS10	3.0	1.09	—
20S10	*PAL20S10	3.0	1.09	—
20X4	PAL20X4A	3.0	1.09	3.2I
	*PAL20X4	3.0	1.09	3.2I
20X8	PAL20X8A	3.0	1.09	3.2I
	*PAL20X8	3.0	1.09	3.2I
20X10	PAL20X10A	3.0	1.09	3.2I
	*PAL20X10	3.0	1.09	3.2I
22P10	*AmPAL22P10	—	2.0	3.2I
22V10	PAL22V10, AmPAL22V10	3.1	1.09	3.2I
	*PALC22V10	—	2.0	3.2I
23S8	AmPAL23S8	—	2.0	3.2I
32VX10	PAL32VX10	—	—	3.2I
6L16	*PAL6L16A	3.0	—	—
8L14	*PAL8L14A	3.0	—	—
141	*Am29PL141	—	2.0	3.2I
	*Am29LPL141	—	—	3.2I
142	*Am29PL142	—	2.0	—
14R21	*PMS14R21	—	2.0	—

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(800) 247-5700 or (206) 881-6444

UniSite™ 40 Programmer
Model 60 Programmer
Model 29A/B Programmers
LogicPak™ 303A-V04

Architecture	Part Number	Family-Pinout Code	Revision					
			UniSite 40		Model 60		Model 29A, 29B LogicPak 303A-V04	
			DIP	PLCC	DIP	PLCC	DIP 303A-011A	PLCC 303A-011B
10H8	*PAL10H8	22-18	1.54	1.5	V05	V12	V01	V03
10L8	*PAL10L8	22-13	1.54	1.5	V05	V12	V01	V01
12H6	*PAL12H6	22-19	1.54	1.5	V05	V12	V01	V03
12L6	*PAL12L6	22-14	1.54	1.5	V05	V12	V01	V01
12L10	*PAL12L10	22-01	1.54	1.5	V05	V12	V01	V01
14H4	*PAL14H4	22-20	1.54	1.5	V05	V12	V01	V03
14L4	*PAL14L4	22-15	1.54	1.5	V05	V12	V01	V01
14L8	*PAL14L8	22-02	1.54	2.3	V05	V12	V01	V01
16C1	*PAL16C1	22-21	1.54	1.5	V05	V12	V01	V03
16H2	*PAL16H2	22-22	1.54	1.5	V05	V12	V01	V03
16H8	*AmPAL16H8	97-25	1.3	2.1	V10	—	V05	V02
16HD8	*AmPAL16HD8	97-25	1.3	—	V10	—	V05	V02
16L2	*PAL16L2	22-16	1.54	1.5	V05	V12	V01	V01
16L6	*PAL16L6	22-03	1.54	2.3	V05	V12	V01	V01
16L8	PAL16L8-7(-12Mil)	20-17	2.7	2.5	V12	—	V05	V03
	PAL16L8H-15/D/B	30-17	2.4	2.4	V09	V13	V09	V01
	PAL16L8B-2/B-4/A/A-2/A-4	22-17	1.54	1.5	V05	V12	V01	V03
	PALC16L8Z	46-17	2.3	—	V13	—	V04	V03
	*PALC16L8Q	DB-17	2.4	—	V11	—	V04	V04
	*AmPAL16L8	97-17	1.3	1.6	V10	V12	V05	V01
16LD8	*AmPAL16LD8	97-17	1.3	—	V10	—	V05	V02
16P8	PAL16P8A	22-30	1.54	—	V05	V12	V01	V01
16R4	PAL16R4-7(-12Mil)	20-81	2.7	2.5	V12	—	V05	V03
	PAL16R4H-15	30-67	2.4	—	V11	V13	V09	V01
	PAL16R4D/B	30-24	2.4	2.4	V13	V13	V09	V04
	PAL16R4B-2/B-4/A/A-2/A-4	22-24	1.54	1.5	V05	V12	V01	V03
	PALC16R4Z	46-24	2.3	—	V13	—	V04	V03
	*PALC16R4Q	DB-24	2.4	—	V11	—	V04	V04
	*AmPAL16R4	97-81	1.3	2.1	V10	V12	V05	V01
16R6	PAL16R6-7(-12Mil)	20-80	2.7	2.5	V12	—	V05	V03
	PAL16R6H-15	30-67	2.4	—	V11	V13	V09	V01
	PAL16R6D/B	30-24	2.4	2.4	V13	V13	V09	V04
	PAL16R6B-2/B-4/A/A-2/A-4	22-24	1.54	1.5	V05	V12	V01	V03
	PALC16R6Z	46-24	2.3	—	V13	—	V04	V03
	*PALC16R6Q	DB-24	2.4	—	V11	—	V04	V04
	*AmPAL16R6	97-80	1.3	2.1	V10	V12	V05	V01
16R8	PAL16R8-7(-12Mil)	20-82	2.7	2.5	V12	—	V05	V03
	PAL16R8H-15	30-67	2.4	—	V11	V13	V09	V01
	PAL16R8D/B	30-24	2.4	2.4	V13	V13	V09	V04
	PAL16R8B-2/B-4/A/A-2/A-4	22-24	1.54	1.5	V05	V12	V01	V03
	PALC16R8Z	46-24	2.3	—	V13	—	V04	V03
	*PALC16R8Q	DB-24	2.4	—	V11	—	V04	V04
	*AmPAL16R8	97-82	1.3	2.1	V10	V12	V05	V01
16RA8	PAL16RA8	22-31	1.54	1.5	V05	V12	V01	V01
16RP4	PAL16RP4A	22-31	1.54	1.5	V05	V12	V01	V01

Data I/O Corporation

Archi-tecture	Part Number	Family-Pinout Code	Revision					
			UniSite 40		Model 60		Model 29A, 29B LogicPak 303A-V04	
			DIP	PLCC	DIP	PLCC	DIP 303A-011A	PLCC 303A-011B
16RP6	PAL16RP6A	22-31	1.54	1.5	V05	V12	V01	V01
16RP8	PAL16RP8A	22-31	1.54	1.5	V05	V12	V01	V01
16V8	PALCE16V8H/Q	80-55	2.5	3.0	V14.1	—	V10	V04
	16V8 as 16L8	80-17	2.6	3.0	—	—	—	—
	16V8 as 16R4	80-81	2.6	3.0	—	—	—	—
	16V8 as 16R6	80-80	2.6	3.0	—	—	—	—
	16V8 as 16R8	80-82	2.6	3.0	—	—	—	—
16X4	*PAL16X4	22-24	1.54	1.5	V05	V12	V01	V03
18L4	*PAL18L4	22-04	1.54	1.5	V05	V12	V01	V01
18P8	AmPAL18P8	97-29	1.3	1.5	V05	V12	V01	V02
18U8	*PALC18U8	DB-2E	2.2	—	V14.1	—	V04	V04
20C1	*PAL20C1	22-12	1.54	2.1	V05	V12	V01	V01
20EG8	PAL10H20EG8	22-6C	2.7	2.7	—	—	—	—
	PAL10020EG8	22-6E	2.7	2.7	—	—	—	—
20EV8	PAL10H20EV8	22-6B	2.7	2.7	—	—	—	—
	PAL10020EV8	22-6D	2.7	2.7	—	—	—	—
20G8	*PAL10H20G8	22-42	2.0	—	—	—	303A-ECL	—
20L2	*PAL20L2	22-05	1.54	1.5	V05	V12	V01	V01
20L8	PAL20L8-7(-12Mil)	20-26	2.6	2.7	—	—	—	—
	PAL20L8-10(-15Mil)/B-2	22-26	1.54	2.7	V05	V12	V01	V01
	PAL20L8B/A/A-2	22-26	1.54	2.1	V05	V12	V01	V03
	PALC20L8Z	46-26	1.54	—	V10	—	V06	V03
20L10	PAL20L10A	22-06	1.54	1.5	V05	V12	V09	V01
	AmPAL20L10	97-06	2.0	—	V10	—	V03	V04
	*PAL20L10	22-06	1.54	1.5	V05	V12	V09	V01
20P8	*PAL10H20P8	22-42	2.0	—	—	—	303A-ECL	—
20R4	PAL20R4-7(-12Mil)	20-65	2.6	2.7	—	—	—	—
	PAL20R4-10(-15Mil)/B-2	22-68	2.4	2.7	V10	V12	V04	V02
	PAL20R4B/A/A-2	22-27	1.54	1.5	V05	V12	V01	V03
	PALC20R4Z	46-27	1.54	—	V10	—	V06	V03
20R6	PAL20R6-7(-12Mil)	20-66	2.6	2.7	—	—	—	—
	PAL20R6-10(-15Mil)/B-2	22-68	2.4	2.7	V10	V12	V04	V02
	PAL20R6B/A/A-2	22-27	1.54	2.1	V05	V12	V01	V03
	PALC20R6Z	46-27	1.54	—	V10	—	V06	V03
20R8	PAL20R8-7(-12Mil)	20-68	2.6	2.7	—	—	—	—
	PAL20R8-10(-15Mil)/B-2	22-68	2.4	2.7	V10	V12	V04	V02
	PAL20R8B/A/A-2	22-27	1.54	1.5	V05	V12	V01	V03
	PALC20R8Z	46-27	1.54	—	V10	—	V06	V03
20RA10	PAL20RA10-20	22-45	1.54	2.3	V05	V12	V08	—
	PAL20RA10	22-45	1.54	1.5	V05	V12	V09	—
	*PALCE20RA10Z	DE-45	2.3	—	—	—	V06	—
20RS4	*PAL20RS4	22-46	1.54	2.0	V05	V12	V01	V01
20RS8	*PAL20RS8	22-45	1.54	2.3	V05	V12	V01	V01
20RS10	*PAL20RS10	22-44	1.54	2.0	V05	V12	V01	V01
20S10	*PAL20S10	22-43	1.54	1.5	V05	V12	V01	V01

Data I/O Corporation

Archi-tecture	Part Number	Family-Pinout Code	Revision					
			UniSite 40		Model 60		Model 29A, 29B LogicPak 303A-V04	
			DIP	PLCC	DIP	PLCC	DIP 303A-011A	PLCC 303A-011B
20V8	PALCE20V8H	80-57	2.7	—	—	—	—	—
	PAL20V8 as 20L8	80-26	2.7	—	—	—	—	—
	PAL20V8 as 20R4	80-65	2.7	—	—	—	—	—
	PAL20V8 as 20R6	80-66	2.7	—	—	—	—	—
	PAL20V8 as 20R8	80-27	2.7	—	—	—	—	—
20X4	PAL20X4A	22-36	1.54	1.7	V05	V12	V09	V04
	*PAL20X4	22-23	1.54	1.7	V05	V12	V09	V04
20X8	PAL20X8A	22-36	1.54	1.7	V05	V12	V09	V04
	*PAL20X8	22-23	1.54	1.7	V05	V12	V09	V04
20X10	PAL20X10A	22-36	1.54	1.7	V05	V12	V09	V04
	*PAL20X10	22-23	1.54	1.7	V05	V12	V09	V04
22IP6	PAL22IP6-25	22-6A	3.0	—	—	—	—	—
22P10	*AmPAL22P10	97-2B	2.0	—	V10	—	V03	V04
22V10	PAL22V10, AmPAL22V10	97-28	1.3	2.0	V03	V12	V01	V01
	PALCE22V10	80-28	3.0	—	—	—	—	—
	*PALC22V10	DB-28	2.3	—	V12	—	V09	V04
23S8	AmPAL23S8	97-84	2.0	—	V11	—	V04	—
26V12	PALCE26V12	80-4E	2.5	—	—	—	V10	—
29M16	PALCE29M16	60-4B	2.5	—	V10	—	V03	—
29MA16	PALCE29MA16	60-4C	2.4	—	V10	—	V03	—
32VX10	PAL32VX10	22-77	1.54	—	V10	V13	V01	V01
6L16	*PAL6L16A	22-48	1.54	2.2	V05	V12	V01	V01
8L14	*PAL8L14A	22-49	1.54	2.3	V05	V12	V01	V01
105	PLS105	2A-63	2.2	2.2	V11	—	V04	V03
167	PLS167	2A-60	2.2	—	V11	—	V04	V03
168	PLS168	2A-74	2.2	—	V11	—	V04	V03
30S16	PLS30S16	97-A9	2.6	—	—	—	—	—
141	*Am29PL141	97-79	1.5	—	—	—	303A-FPC-V01	—
	*Am29LPL141	97-79	1.5	—	—	—	303A-FPC-V01	—
142	*Am29PL142	97-76	2.0	—	—	—	303A-FPC-V02	—
151	Am29CPL151	94-70	—	—	—	—	V08	—
154	Am29CPL154	94-7E	2.4	—	—	—	V10	—
14R21	*PMS14R21	22-58	2.4	—	—	—	V10	V03
2971	Am2971	97-78	1.55	—	—	—	—	—
1736	Am1736	127-EE	2.6	—	—	—	—	—

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

PLCC support is for standard pinout in data sheet. For non-standard pinouts or other packages, contact Data I/O Corporation or AMD.

Digelec, Inc.
22736 Vanowen Street
Canoga Park, CA 91307
(800) 367-8750 or (818) 887-3755

System UP 803
Model 860

Archi-tecture	Part Number	Revision: System UP 803 Logic Center FAM 52	Adapter	Rev.	Revision: Model 860
10H8	*PAL10H8	5.4	DA 53	A-3	A1.2
10L8	*PAL10L8	5.4	DA 53	A-3	A1.2
12H6	*PAL12H6	5.4	DA 53	A-3	A1.2
12L6	*PAL12L6	5.4	DA 53	A-3	A1.2
12L10	*PAL12L10	5.4	DA 55	C-1	A1.2
14H4	*PAL14H4	5.4	DA 53	A-3	A1.2
14L4	*PAL14L4	5.4	DA 53	A-3	A1.2
14L8	*PAL14L8	5.4	DA 55	C-1	A1.2
16C1	*PAL16C1	5.4	DA 53	A-3	A1.2
16H2	*PAL16H2	5.4	DA 53	A-3	A1.2
16H8	*AmPAL16H8	5.5	DA 53	A-3	A1.2
16HD8	*AmPAL16HD8	5.5	DA 53	A-3	A1.2
16L2	*PAL16L2	5.4	DA 53	A-3	A1.2
16L6	*PAL16L6	5.4	DA 55	C-1	A1.2
16L8	PAL16L8H-15/D/B	5.4	DA 53	A-3	A1.2
	PAL16L8/B-2/B-4/A/A-2/A-4	5.4	DA 53	A-3	A1.2
	*PALC16L8Q	—	—	—	A1.2
	*AmPAL16L8	5.5	DA 53	A-3	A1.2
16LD8	*AmPAL16LD8	5.5	DA 53	A-3	A1.2
16P8	PAL16P8A	5.4	DA 53	A-3	A1.2
16R4	PAL16R4H-15	5.4	DA 53	C-1	A1.2
	PAL16R4D/B	5.4	DA 53	A-3	A1.2
	PAL16R4/B-2/B-4/A/A-2/A-4	5.4	DA 53	A-3	A1.2
	*PALC16R4Q	—	—	—	A1.2
	*AmPAL16R4	5.5	DA 53	A-3	A1.2
16R6	PAL16R6H-15	5.4	DA 53	C-1	A1.2
	PAL16R6D/B	5.4	DA 53	A-3	A1.2
	PAL16R6/B-2/B-4/A/A-2/A-4	5.4	DA 53	A-3	A1.2
	*PALC16R6Q	—	—	—	A1.2
	*AmPAL16R6	5.5	DA 53	A-3	A1.2
16R8	PAL16R8H-15	5.4	DA 53	C-1	A1.2
	PAL16R8D/B	5.4	DA 53	A-3	A1.2
	PAL16R8/B-2/B-4/A/A-2/A-4	5.4	DA 53	A-3	A1.2
	*PALC16R8Q	—	—	—	A1.2
	*AmPAL16R8	5.5	DA 53	A-3	A1.2
16RA8	PAL16RA8	5.4	DA 53	C-1	A1.2
16RP4	PAL16RP4A	5.4	DA 53	A-3	A1.2
16RP6	PAL16RP6A	5.4	DA 53	A-3	A1.2
16RP8	PAL16RP8A	5.4	DA 53	A-3	A1.2
16V8	PALCE16V8H/Q	—	—	—	A1.4
16X4	*PAL16X4	5.4	DA 53	A-3	A1.2
18L4	*PAL18L4	5.4	DA 55	C-1	A1.2
18P8	AmPAL18P8	5.5	DA 55	B-3	A1.2
20C1	*PAL20C1	5.4	DA 55	C-1	A1.2

Digelec, Inc.

Architecture	Part Number	Revision			
		System UP 803			
		Logic Center FAM 52	Adapter	Rev.	Model 860
20G8	*PAL10H20G8	5.4	DA 60	A-1	—
20L2	*PAL20L2	5.4	DA 55	C-1	A1.2
20L8	PAL20L8-10(-15Mil)/B-2	5.4	DA 55	C-1	A1.2
	PAL20L8B/A/A-2	5.4	DA 55	C-1	A1.2
	PALC20L8Z	5.4	DA 55	C-1	A1.2
20L10	PAL20L10A	5.4	DA 55	C-1	A1.2
	AmPAL20L10	5.5	DA 53	A-3	A1.2
	*PAL20L10	5.4	DA 55	C-1	A1.2
20P8	*PAL10H20P8	5.4	DA 60	A-1	—
20R4	PAL20R4-10(-15Mil)/B-2	5.4	DA 55	C-1	A1.2
	PAL20R4B/A/A-2	5.4	DA 55	C-1	A1.2
	PALC20R4Z	5.4	DA 55	C-1	A1.2
20R6	PAL20R6-10(-15Mil)/B-2	5.4	DA 55	C-1	A1.2
	PAL20R6B/A/A-2	5.4	DA 55	C-1	A1.2
	PALC20R6Z	5.4	DA 55	C-1	A1.2
20R8	PAL20R8-10(-15Mil)/B-2	5.4	DA 55	C-1	A1.2
	PAL20R8B/A/A-2	5.4	DA 55	C-1	A1.2
	PALC20R8Z	5.4	DA 55	C-1	A1.2
20RA10	PAL20RA10	5.4	DA 55	C-1	A1.2
	PAL20RA10-20	5.4	DA 55	C-1	A1.2
20RS4	*PAL20RS4	5.4	DA 55	C-1	A1.2
20RS8	*PAL20RS8	5.4	DA 55	C-1	A1.2
20RS10	*PAL20RS10	5.4	DA 55	C-1	A1.2
20S10	*PAL20S10	5.4	DA 55	C-1	A1.2
20X4	PAL20X4A	5.4	DA 55	C-1	A1.2
	*PAL20X4	5.4	DA 55	C-1	A1.2
20X8	PAL20X8A	5.4	DA 55	C-1	A1.2
	*PAL20X8	5.4	DA 55	C-1	A1.2
20X10	PAL20X10A	5.4	DA 55	C-1	A1.2
	*PAL20X10	5.4	DA 55	C-1	A1.2
22P10	*AmPAL22P10	5.5	DA 53	A-3	A1.2
22V10	PAL22V10, AmPAL22V10	5.5	DA 55	B-3	A1.2
	*PALC22V10	—	—	—	A1.2
32VX10	PAL32VX10	6.54	DA 55	C-1	A1.2
6L16	*PAL6L16A	6.54	DA 62	—	A1.2
8L14	*PAL8L14A	6.54	DA 62	—	A1.2
141	*Am29PL141	—	—	—	A1.1

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

PLCC support is for standard pinout in data sheet. For non-standard pinouts or other packages, contact Digelec or AMD.

Kontron Electronics
630 Clyde Ave.
Mountain View, CA 94039-7230
(800) 227-8834 or (415) 965-7020

System MPP 80S
System EPP-80

Architecture	Part Number	Revision	
		System MPP 80S Module MOD 21 Adapter	System EPP-80 Module UPM-B
10H8	*PAL10H8	SA-27	1.44
10L8	*PAL10L8	SA-27	1.44
12H6	*PAL12H6	SA-27	1.44
12L6	*PAL12L6	SA-27	1.44
12L10	*PAL12L10	SA-27-1	1.44
14H4	*PAL14H4	SA-27	1.44
14L4	*PAL14L4	SA-27	1.44
14L8	*PAL14L8	SA-27-1	1.44
16C1	*PAL16C1	SA-27	1.44
16H2	*PAL16H2	SA-27	1.44
16H8	*AmPAL16H8	SA-27	1.45
16HD8	*AmPAL16HD8	SA-27	1.45
16L2	*PAL16L2	SA-27	1.44
16L6	*PAL16L6	SA-27-1	1.44
16L8	PAL16L8H-15/D/B PAL16L8/B-2/B-4/A/A-2/A-4 *AmPAL16L8	— SA-27 SA-27	1.44 1.44 1.45
16LD8	*AmPAL16LD8	SA-27	1.45
16P8	PAL16P8A	—	1.44
16R4	PAL16R4H-15 PAL16R4D/B PAL16R4/B-2/B-4/A/A-2/A-4 *AmPAL16R4	— — SA-27 SA-27	1.44 1.44 1.44 1.45
16R6	PAL16R6H-15 PAL16R6D/B PAL16R6/B-2/B-4/A/A-2/A-4 *AmPAL16R6	— — SA-27 SA-27	1.44 1.44 1.44 1.45
16R8	PAL16R8H-15 PAL16R8D/B PAL16R8/B-2/B-4/A/A-2/A-4 *AmPAL16R8	— — SA-27 SA-27	1.44 1.44 1.44 1.45
16RA8	PAL16RA8	—	1.47
16RP4	PAL16RP4A	—	1.44
16RP6	PAL16RP6A	—	1.44
16RP8	PAL16RP8A	—	1.44
16X4	*PAL16X4	SA-27	1.44
18L4	*PAL18L4	SA-27-1	1.44
18P8	AmPAL18P8	—	1.45
20C1	*PAL20C1	SA-27-1	1.44
20G8	*PAL10H20G8	—	1.47
20L2	*PAL20L2	SA-27-1	1.44
20L8	PAL20L8-10(-15Mil)/B-2 PAL20L8B/A/A-2 PALC20L8Z	SA-27-1 SA-27-1 —	1.44 1.44 2.00

Kontron Electronics

Archi-tecture	Part Number	Revision: System MPP 80S Module MOD 21 Adapter	Revision: System EPP-80 Module UPM-B
20L10	PAL20L10A	SA-27-1	1.44
	*PAL20L10	SA-27-1	1.44
20P8	*PAL10H20P8	—	1.47
20R4	PAL20R4-10(-15Mil)/B-2	SA-27-1	1.44
	PAL20R4B/A/A-2	SA-27-1	1.44
	PALC20R4Z	—	2.00
20R6	PAL20R6-10(-15Mil)/B-2	SA-27-1	1.44
	PAL20R6B/A/A-2	SA-27-1	1.44
	PALC20R6Z	—	2.00
20R8	PAL20R8-10(-15Mil)/B-2	SA-27-1	1.44
	PAL20R8B/A/A-2	SA-27-1	1.44
	PALC20R8Z	—	2.00
20RA10	PAL20RA10	—	1.44
	PAL20RA10-20	—	1.44
20RS4	*PAL20RS4	—	1.44
20RS8	*PAL20RS8	—	1.44
20RS10	*PAL20RS10	—	1.44
20S10	*PAL20S10	—	1.44
20X4	PAL20X4A	SA-27-1	1.44
	*PAL20X4	SA-27-1	1.44
20X8	PAL20X8A	SA-27-1	1.44
	*PAL20X8	SA-27-1	1.44
20X10	PAL20X10A	SA-27-1	1.44
	*PAL20X10	SA-27-1	1.44
22V10	PAL22V10, AmPAL22V10	—	1.45
	*PALC22V10	—	2.00
32VX10	PAL32VX10	—	2.00
6L16	*PAL6L16A	—	2.00
8L14	*PAL8L14A	—	2.00

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

Logical Devices, Inc.
1201 E. Northwest 65th Place
Fort Lauderdale, FL 33309
(800) 331-7766 or (305) 491-7405

ALLPRO™ Programmer

Architecture	Part Number	ALLPRO Revision
10H8	*PAL10H8	1.44CR2
10L8	*PAL10L8	1.44CR2
12H6	*PAL12H6	1.44CR2
12L6	*PAL12L6	1.44CR2
12L10	*PAL12L10	1.44CR2
14H4	*PAL14H4	1.44CR2
14L4	*PAL14L4	1.44CR2
14L8	*PAL14L8	1.44CR2
16C1	*PAL16C1	1.44CR2
16H2	*PAL16H2	1.44CR2
16H8	*AmPAL16H8	1.44CR2
16HD8	*AmPAL16HD8	1.44CR2
16L2	*PAL16L2	1.44CR2
16L6	*PAL16L6	1.44CR2
16L8	PAL16L88-7(-12Mil) PAL16L8H-15/D/B PAL16L8/B-2/B-4/A/A-2/A-4 *PALC16L8Q *AmPAL16L8	1.48C 1.44CR2 1.44CR2 1.48C 1.44CR2
16LD8	*AmPAL16LD8	1.44CR2
16P8	PAL16P8A	1.44CR2
16R4	PAL16R4-7(-12Mil) PAL16R4H-15 PAL16R4D/B PAL16R4/B-2/B-4/A/A-2/A-4 *PALC16R4Q *AmPAL16R4	1.48C 1.44CR2 1.44CR2 1.44CR2 1.48C 1.44CR2
16R6	PAL16R6-7(-12Mil) PAL16R6H-15 PAL16R6D/B PAL16R6/B-2/B-4/A/A-2/A-4 PALC16R6Q *AmPAL16R6	1.48C 1.44CR2 1.44CR2 1.44CR2 1.48C 1.44CR2
16R8	PAL16R8-7(-12Mil) PAL16R8H-15 PAL16R8D/B PAL16R8/B-2/B-4/A/A-2/A-4 *PALC16R8Q *AmPAL16R8	1.48C 1.44CR2 1.44CR2 1.44CR2 1.48C 1.44CR2

Architecture	Part Number	ALLPRO Revision
16RA8	PAL16RA8	1.44CR2
16RP4	PAL16RP4A	1.44CR2
16RP6	PAL16RP6A	1.44CR2
16RP8	PAL16RP8A	1.44CR2
16X4	*PAL16X4	1.44CR2
18L4	*PAL18L4	1.44CR2
18P8	AmPAL18P8	1.48C
18U8	*PALC18U8	1.48C
20C1	*PAL20C1	1.44CR2
20L2	*PAL20L2	1.44CR2
20L8	PAL20L8-10(-15Mil)/B-2 PAL20L8B/A/A-2 PALC20L8Z	1.44CR2 1.44CR2 1.44CR2
20L10	PAL20L10A AmPAL20L10 *PAL20L10	1.44CR2 1.48C 1.44CR2
20R4	PAL20R4-10(-15Mil)/B-2 PAL20R4B/A/A-2 PALC20R4Z	1.44CR2 1.44CR2 1.44CR2
20R6	PAL20R6-10(-15Mil)/B-2 PAL20R6B/A/A-2 PALC20R6Z	1.44CR2 1.44CR2 1.44CR2
20R8	PAL20R8-10(-15Mil)/B-2 PAL20R8B/A/A-2 PALC20R8Z	1.44CR2 1.44CR2 1.44CR2
20RA10	PAL20RA10 PAL20RA10-20 *PALCE20RA10Z	1.44CR2 1.44CR2 1.48C
20RS4	*PAL20RS4	1.44CR2
20RS8	*PAL20RS8	1.44CR2
20RS10	*PAL20RS10	1.44CR2
20S10	*PAL20S10	1.44CR2
20X4	PAL20X4A *PAL20X4	1.44CR2 1.44CR2
20X8	PAL20X8A *PAL20X8	1.44CR2 1.44CR2
20X10	PAL20X10A *PAL20X10	1.44CR2 1.44CR2

Logical Devices, Inc.

Architecture	Part Number	ALLPRO Revision
22P10	*AmPAL22P10	1.48C
22V10	PAL22V10, AmPAL22V10 *PALC22V10	1.48C 1.48C
23S8	AmPAL23S8	1.48C
26V12	PALCE26V12	1.48C
29M16	PALCE29M16	1.48C
29MA16	PALCE29MA16	1.48C
32VX10	PAL32VX10	1.44CR2
6L16	*PAL6L16A	1.44CR2
8L14	*PAL8L14A	1.44CR2
141	*Am29PL141 *Am29LPL141	1.48C 1.48C
142	*Am29PL142	1.48C
151	Am29CPL151	1.48C
154	Am29CPL154	1.48C
2971	Am2971	1.48C

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

Microprоss
Parc d'Activite des Pres
5, rue Denis-Papin
59650 Villeneuve d'Ascq
France
20 47 90 20

ROM 5000 Programmer
ROM 3000 Programmer

Architecture	Part Number	Revision	
		ROM 5000	ROM 3000
10H8	*PAL10H8	3.5	5.83
10L8	*PAL10L8	3.5	5.83
12H6	*PAL12H6	3.5	5.83
12L6	*PAL12L6	3.5	5.83
12L10	*PAL12L10	3.5	5.83
14H4	*PAL14H4	3.5	5.83
14L4	*PAL14L4	3.5	5.83
14L8	*PAL14L8	3.5	5.83
16C1	*PAL16C1	3.5	5.83
16H2	*PAL16H2	3.5	5.83
16H8	*AmPAL16H8	—	5.83
16HD8	*AmPAL16HD8	—	5.83
16L2	*PAL16L2	3.5	5.83
16L6	*PAL16L6	3.5	5.83
16L8	PAL16L8-7(-12Mil)	—	5.83
	PAL16L8H-15	3.5	5.83
	PAL16L8D/B	3.5	5.83
	PAL16L8/B-2/B-4/A/A-2/A-4	3.5	5.83
	*PALC16L8Q	—	5.83
	*AmPAL16L8	3.5	5.83
16LD8	*AmPAL16LD8	—	5.83
16P8	PAL16P8A	3.5	5.83
16R4	PAL16R4-7(-12Mil)	—	5.83
	PAL16R4H-15	3.5	5.83
	PAL16R4D/B	3.5	5.83
	PAL16R4/B-2/B-4/A/A-2/A-4	3.5	5.83
	*PALC16R4Q	—	5.83
	*AmPAL16R4	3.5	5.83
16R6	PAL16R6-7(-12Mil)	—	5.83
	PAL16R6H-15	3.5	5.83
	PAL16R6D/B	3.5	5.83
	PAL16R6/B-2/B-4/A/A-2/A-4	3.5	5.83
	*PALC16R6Q	—	5.83
	*AmPAL16R6	3.5	5.83
16R8	PAL16R8-7(-12Mil)	—	5.83
	PAL16R8H-15	3.5	5.83
	PAL16R8D/B	3.5	5.83
	PAL16R8/B-2/B-4/A/A-2/A-4	3.5	5.83
	*PALC16R8Q	—	5.83
	*AmPAL16R8	3.5	5.83
16RA8	PAL16RA8	4.6	5.83
16RP4	PAL16RP4A	3.5	5.83
16RP6	PAL16RP6A	3.5	5.83
16RP8	PAL16RP8A	3.5	5.83
16X4	*PAL16X4	3.5	5.83
18L4	*PAL18L4	3.5	5.83

Microprocess

Archi-tecture	Part Number	Revision	
		ROM 5000	ROM 3000
18P8	AmPAL18P8	—	5.83
18U8	*PALC18U8	—	5.83
20C1	*PAL20C1	3.5	5.83
20G8	*PAL10H20G8	4.6	5.83
20L2	*PAL20L2	3.5	5.83
20L8	PAL20L8-10(-15Mil)/B-2	3.5	5.83
	PAL20L8B/A/A-2	3.5	5.83
	PALC20L8Z	—	5.83
20L10	PAL20L10A	3.5	5.83
	AmPAL20L10	—	5.83
	*PAL20L10	3.5	5.83
20P8	*PAL10H20P8	4.6	5.83
20R4	PAL20R4-10(-15Mil)/B-2	3.5	5.83
	PAL20R4B/A/A-2	3.5	5.83
	PALC20R4Z	—	5.83
20R6	PAL20R6-10(-15Mil)/B-2	3.5	5.83
	PAL20R6B/A/A-2	3.5	5.83
	PALC20R6Z	—	5.83
20R8	PAL20R8-10(-15Mil)/B-2	3.5	5.83
	PAL20R8B/A/A-2	3.5	5.83
	PALC20R8Z	—	5.83
20RA10	PAL20RA10	3.5	5.83
	PAL20RA10-20	3.5	5.83
	*PALCE20RA10Z	—	5.83
20RS4	*PAL20RS4	3.5	5.83
20RS8	*PAL20RS8	3.5	5.83
20RS10	*PAL20RS10	3.5	5.83
20S10	*PAL20S10	3.5	5.83
20X4	PAL20X4A	3.5	5.83
	*PAL20X4	3.5	5.83
20X8	PAL20X8A	3.5	5.83
	*PAL20X8	3.5	5.83
20X10	PAL20X10A	3.5	5.83
	*PAL20X10	3.5	5.83
22IP6	PAL22IP6-25	—	5.83
22P10	*AmPAL22P10	—	5.83
22V10	PAL22V10, AmPAL22V10	—	5.83
	*PALC22V10	4.6	5.83
23S8	AmPAL23S8	—	5.83
29M16	PALCE29M16	—	5.83
29MA16	PALCE29MA16	—	5.83
32VX10	PAL32VX10	4.51	5.83

Microprocess

Architecture	Part Number	Revision	
		ROM 5000	ROM 3000
6L16	*PAL6L16A	4.6	5.83
8L14	*PAL8L14A	4.6	5.83
105	PLS105	—	5.83
167	PLS167	—	5.83
168	PLS168	—	5.83
141	*Am29PL141	—	5.83
142	*Am29PL142	—	5.83
151	Am29CPL151	—	5.83
14R21	*PMS14R21	—	5.83

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

Stag Microsystems
1600 Wyatt Drive
Suite 3
Santa Clara, CA 95054
(408) 988-1118

ZL30 Programmer
PPZ Module Zm2200 Programmer

Architecture	Part Number	Family-Pinout Code	Revision	
			ZL30	PPZ Module Zm2200
10H8	*PAL10H8	20-20	30A01	14
10L8	*PAL10L8	20-25	30A01	14
12H6	*PAL12H6	20-21	30A01	14
12L6	*PAL12L6	20-26	30A01	14
12L10	*PAL12L10	21-50	30A01	14
14H4	*PAL14H4	20-22	30A01	14
14L4	*PAL14L4	20-27	30A01	14
14L8	*PAL14L8	21-51	30A01	14
16C1	*PAL16C1	20-24	30A01	14
16H2	*PAL16H2	20-23	30A01	14
16H8	*AmPAL16H8	90-35	30A27	18
16HD8	*AmPAL16HD8	90-37	30A27	18
16L2	*PAL16L2	20-28	30A01	14
16L6	*PAL16L6	21-52	30A01	12
16L8	PAL16L8-7(-12Mil)	95933	30A31	37
	PAL16L8H-15/D/B	22-29	30A10	12
	PAL16L8/B-2/B-4/A/A-2/A-4	20-29	30A01	14
	PALC16L8Z	25-29	30A31	—
	*PALC16L8Q	24-29	30A29	36
	*AmPAL16L8	90-29	30A27	18
16LD8	*AmPAL16LD8	90-36	30A27	18
16P8	PAL16P8A	20-38	30A01	15
16R4	PAL16R4-7(-12Mil)	95932	30A31	37
	PAL16R4H-15	22932	30A15	12
	PAL16R4D/B	22-32	30A10	12
	PAL16R4/B-2/B-4/A/A-2/A-4	20-32	30A01	14
	PALC16R4Z	25-32	30A31	—
	*PALC16R4Q	24-32	30A29	36
	*AmPAL16R4	90-32	30A27	18
16R6	PAL16R6-7(-12Mil)	95931	30A31	37
	PAL16R6H-15	22931	30A15	12
	PAL16R6D/B	22-31	30A10	12
	PAL16R6/B-2/B-4/A/A-2/A-4	20-31	30A01	14
	PALC16R6Z	25-31	30A31	—
	*PALC16R6Q	24-31	30A29	36
	*AmPAL16R6	90-31	30A27	18
16R8	PAL16R8-7(-12Mil)	95930	30A31	37
	PAL16R8H-15	22930	30A15	12
	PAL16R8D/B	22-30	30A10	12
	PAL16R8/B-2/B-4/A/A-2/A-4	20-30	30A01	14
	PALC16R8Z	25-30	30A31	—
	*PALC16R8Q	24-30	30A29	36
	*AmPAL16R8	90-30	30A27	18
16RA8	PAL16RA8	20-19	30A10	36
16RP4	PAL16RP4A	20-13	30A01	15
16RP6	PAL16RP6A	20-12	30A01	15

Stag Microsystems

Archi-tecture	Part Number	Family-Pinout Code	Revision	
			ZL30	PPZ Module Zm2200
16RP8	PAL16RP8A	20-11	30A01	15
16V8	PALCE16V8H/Q	95009	30A35	—
	16V8 as 10H8	95020	30A35	—
	16V8 as 10L8	95025	30A35	—
	16V8 as 12H6	95021	30A35	—
	16V8 as 12L6	95026	30A35	—
	16V8 as 14H4	95022	30A35	—
	16V8 as 14L4	95027	30A35	—
	16V8 as 16H2	95023	30A35	—
	16V8 as 16H8	95035	30A35	—
	16V8 as 16L2	95028	30A35	—
	16V8 as 16L8	95029	30A35	—
	16V8 as 16P8	95038	30A35	—
	16V8 as 16R4	95032	30A35	—
	16V8 as 16R6	95031	30A35	—
	16V8 as 16R8	95030	30A35	—
	16V8 as 16RP4	95013	30A35	—
	16V8 as 16RP6	95012	30A35	—
	16V8 as 16RP8	95011	30A35	—
16X4	*PAL16X4	20-33	30A01	14
18L4	*PAL18L4	21-53	30A01	12
18P8	AmPAL18P8	90-10	30A31	18
18U8	*PALC18U8	24193	30A32	37
20C1	*PAL20C1	21-55	30A01	12
20L2	*PAL20L2	21-54	30A01	12
20L8	PAL20L8-7(-12Mil)	95-56	30A05	—
	PAL20L8-10(-15Mil)/B-2	21-56	30A32	12
	PAL20L8B/A/A-2	21-56	30A01	12
	PALC20L8Z	24-56	30A30	33
20L10	PAL20L10A	21-60	30A01	36
	AmPAL20L10	91-60	30A21	33
	*PAL20L10	21-60	30A01	36
20R4	PAL20R4-7(-12Mil)	95-59	30A05	—
	PAL20R4-10(-15Mil)/B-2	21-59	30A32	12
	PAL20R4B/A/A-2	21-59	30A01	12
	PALC20R4Z	24-59	30A30	33
20R6	PAL20R6-7(-12Mil)	95-58	30A05	—
	PAL20R6-10(-15Mil)/B-2	21-58	30A32	12
	PAL20R6B/A/A-2	21-58	30A01	12
	PALC20R6Z	24-58	30A30	33
20R8	PAL20R8-7(-12Mil)	95-57	30A05	—
	PAL20R8-10(-15Mil)/B-2	21-57	30A32	12
	PAL20R8B/A/A-2	21-57	30A01	12
	PALC20R8Z	24-57	30A30	33
20RA10	PAL20RA10	21-77	30A10	36
	PAL20RA10-20	21-77	30A10	36
	*PALCE20RA10Z	25-57	30A32	—

Stag Microsystems

Archi-tecture	Part Number	Family-Pinout Code	Revision	
			ZL30	PPZ Module Zm2200
20RS4	*PAL20RS4	21-78	30A01	26
20RS8	*PAL20RS8	21-79	30A01	26
20RS10	*PAL20RS10	21-80	30A01	26
20S10	*PAL20S10	21-81	30A01	26
20V8	PALCE20V8H	94069	30A35	—
	20V8 as 14L8	94051	30A35	—
	20V8 as 16L6	94052	30A35	—
	20V8 as 18L4	94053	30A35	—
	20V8 as 20L2	94054	30A35	—
	20V8 as 20L8	94056	30A35	—
	20V8 as 20R4	94059	30A35	—
	20V8 as 20R6	94058	30A35	—
	20V8 as 20R8	94057	30A35	—
20X4	PAL20X4A	21-63	30A01	36
	*PAL20X4	21-63	30A01	36
20X8	PAL20X8A	21-62	30A01	36
	*PAL20X8	21-62	30A01	36
20X10	PAL20X10A	21-61	30A01	36
	*PAL20X10	21-61	30A01	36
22P10	*AmPAL22P10	91121	30A21	33
22V10	PAL22V10, AmPAL22V10	91-70	30A31	35
	*PALC22V10	24070	30A26	33
23S8	AmPAL23S8	90128	30A26	36
29M16	PALCE29M16	94135	—	37
29MA16	PALCE29MA16	94136	—	37
32VX10	PAL32VX10	21-66	30A27	23
105	PLS105	21-02	30A29	37
167	PLS167	21-91	30A29	37
168	PLS168	21-97	30A29	37
141	*Am29PL141	92-92	—	20
14R21	*PMS14R21	21139	30A22	28

Notes:

* Not recommended for new designs – contact AMD for replacement device information.

(-XXMil) = Military suffix.

If part number has no performance suffix, information applies to all options.

Earliest revision shown. Later revisions also can be assumed to support these products.

PLCC support is for standard pinout in data sheet. For non-standard pinouts or other packages, contact Stag Microsystems or AMD.

TESTPRO CERTIFICATION MEANS:

- AMD-written procedures
- AMD-trained operators
- ESD-protected facilities
- Programming on AMD-approved Data I/O programmers
- Functional testing on a proprietary AutoVec™ 2850 tester from Exatron
- Regular quality audits by AMD

If you buy programmable array logic (PAL®) devices in volume through distribution, you already know about AMD, and it's a good bet that our outstanding ICs have played a part in the success of your products. Now we have something new called TestPro.

The AMD TestPro Centers for distributors represent more than continuing excellence from the world's largest supplier of programmable products. TestPro is a comprehensive system for delivering factory-quality devices to you.

TestPro provides a dramatic increase in PAL device quality. You'll decrease manufacturing costs. Fewer device failures will mean lower system rework costs, and TestPro ICs can be incorporated into your systems with a minimum of handling and a maximum of confidence.

Why Functional Testing Is Important

AMD invented the PAL device in 1978, and engineered key enhancements. Distributor TestPro Centers represent a synthesis of the techniques and expertise in programming, testing and handling that have become our mainstay in supplying thousands of customers with tens of millions of superior devices.

PAL devices have three main components: the fuse array, programming and verification circuitry, and functional circuitry.

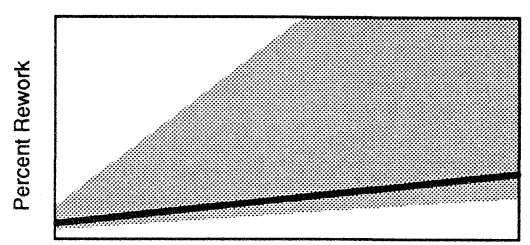
The fuse array contains device logic and is programmed through the programming circuitry. Then the pattern in the fuse array is checked via the verification circuitry. Functional circuitry is used in the actual device operation.

The programming and verification circuitry are thoroughly tested prior to shipment from the factory by a combination of opening test fuses or exercising every fuse. In addition, much design and testing effort goes into functionally testing each PAL device prior to shipment. Since there is almost an infinite number of logic combinations that can be chosen for your logic, "complete" functional verification is impractical. As a result, a small percentage of PAL devices that pass array verification when you program them can still be non-functional. These devices are called post-programming functional rejects. Although small in number, these rejects can turn into board-level rejects unless they are identified and removed.

One way to verify the functionality of PAL devices is to generate and use test vectors, but the quality of the resulting testing is dependent on the quality of these "engineered" vectors. As an alternative, AMD, in cooperation with Exatron and Data I/O, has created a better solution. The result is a sophisticated programming and test system that utilizes a Data I/O 60H programmer in concert with an Exatron Autovec tester.

Immediately after the Data I/O 60H programs each part, the Exatron Autovec exercises it with a million-plus pseudo random vectors. AutoVec testing is as consistent and effective as the best of engineered vectors and more cost-effective.

Percent Board Rework vs Number of Devices Per Board



Testing quality using engineered vectors varies according to the thoroughness of the vectors.

AutoVec

AMD provides a 120-page TestPro operations and procedures manual that serves as a reference in operating TestPro. The manual incorporates techniques that minimize electrostatic discharge (ESD) effects, specifies certified programming steps and regulates marking and quality assurance efforts.

The AMD-approved distributor personnel assigned to TestPro facilities are expert programming center operators. In-depth training programs for these operators are backed by regular AMD site inspections and periodic retraining and recertification.

All in all, the combination of the right hardware, trained operators, effective procedures, and AMD certification allows you to eliminate the costs of programming, vector generation, testing and marking (labeling). The reduction in handling also results in fewer rejects and less mixing.

The Big Payoff

All board production can benefit from high-quality components. The more PAL devices per board and the higher the rework cost, the more benefit you will derive from TestPro quality.

Some typical numbers for the identified savings are shown below:

	User Typical Cost/Unit	TestPro Cost/Unit
Program and Test	$ .25 — 1.00[1]	$ .25 — .75[2]
Marking	$ .10 — .20	
Board Rework Cost	$ .25 — .50[1]	Negligible
Elimination of Sockets	$ .25 — .50	0
Total	$ .85 — 2.20	$ .25 — .75

Note:

[1] Depends on what kind of testing you do

[2] Depends on quantity, lot size, initiation fee, etc.

All this and you avoid the costs of misprogramming or mismarking.

Only you know what your exact situation is, but the following work sheet will help you quantify your savings.

Board Cost Savings Work Sheet

		Example	Your Numbers
Total Number of PLDs Per Board	(a)	20	_____
Total Cost of Unprogrammed Devices	(b)	$ 40	_____
Your Cost Per Unit of Programming, Testing and Marking	(c)	$ .60	_____
Component Cost if you Program	(d)=(b)+(a)(c)	$ 52	_____
Total Cost of TestPro Components	(e)	$ 47	_____
Cost Savings of TestPro Devices at the Component Level	(f)=(d)-(e)	$ 5	_____
Rework Elimination Savings (Decrease in Failure Rate Multiplied by Rework Cost)	(g)	$ 7	_____
Savings From Elimination of Sockets	(h)	$ 7	_____
Overall Savings	(f)+(g)+(h)	$ 19	_____

With TestPro PAL Devices, You Get:

- Reduced system rework costs
- Manufacturing cost savings
- Less incoming inspection due to higher quality devices

AMD TestPro Centers

ARIZONA		
	HAMILTON/AVNET—CHANDLER	(602) 961–6400
CALIFORNIA		
	ANTHEM—CHATSWORTH	(818) 700–1000
	ANTHEM—IRVINE	(714) 768–4444
	ANTHEM—SAN JOSE	(408) 453–1200
	ARROW/KIERULFF—SUNNYVALE	(408) 745–6600
	ARROW/KIERULFF—TUSTIN	(714) 838–5422
	HAMILTON/AVNET—GARDENA	(213) 217–6700
	HAMILTON/AVNET—SUNNYVALE	(408) 743–3000
	SCHWEBER—IRVINE	(714) 863–0200
	SCHWEBER—SAN JOSE	(408) 432–7171
	WYLE—SANTA CLARA	(408) 727–2500
	WYLE—IRVINE	(714) 851–9953
COLORADO		
	ANTHEM—ENGLEWOOD	(303) 790–4500
	ARROW/KIERULFF—ENGLEWOOD	(303) 790–4444
	WYLE—THORNTON	(303) 457–9953
GEORGIA		
	ARROW/KIERULFF—NORCROSS	(404) 449–8252
	SCHWEBER—NORCROSS	(404) 449–9170
KENTUCKY		
	HAMILTON/AVNET—LEXINGTON	(606) 259–1475
MASSACHUSETTS		
	ANTHEM—WILMINGTON	(508) 657–5170
	ARROW/KIERULFF—WILMINGTON	(508) 658–0900
	HAMILTON/AVNET—PEABODY	(508) 532–3701
	SCHWEBER—BEDFORD	(617) 275–5100
MINNESOTA		
	ARROW/KIERULFF—EDINA	(612) 830–1800
	SCHWEBER—EDEN PRAIRIE	(612) 941–5280
NEW YORK		
	ARROW/KIERULFF—BROOKHAVEN	(516) 924–9400
OREGON		
	ALMAC—BEAVERTON	(503) 629–8090
	ANTHEM—BEAVERTON	(503) 643–1114
TEXAS		
	ARROW/KIERULFF—CARROLLTON	(214) 380–6464
	SCHWEBER—DALLAS	(214) 247–6300
	WYLE—RICHARDSON	(214) 235–9953
CANADA		
	HAMILTON/AVNET—MISSISSAUGA	(416) 677–7432

ProPAL™ and HAL® Devices Program

ProPAL and HAL devices are programmable logic devices that are programmed, marked and functionally tested by Advanced Micro Devices. Our functional testing offers the user board-ready product at quality levels as stringent as 50 PPM, providing significant benefits in both quality and manufacturing cost savings. The ProPAL and HAL Device Program provides system manufacturers a risk free migration path from system prototype to full production with extremely high quality, board-ready devices.

ProPAL Devices

ProPAL (Programmed PAL®) devices are simply PAL devices that the factory programs and tests for you. You receive a fully functional device without having to do any programming and testing, and still have the flexibility to handle design changes easily.

HAL Devices

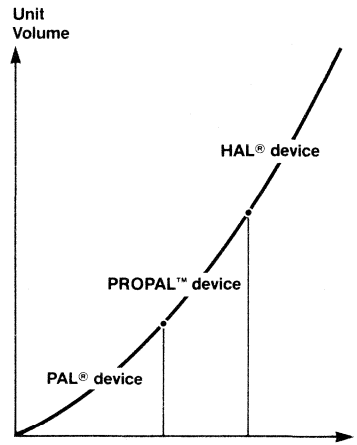
HAL (Hard Array Logic) devices are to PAL devices as ROMs are to PROMs. Instead of fuses in the logic array, your pattern is implemented using metal links that are masked in during wafer fabrication.

Should You Use a ProPAL or HAL Device?

PAL devices offer the flexibility and convenience needed for prototyping your innovative designs. They provide a means for designing an efficient system by integrating functions and saving you board space. For design, prototyping and low volume production, it makes sense to program and test your own PAL devices. You always have the option of making last minute design tweaks as you fine tune your system design.

Once your production volumes begin to ramp up to higher volumes our ProPAL and HAL device offerings provide some cost-effective alternatives.

At modest initial volumes ProPAL devices provide the best solution by eliminating the need for the customer to program and test while retaining enough flexibility to accommodate design changes. We offer two different testing options for ProPAL devices which are described below. A detailed technical description of what these testing options involve follows in the functional testing section.



Programmable Solutions

The AutoVec™ option provides a cost effective solution for low volume business (as few as 250 devices/pattern) at a typical quality level of 500-700 Parts Per Million (PPM).

When your volumes reach a moderate volume of a few thousand devices per year for each pattern, AC-functional tested ProPAL devices provide the right solution. AC-functional testing provides 50 PPM level quality. Of course the AutoVec option is available for these larger volumes, but larger volume business is usually best handled with the AC-functional testing option.

When you feel that your design has stabilized and your production volume has ramped up to several thousand devices per year, HAL devices are the most cost effective way to purchase your programmable logic. All HAL devices are fully AC-functionally tested and also have demonstrated quality levels of better than 50 PPM.

The Importance of Functional Testing

Programming is final manufacturing, and the quality of a programmed device must be verified by thorough testing. After programming, a device is "array verified." This verification checks the fuse array to verify that the pattern programmed into the device is correct. However, array verification does not guarantee functionality. Devices can pass this verification but fail in the circuit board. These are called post-programming functional rejects. Post-programming functional testing simulates

Publication #	Rev.	Amendment	Issue Date
10276	B	/0	1/90

Table 1.

Alternative	Board Level PPM	Comments
1. Fuse Verification Only	5000–10,000	Lowest quality level available. Part of standard programming sequence. No additional costs, insertions.
2. Simple Pseudo-Random Vectors	2000–3000	Gross functionality test. Relatively unsophisticated, has difficulty with complex (e.g. state machine) patterns. Simple, minimal operator expertise required.
3. Third Party Software Generated Vector Testing	1000–2000	Requires engineering time and expertise, additional equipment (usually PC–based). Uses "structured vectors" that test for possible faults – but will typically not cover all faults.
4. AutoVec Testing	500–700	Extremely sophisticated signature analysis testing. Tests almost all PLDs and possible patterns. Simple, requires minimal operator expertise.
5. AMD Full AC-Functional and Threshold Testing	50–100	Available only through the AMD factory. Highest quality testing available. Quality is a result of many years and tens of millions of units experience. All HAL devices are fully AC-functionally tested.

the actual operation of the device to verify functionality. This testing detects these functional rejects before they get into your system. The typical post-programming functional reject rate for PAL devices is about 0.5–1.0%, or 5000–10,000 PPM. Our AC-functional testing options for ProPAL and HAL devices offer 50-PPM quality levels.

Table 1 lists typical quality levels provided by the various testing alternatives available, from no functional testing to full AC-functional testing.

Alternatives (1), (2) and (3) are commercially available. The PLD user can easily purchase the equipment and/or software for these alternatives, or obtain them as value added services through distribution.

AutoVec testing, alternative (4), is available from the AMD factory or through AMD certified distributor TestPro™ centers. AMD is developing a nation-wide network of these centers to make this level of quality easily available to any PLD user who wants it.

Full AC-functional testing is available only through the AMD factory. This level of testing represents state-of-the-art testing and quality, providing the end user with near zero-defect board level quality.

ProPAL and HAL Device Functional Testing

Thorough functional testing is at the heart of our ProPAL and HAL device program. We offer a range of programming and testing options. These are discussed in detail in this section.

All functional testing of PAL devices starts with some type of test vectors, but the similarity ends there, because when it comes to functional testing of PAL devices, all vectors are not alike. They range in complexity from simple, short pseudo-random testing sequences (e.g., Data I/O's Fingerprint™ Test) to sophisticated structured vectors generated by expensive software programs used interactively by dedicated test engineers.

We offer a sophisticated brand of signature analysis testing and two types of structured vector testing. The signature analysis testing is performed on the AutoVec tester. The structured vector testing option is AC-functional vector-testing. AC-functional testing includes full functional and DC threshold testing plus functional testing for AC conditions. The following is a brief description of just what these testing options are and what they yield in final quality.

AutoVec Testing

The AutoVec tester is an extremely sophisticated signature analysis tester. It generates a sequence of up to 20 million vectors via a proprietary hardware-based pseudo-random vector generation algorithm. These vectors provide a typical quality level of 500-700 PPM for finished product.

AutoVec testing requires less engineering interaction and setup time than AC-functional testing (while still providing excellent quality levels), allowing for more flexible business conditions. These more flexible business conditions include lowered NREs and reduced minimum volume requirements.

AC-Functional Testing

The AC-functional testing option offers the highest level of quality in the ProPAL and HAL device program. This exceptional quality is a result of the increasingly sophisticated structured test vectors and test equipment used for testing.

When generating vectors for this level of testing we start with a proprietary transistor level schematic of the device under test. With this we can model internal gate level stuck-at-faults. Most other vector generation packages use inexact models — such as logic diagram representations — as the basis for vector generation. With our proprietary exact device representation it is possible to cover all possible faults of the internal gates (where these faults can occur).

AMD's Proprietary Software TGEN also checks for tri-state faulting. This is in addition to the stuck-at-1 or stuck-at-0 faulting tested for by most commercially available test packages and conventional testing methods.

Finally, TGEN is used to check the design for potential design problems (e.g., race conditions). Additional vectors are added as needed to test for these and guarantee reproducible test results.

In the process AMD test engineers interactively add vectors until 100% of the detectable faults are covered. The end result: guaranteed 90% fault coverage on every pattern we test, with typical fault coverage > 95%. If 90% fault coverage cannot be obtained, our Field Application Engineers will work with the customer to improve the testability of the design, or we will continue processing your product upon receipt of a waiver.

At this point the vectors provide coverage for DC-functional conditions. The functional testing coverage is now extended to AC testing. AMD test engineers, working with additional proprietary in-house "intelligent" software, use these vectors as the basis for generating their AC test vectors. For high quality AC testing, the design must be considered. Multiple feedback paths must be accounted for in the testing sequence. These "intelligent" software packages "learn" the design and flag the test engineer when special AC testing considerations are found. In this iterative process the engineer adds vectors to cover AC testing conditions. Typically, the number of DC functional vectors is doubled or tripled for full AC testing coverage. This expanded set of vectors is incorporated into a test program that does DC testing, functional, threshold-functional and AC-functional all at the VCC extremes. The end result is excellent system level quality with a board level reject rate less than 50 PPM.

Quality and Cost Savings

The quality and cost savings benefits the ProPAL and HAL device program offers are substantial. The investment the PAL device user makes in ProPAL and HAL devices yields a significant return in product quality and manufacturing savings.

The quality is a result of our many years and millions of units of experience in the design, manufacture, programming and testing of PAL devices. This experience lets us provide PAL device users finished quality levels as stringent as 50 PPM.

PERCENT OF SYSTEMS FAILING
vs NUMBER OF DEVICES/SYSTEM, PPM

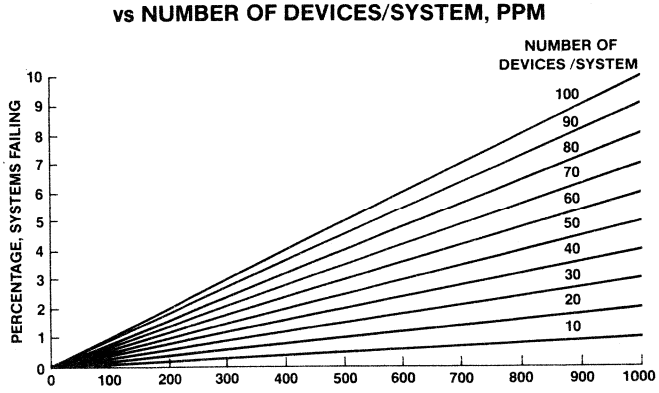


Table 2. Manufacturing Yield for Various Component Quality Levels

Devices/ System / PPM	5	10	25	50	100
50	99.975%	99.95%	99.87%	99.75%	99.5%
500	99.75%	99.5%	98.8%	97.5%	95%
5000	97.5%	95.1%	88%	78%	61%
10,000	95.1%	91.5%	78%	61%	37%

The reduced manufacturing costs are derived from the high quality provided by ProPAL and HAL devices (quality that results in increased manufacturing yield) and reduced component processing and handling costs.

The manufacturing yield (the number of working systems produced as a percentage of total number of systems produced) is a function of the quality of the components in a system. Figure 1 is a plot of the relationship between component quality and manufacturing yield. It is a graphic illustration of what is intuitively clear — as the quality of the components in a system improves, the manufacturing yield for that system improves.

Additional manufacturing cost savings come in the form of reduced processing and handling costs. Purchasing pre-programmed and functionally tested devices direct from the factory eliminates the need for the user to perform any programming or functional testing. This eliminates the need for the user to carry all the associated overhead:

- Programming (programmer equipment cost, floor space, maintenance and calibration, operator costs)
- Labeling/stripping/marking (equipment cost, floor space, maintenance, operator costs)
- Vector generation (computer/software costs, engineering costs)
- Testing (equipment costs, operator costs)
- Elimination of sockets (which allows for auto-insertion)

When ProPAL and HAL devices are utilized, handling-related rejects are virtually eliminated. We have historically found this to be one of the largest sources of rejects. Mixed device types, mixed bit patterns, mixed reject and good devices, bent leads and ESD damaged devices can all result in board level failures, failures that can be avoided with ProPAL and HAL devices. ProPAL and HAL devices come programmed, marked and fully tested, ready to go directly from the shipping box to the production floor.

The following example does not take into account a few items:

- The cost of programming, testing and marking for the PAL device user. As discussed previously, this includes labor costs, equipment costs, maintenance and calibration costs as well as other variable costs.
- Increases in production efficiency. These increases result from the reduced number of handling steps required, the ability to use auto-insertion and other manufacturing flow issues.
- The programming/test charges associated with ProPAL and HAL devices services.

A Cost Savings Example

A system manufacturer produces 2000 systems per month, each having 10 PAL devices (total 20,000 PAL devices/month). This manufacturer's cost of diagnosing and reworking a non-functional system (at system test) is $150. What cost benefits does the ProPAL and HAL Device Program offer this manufacturer?

Case I

No functional testing is performed — 5000 PPM board level quality.

- Manufacturing yield (from Table 2) = 95.1%
- 4.9% or 98 systems/month require rework.
- At $150/system, total rework costs/month are: 98 x $150 = $14,700
- At 20,000 devices/month, rework costs are: $14,700/20,000 = $0.73/device.

Case II

- AutoVec testing is performed — 500 PPM board level quality.
- Manufacturing yield (from Table 2) = 99.5%.
- 0.5% or 10 systems/month require rework.
- At $150/system, total rework costs/month are : 10 x $150 = $1500.

- At 20,000 devices/month, rework costs are: $1500/20,000 = $0.08/device.

Case III

- AC-functional testing is performed — 50 PPM board level quality.
- Manufacturing yield (from Table 2) = 99.975%.
- 0.025% or < 1 system/month require rework.
- At $150/system, total rework costs/month are: < $150.
- At 20,000 devices/month, rework costs are: < $150/20,000 = $0.01/device.

Cost Savings (utilizing):

- AutoVec testing: $0.73 - $0.08 = $0.65/device.
- AC-functional testing: $0.73 - $0.01 = $0.72/device.

The cost of doing programming varies from manufacturer to manufacturer. Generally, unless a manufacturer does high volume programming, this cost can be substantial.

Additionally, other manufacturing cost benefits are also realized. If PAL devices are being socketed, the high quality levels of ProPAL and HAL devices allow for elimination of those sockets and the utilization of auto-insertion in the manufacturing flow. Board ready devices also lend themselves more readily to just-in-time or ship-to-stock purchasing and manufacturing programs.

Finally the total costs of reworking systems must be considered. As systems become increasingly complex and dense, utilizing surface mount and increasingly sophisticated CAD/CAM technology, testing and reworking defective systems becomes increasingly expensive. Using high quality components minimizes this expense.

The cost of ProPAL and HAL device services depends on a number of factors (device type, volume, device base price). It is typically much less than it costs a manufacturer to program and test devices, not to mention the savings realized through the increased quality.

When you utilize our ProPAL and HAL Device Program you're getting tremendous quality and manufacturing cost benefits — semicustom product without many of the risks:

- You can prototype your system and start production with standard PAL devices.
- The Non-Recurring Engineering (NRE) charges for ProPAL and HAL devices are far lower than those normally required for a semi-custom circuit, and can be amortized over your first production quantity.
- You save on the cost of programming and testing devices. This also shortens your production cycle, since you can plug the devices into the socket with no additional processing.
- You save on the costs of generating test programs and functionally testing devices. All devices are fully functionally tested before they leave the factory.
- We provide you with custom marking. This saves you the added expense of stripping the mark from standard devices and remarking them with your own mark.
- You eliminate handling errors. When you use ProPAL and HAL devices, you are receiving board ready product. No need to program, mark or test. And the elimination of these extra processing steps means the elimination of many handling steps, which can be the number one cause of defective components.
- You eliminate or reduce board and system level reworking. The high quality levels provided by our ProPAL and HAL device offerings significantly reduces board reworking costs.

How Can You Take Advantage of This?

The following are some guidelines which you can use to help convert your designs to ProPAL and HAL devices.

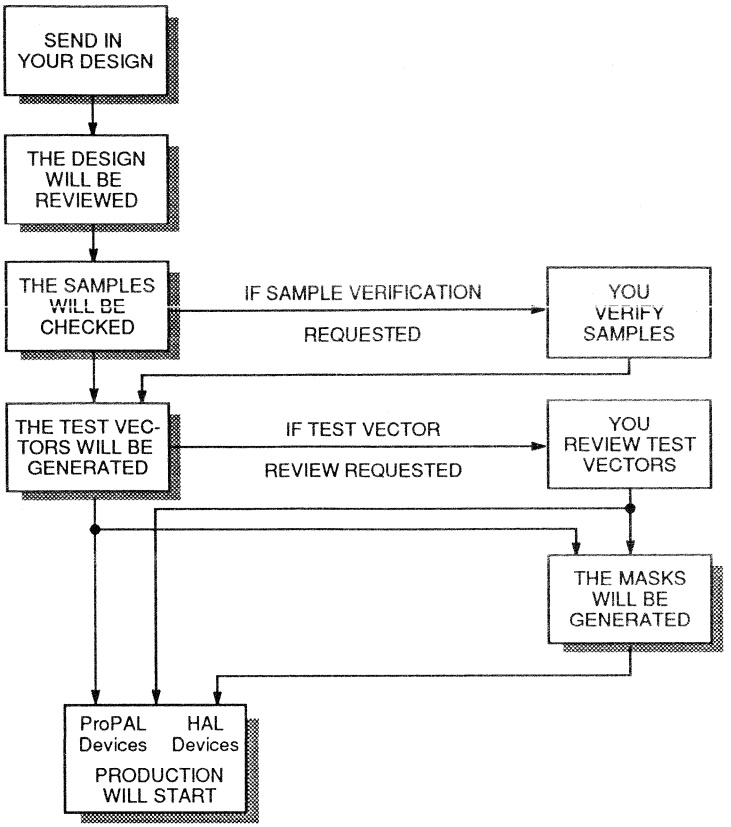
1. Send in Your Design

You will need to provide your logic equations from either PALASM®, ABEL™ or CUPL™ on magnetic media*.

When AMD generates vectors for use in functionally testing your pattern, "seed" vectors are helpful, although not necessary in providing the foundation upon which the final test vectors will be based.

If provided, a master PAL device containing your design can be used by AMD to verify that the pattern you submitted has been correctly processed. If you cannot provide an AMD master PAL device, AMD will accept your design inputs and provide ProPAL samples for your approval.

* Floppy disks are accepted in standard DEC® RT-11 (RX01) or RSX-11M®, files 11 format, or an IBM PC™ 5 1/4 in. diskette. IBM compatible (800 or 1600 BPI) nine track magnetic tapes are accepted in unlabeled (card image), files-11, or VAX VMS® backup format. If magnetic media absolutely cannot be provided, legible printout (signed and dated) from PALASM software will be accepted. Please note that magnetic media are required if you have more than 50 vectors.



2. AMD Will Verify the Design

Upon receiving your design package, AMD will enter your design into their computer and verify that there are no format or syntax problems. A fuse map will be generated, and verification sample ProPAL devices programmed.

If any questions are encountered at this stage, they will be resolved with you before any further processing takes place.

3. AMD Will Check Samples

If you have approved immediate production of your devices, AMD will make a fuse-for-fuse comparison between the verification samples and the master device you provide. If there are no discrepancies, test generation will be started immediately (or upon receipt of your purchase order).

If you prefer to verify programmed sample ProPAL devices prior to initiating production, AMD can provide them for your approval before proceeding further. Verification sample approval is also needed when no master devices are provided.

4. AMD Will Generate Test Vectors

Next, a functional test sequence is generated using TGEN™, a proprietary software package. Any seed vectors you provide will be used to help initiate test generation. TGEN will check for race conditions, monitor fault coverage and systematically add vectors until test coverage goals are met.

AMD has a test quality standard that sets as a minimum goal 90% coverage of all stuck-at faults. If acceptable coverage cannot be obtained, ways of increasing the testability of the design may have to be considered before AMD can process the pattern.

When suitable test coverage is obtained, as is normally the case, there is no need for you to be involved with vector generation. If, however, you wish to approve the test vectors before production units are generated, the vectors will be made available to you.

5. AMD Will Generate Production Units

After an acceptable test sequence has been generated, AMD will generate the appropriate HAL mask and manufacture the devices. Or in the case of a ProPAL device, AMD will arrange to program and test blank units.

Having Your Devices Marked

The standard mark consists of the device type, the package type, the date code, and logo.

If you wish, you can have the standard marking replaced by a custom marking. The logo and date code are standard, but any other markings, such as your part number or revision number, can be as you desire. The character and line limitations for the most common packages are in Table 3.

If the package you want is not listed, your local representative can help you determine the guidelines you need.

Contacts

When you are ready to put the power of the factory to work for you, just contact your local sales representative. And let us take care of your production programming, testing, and marking needs.

Table 3.

PLASTIC	20 pin (300 mil)	2 lines/13 characters per line
	24 pin (300 mil)	2 lines/17 characters per line
CERDIP	20 pin (300 mil)	2 lines/16 characters per line
	24 pin (300 mil)	2 lines/17 characters per line
PLCC	20 lead	4 lines/11 characters per line
	28 lead	5 lines/12 characters per line

Testability

INTRODUCTION

With digital logic design, it is all too easy to design a circuit which merely implements a specified function. When production starts it is suddenly found that the circuit cannot be tested, or perhaps that tests cannot be performed economically. Dealing with this situation can, at the very least, have a negative impact on the introduction of the system into the marketplace.

Potential headache can be avoided by taking test issues into consideration during the initial design. Instead of just designing a circuit which implements a specified function, which is the bare minimum that must be accomplished, that function needs to be implemented in a manner which can be tested.

The purpose of this section is to establish the notion of testability and its importance, and then to provide ways of avoiding the most common untestable circuits. The issues will be discussed primarily in the context of logic design in PLD's, although they are also relevant for general logic design.

After testability has been discussed for general circuits, some specific testability circuitry on the Am29CPL151/4 devices will be discussed. Finally, test vectors will be reviewed. Various kinds of vectors are mentioned, and the general tools available for vector generation will be summarized.

Defining Testability — A Qualitative Look

A completely testable design is one in which any and all device faults can be systematically detected.

First note that the issue is one of devices, not designs. The design itself must work as specified; that is the main job of the design engineer. Once the design is implemented in a device, the issue is how to test the device to make sure that the design has been correctly implemented. Throughout this paper, then, it will be assumed that a particular design works as is; we will just be addressing its testability.

The easiest and most effective means of testing a circuit is through a systematic series of tests. A random set of tests may also do well, but does not yield much information regarding the testability of a circuit itself. No number of random (or systematic) vectors can test an inherently untestable circuit.

In order to be able to perform a systematic test sequence, every part of the circuit under test must be accessible, so that it can be controlled. Only then can each node be forced high or low as needed. This is essentially a requirement of complete *controllability* of the circuit.

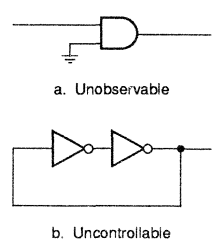
In order to be able to detect faults every part of the circuit must also be visible to the outside world, so that the results of each test can be observed. In this manner, each node can be inspected to determine its logic level. This requires complete *observability*.

These are, of course, the age-old issues of controllability and observability, which are as important for digital logic circuits as they are for so many other kinds of systems. If any portion of a circuit is uncontrollable or unobservable, then the testability of the entire circuit is compromised.

Figure 1 shows a couple of completely untestable circuits. The integrity of the top input in Figure 1a can never be verified. No matter whether it is shorted to ground, to V_{CC}, or whether it is functioning correctly, the output will be the same. That is to say, any faults on the top input cannot be observed at the output.

The circuit in Figure 1a would appear pretty useless as is. It is possible, however, that instead of being directly grounded, the second input may be driven by some distant signal, possibly on a different PC board, which happens to be a a logic low. If you cannot bring this line to a logic high, then it might as well be grounded.

The circuit in Figure 1b essentially has no input. This circuit can be thought of as a latch, but there is no way to change its logic state. Therefore, it is completely uncontrollable.



a. Unobservable

b. Uncontrollable

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Figure 1. Untestable Circuits

Quantifying Testability

In theory, if we want to quantify the testability of a given circuit, we might first attempt to make a list of all possible things that could go wrong with a circuit (no matter how unlikely), and then verify that all such "faults" can be tested, in all combinations and permutations. But for a circuit of any significance whatsoever, it will rapidly become apparent that this is not a practical solution.

What we need instead is a measure which can give an empirically reliable indication of the testability of a circuit, or of the quality of a given set of tests. There are several different such measures, but the most popular of these is the *single stuck-at faults* model.

There are several ways of analyzing circuits for single stuck-at faults. For very large circuits, various *testability analysis* schemes have been developed. However, for smaller circuits, especially of the size that would be put into a PLD, the more common method uses simulation.

Simulating Single Stuck-At Faults

A given circuit is first simulated. The quality of the simulation is important; the more complete the simulation the better. A thorough simulation can then serve as a benchmark test sequence later. In this way, the fault simulation procedure also allows us to measure the quality of a given simulation, or set of tests, in addition to the testability of the circuit.

The results of the simulation are recorded. Next, one node in the circuit is modeled with a *"stuck-at" fault* — either *stuck-at-one* (SA1) or *stuck-at-zero* (SA0), as shown in Figure 2. The circuit is now resimulated. If the simulation results of the modified circuit are different from the simulation results of the good circuit, then the fault was detected. If not, then we have a faulty circuit which appears to operate correctly.

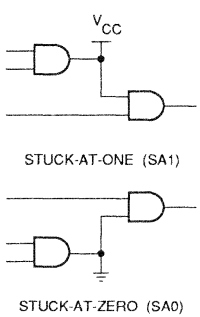

Figure 2. Single "Stuck-At" Faults

This procedure is repeated for each node, one node at a time (hence the name "single" stuck-at faults). The nodes are modeled with both SA1 and SA0 faults, so that for N nodes, we will have 2N simulations. If of those 2N simulations, D of them produced simulation results different from those of the original circuit, then we say that this simulation tested this circuit with a test coverage of D/(2N)*100%. Whereas this specifically tests only for single faults, experience shows that it is also a good test for multiple stuck-at faults.

Undetected Faults

Why are some of the faults not detected? For simple combinatorial logic, there are two basic reasons: either the simulation was not complete enough to find the fault, or the circuit itself cannot be tested for the fault. So when an undetected fault is located, the first step taken is to add vectors to the simulations which will exercise the node being tested. By doing this, we gradually improve the quality of the simulation, and thus the quality of the test sequence that we can use in production.

It is possible that certain nodes will have undetectable faults for which no new vectors can be added. These are the result of an untestable design. It is the joint job of the test and design engineers to generate a test sequence that is as complete as possible. It is the design engineer's responsibility to provide a circuit which is testable. If both of these responsibilities are carried out, the result will be a testable circuit which can be tested with an exhaustive test sequence. This will yield the highest quality system. Note, however, that the overall responsibility is shared between the design and test engineers.

Needless to say, this process of analyzing the testability of a circuit is not done all by hand; software aids are used. There are many different kinds of programs that run on many different kinds of systems, ranging from PCs to workstations to mainframes. Some of them are standalone programs; others are integrated into larger overall environments. Their specific capabilities also vary, but in general, they can simulate a given circuit with a given set of vectors; analyze the test coverage that the vectors provide for the circuit; and generate new tests, either from scratch or by improving on the coverage of a few manually generated "seed" vectors. Most can also point out potential problems areas of a circuit, such as race conditions and logic hazards.

Finally, one frequently asked question is "So what if there is a fault that can never be detected. Who cares?" Theoretically, this question is not unreasonable. However, most companies will not feel comfortable telling a customer "We only tested half of the system, but if anything goes wrong with the other half, you'll never notice it." In addition, as will be seen, many untestable circuits occur as a result of poor design practices.

Testability issues for sequential circuits have implications far beyond the test bed. Indeed, failure to take these issues into account can greatly affect the normal performance of a system. The key for state machines is controllability. The challenge is to make all elements of the circuit controllable, both for testing and for general functionality.

Designing Testable Combinatorial Circuits

All of the previous procedures dealt mostly with the ways in which existing circuits are treated. However, if a finished circuit is found to be untestable, then it must be redesigned for testability. An easier approach is to design for testability from the beginning. Unfortunately there is no direct recipe for a testable design. There are, however, many common ways of making a circuit untestable. Most of this section is devoted to pointing out such problems.

The simplest kind of problem is *redundant logic*. Figure 3a shows one such circuit. It has a purely redundant product term. If the output of either of the product terms is stuck low, for any reason, then as long as the other product term is good, the fault will never be visible at the output.

This may initially look like a benefit, since we have what we could call a "primary" circuit with a "backup." One can cover up some of the failures of the other (but not all failures). If this kind of

redundancy is truly desired, this is not the way to achieve it. When you ship out this circuit, you do not know if you really have a working primary and backup. The primary may already be malfunctioning; since it was never tested, you will never know. If you want useful, reliable redundancy, test circuitry must be added, as in Figure 3b, so that each part of the circuit can be independently tested.

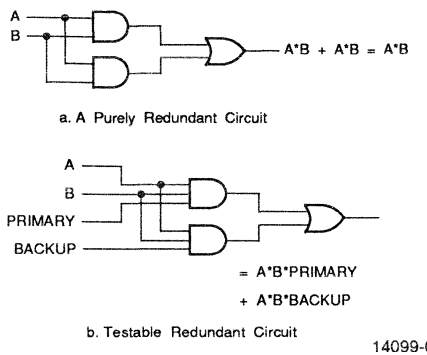

Figure 3. Making Redundancy Testable

Figure 4 shows another redundant circuit. Although the product terms are not identical, the larger AND gate is really redundant. Any stuck-low faults at the output of this gate are not detectable.

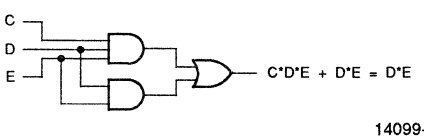

Figure 4. Circuit with a Redundant 3-Input AND Gate

Reconvergent Fanout

Redundant logic is a special case of what is called *reconvergent fanout*. This is a term that refers to circuits that have inputs splitting up, going through independent logic paths, and then reconverging to form a single output, as shown in Figure 5. When this happens, it is very easy to introduce untestable nodes. It may not be easy to identify where such nodes are.

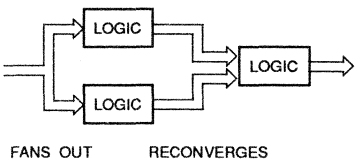

Figure 5. Reconvergent Fanout

Figure 6 is an example of a reconvergent circuit. The inputs are shared between two different product terms, which are eventually summed. This circuit appears harmless enough, but it turns out that the node indicated by "SA1" cannot be tested for a stuck-at-one condition. In other words, there is no way that we can guarantee that that node is operating correctly.

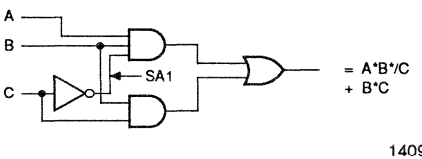

Figure 6. A Reconvergent Circuit with an Untestable Node

It is worth analyzing this circuit a bit more closely. This will give some insight into the kinds of analyses that are necessary when evaluating circuits and generating tests, and into the ways in which untestable nodes are created.

If we wish to prove that the node in question is not stuck high, then we must force it low and prove that we were successful in doing so. Thus we have two requirements: forcing the node low, and seeing the logic low on the output—controlling and observing the node.

First we raise input C high to force the node to a logic low condition, as in Figure 7a. This satisfies our controllability requirement. Next we need to provide a way to propagate this logic low to the output (Figure 7b). This is referred to as *sensitizing a path* to the output. The first step is to get the logic low past the AND gate. But if either input A or B is low, then the output of the AND gate will be low regardless of the node being tested. Thus we must force both A and B to a logic high, so that if there is a low on the output of the AND gate, we will know for sure that it came from the node we are testing. This is shown in Figure 7c.

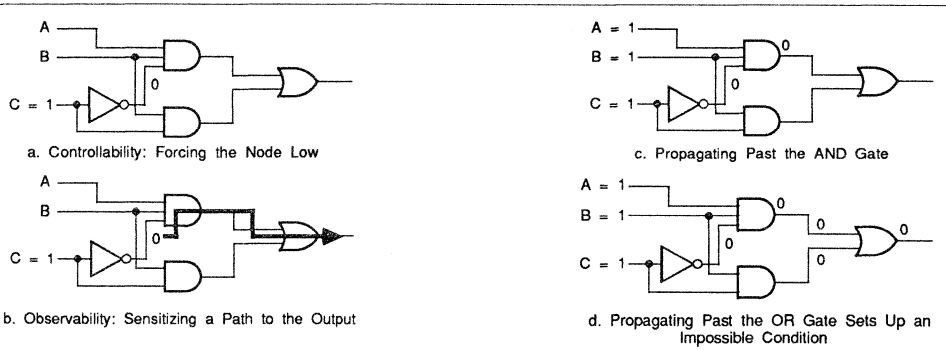

Figure 7. Analyzing Testability

Next we wish to get the logic low through the OR gate to the output. To do this, we must insure that the second OR input is always low; if it is high, then the output of the OR gate will be high regardless of the node being tested. If we can keep the lower OR input low, then if the node we are testing was sucessfully forced into a low condition, then the output will be low. Otherwise the output will be high. This can be seen in Figure 7d.

How do we keep the lower OR input low? By making the output of the lower AND gate low, which can be done by setting one of its inputs low. However, we have already required that all of the inputs be high. Thus we have required a set of conditions that cannot be met. One of three things will result:

1. The lower AND gate has both inputs high, and therefore keeps the lower OR input high. In this case, we may have been successful in forcing the node under test low, but we cannot see it at the output.

2. We bring input B low, allowing the lower OR input to go low. However, now the output of the upper AND gate will always be low. So we will see a low at the output, but we cannot be sure exactly where the low came from.

3. We bring input C low, allowing the lower OR input to go low. However, now we are no longer forcing the node under test low.

So we can either force the node low, but cannot see the low at the output; or, we can see a low at the output but cannot be sure of its source; or, we cannot force the node itself low. In any case, we will never be able to guarantee that the node under test is not stuck high.

Note that the two "independent logic blocks" which generate the signals that eventually reconverge are testable by themselves; they are just AND gates. It is only when we hook them together via the OR gate that the overall circuit becomes untestable. Thus *the testability of individual portions of a circuit does not guarantee that the entire circuit will be testable when the testable pieces are all connected.*

We can minimize this circuit using the following steps:

$$A*B*\overline{C} + B*C = A*B*\overline{C} + B*C + A*B*B \text{ (by consensus)}$$
$$= A*B*\overline{C} + B*C + A*B$$
$$= A*B + B*C$$

Thus the node we were trying to test is really not needed in the logic. The resultant circuit is shown in Figure 8, and is completely testable.

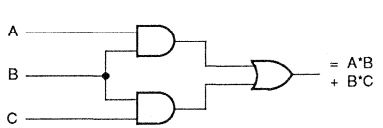

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Figure 8. The Minimized Circuit is Testable

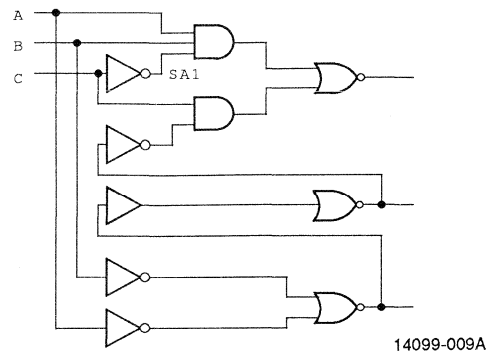

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Figure 9. A Messy Reconvergent Circuit

Not all reconvergent circuits are so simple. Figure 9 shows a more complicated reconvergent circuit. Here some signals have to travel through several levels of logic to reach their final destination. This introduces considerable skew into the circuit, and will produce glitches on the outputs during certain transitions. In addition to this, there is again a stuck-at-one fault that cannot be tested.

Circuits like this can result from the design iteration process, as a designer tries to debug a circuit. By adding this and that, eventually the circuit works. But it is a mess, has poor timing characteristics, and is untestable. A little analysis of the logic itself shows that:

the bottom output is
$$\overline{(\overline{A} + \overline{B})} = A*B$$

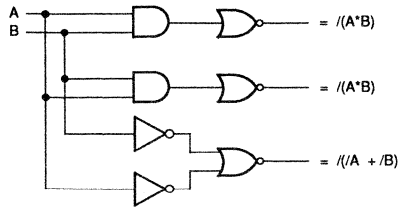
thus the middle output is
$$\overline{(A*B)} = \overline{A} + \overline{B}$$

which makes the top output

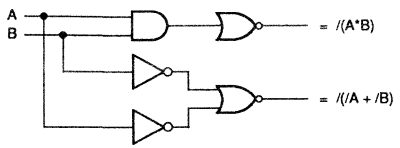
$$\overline{(A*B*\overline{C} + C*\overline{(\overline{A} + \overline{B})})} = \overline{(A*B*\overline{C} + A*B*C)}$$
$$= \overline{(A*B)}$$
$$= \overline{A} + \overline{B}$$

That is, the top two outputs are actually the same, and the third output is just the inverse of the top two. As convoluted as the original circuit looks, the logic itself is actually trivial. So if three outputs are really needed for some reason, we can generate them independently, as in Figure 10a. If only two outputs are needed, it is even easier. Figures 10b and 10c show two possibilities.

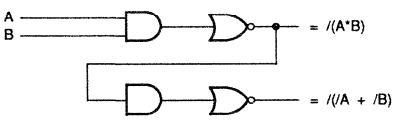
These circuits are much easier to understand, their timing characteristics are better, and they are completely testable.



a. A Cleaner 3-Output Version



b. A Clean, Fast 2-Output Version



c. A Slower 2-Output Version.

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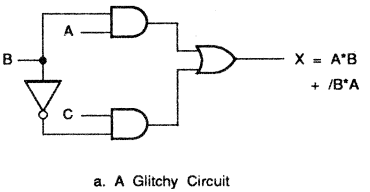
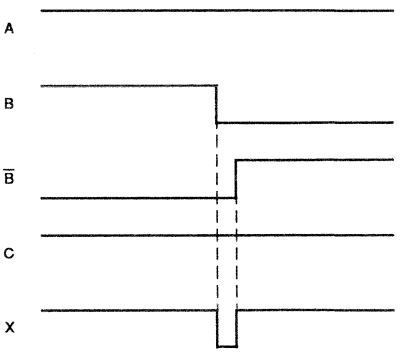
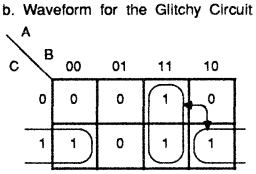
Figure 10. Simplifying the Circuit of Figure 9.



a. A Glitchy Circuit



b. Waveform for the Glitchy Circuit



c. "Gap" in the Karnaugh Map Indicates a Logic Hazard

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Figure 11. Examining a Glitchy Circuit

The Importance of Minimization

The common factor behind all of the untestable circuits we have examined is the fact that all of them were not minimal. By minimizing the logic, we made the circuits testable. This is true in general: *UNMINIMIZED LOGIC CANNOT BE FULLY TESTED.*

Very often, especially when designing with PLDs, an attempt is made to minimize logic only to the point where it fits into a particular PLD. Any further minimization is considered an academic waste of time. This is a grave misconception. Getting rid of all extra product terms, and eliminating all extra literals on the remaining product terms has real value. Failing to do so will result in untestable nodes in the circuit.

Minimizing is not always enjoyable, since hand techniques are usually too tedious, and Karnaugh maps are essentially useless for more than four or five inputs. However, computers have long been used to minimize logic. In particular, PALASM® software (version 2.22 and later) has a minimization routine which can minimize logic automatically before assembly.

Logic Hazards

One occasional side effect of minimization can be the introduction of *glitches* into a circuit. Figure 11a shows such a "glitchy" circuit. The waveform in Figure 11b shows that under steady-state conditions, as long as inputs A and C are high, the output is high regardless of B. However, as B changes from high to low, causing the top product term to shut off and the bottom one to turn on, the inverter adds a bit of delay to the path that will turn on the lower product term. Thus the top term may shut off before the bottom one gets a chance to turn on. In this case, we have two logic low signals going into the OR gate, giving a low on the output. As soon as the lower product term turns on, the output goes back high, but not before the appearance of the high-low-high glitch.

Figure 11c shows the Karnaugh map for this circuit. It is minimal, but there are two product terms which do not overlap; they are "adjacent" in one location. These represent the two AND gates in the circuit diagram. The arrows indicate the troublesome transition: when A and C are high, and when B changes from high to low or the reverse. We can intuitively think of this as a "gap" between the two adjacent product terms, in which a glitch may occur.

Note that glitching is not a certainty. It is called a *hazard* because in certain situation, given certain timing situations, there is a chance that a glitch will occur.

Note also that the glitch is not really caused by the minimization process itself, but is caused by these "gaps" in the Karnaugh map. Unminimized logic with such gaps may also be glitchy.

A PROM is a good example of such a circuit. PROMs can be used to implement any logic function of their inputs. However, regardless of the function, it is implemented in a completely unminimized fashion, using complete minterms. So even a function as simple as the one in Figure 12 (which could be implemented using a single product term, grouping all 1's into a single cell) is implemented with each 1 in its own cell. Thus there is a gap between every cell, meaning that every transition is a potential glitch. PROMs are notoriously glitchy, and it is for this reason that the output of a PROM is actually undefined until its access time has elapsed.

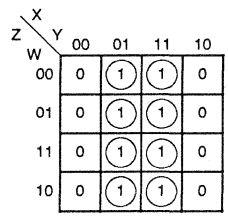

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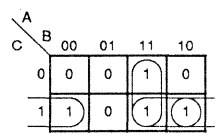
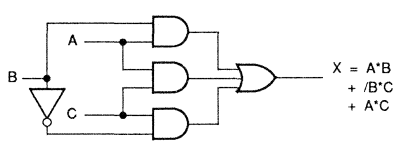
Figure 12. In a PROM, Every Transition Can Glitch

If we go back to the Karnaugh map in Figure 11c, we see that we can eliminate the gap — and the glitch — by adding a product term which overlaps both existing product terms and covers the gap. This is shown in Figure 13a, with the resultant circuit shown in Figure 13b.



a. A Redundant Product Term Can Eliminate the Glitch



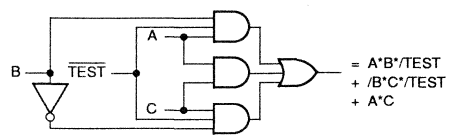
b. A Glitch-Free, but Untestable Circuit

14099-013A

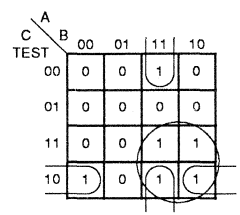
Figure 13. Eliminating Glitches

This circuit is no longer glitchy. Unfortunately, it is also no longer testable, since we have added in a redundant product term that cannot be tested (try it yourself). In order to have a circuit that is both testable and glitch-free, we must add a test input to the circuit which we can use to shut off the outside gates, isolating the middle gate for testing (Figure 14a). When the circuit is operating normally, the extra input is kept at a logic high condition, where it does not interfere with the basic logic function.

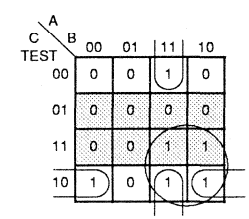
The Karnaugh map for this circuit is shown in Figure 14b. Note that all product terms overlap, but now the circuit is minimal. The size of the Karnaugh map has doubled, since we added another input. But if we isolate just that portion which corresponds to the test input being high, which is the normal operating mode (see Figure 14c), it looks exactly like the map of Figure 13a. Of course we should expect this, since we do not want the addition of a test circuit to affect the basic function.



a. A Testable, Glitch-Free Circuit



b. Karnaugh Map



c. Karnaugh Map Showing Non-Test-Mode Portion

14099-014A

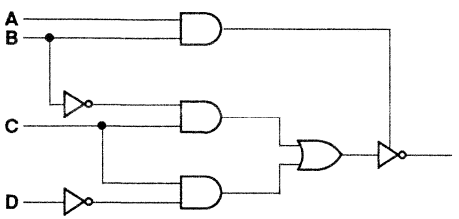
Figure 14. Making a Glitch-Free Circuit Testable

Thus, in general, these types of glitches can be eliminated first by adding some redundant logic to get rid of the gaps in the Karnaugh map, and then by adding a test input to make the circuit testable.

Using Output Enable

Most state machine PLDs are equipped with an enable pin for disabling the outputs. This is a key feature when the circuit board is to be tested in a bed-of-nails tester. When the devices driven by by the PLD are tested, it is recommended that the PLD be disabled so that there is no output level contention. Since the enable pin is usually grounded to keep outputs permanently enabled, it can instead be made available for use during testing.

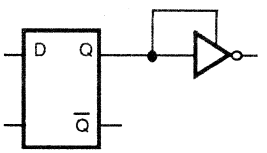
Note that for combinatorial devices, there is generally no output enable pin. The disabling feature is instead implemented through a product term. This feature is called programmable three-state. Designing the part such that the outputs can be disabled during bed-of-nails testing is also encouraged for these combinatorial designs.



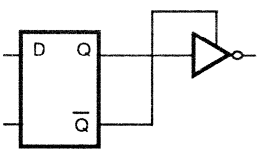
10483A-171

Figure 15. Untestable combinatorial circuit with programmable three-state

The user must be especially aware of the observability of outputs with programmable output three-state. In figure 15, input B controls both the basic circuit logic and the three-state control logic. Therefore, any function which involves B in a LOW state will not be observable, since the output will not be on. Figure 16a is a simplified representation of a register whose output cannot be observed because the three-state buffer is disabled when the output is LOW. Likewise, the circuitry in figure 16b cannot be observed when the flip-flop output is HIGH. The user must make sure that an output will not be disabled when the results of a test are to be observed.



a. LOW state observable



b. HIGH state unobservable

14099-015A

Figure 16. Untestable registered output with programmable three-state

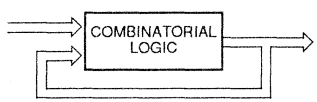
6

Designing Testable Sequential Circuits

The design of sequential circuits involves considerations above and beyond those required for simple combinatorial circuits. Latches and oscillators are circuits which appear combinatorial, but which use feedback to introduce sequential properties. State machines use flip-flops and feedback to generate what can be complex sequential circuits.

Feedback

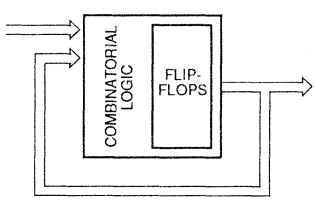
Whereas combinatorial circuits depend only on the conditions of present inputs, *sequential* circuits depend on both present conditions and past behavior to determine future behavior. This is made possible primarily by *feedback*. Feedback takes an output signal and routes it back for use as an input to the same circuit, as shown in Figure 17. We now have a situation where an output depends on itself; this can introduce new testability problems.



14099-016A

Figure 17. Logic with Feedback

Most sequential circuits (under varying circumstances also called *state machines*, *finite state machines*, and *sequencers*) make use of *flip-flops* as memory elements. These memory elements serve to remember a past condition (called a *state*) so that a future decision can be made based on it. This state is then fed back as input. With PLDs, the flip-flops and combinatorial logic are contained within a single device, as shown in Figure 18.



14099-017A

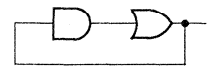
Figure 18. Structure of a Sequential PLD

Of course, the effects of feedback may have to be considered even when there are no flip-flops. The circuit in Figure 17 has feedback, but has no flip-flops. Such a circuit will either function as a *latch* or as an *oscillator*, as will be seen.

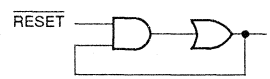
Before we look into the special needs of circuits with feedback, bear in mind that all of the testability criteria discussed for combinatorial logic still hold. The blocks of combinatorial logic shown in Figures 17 and 18 must be testable by themselves. What we will discuss here are issues which must be considered in addition to the issues involving combinatorial logic.

Latches

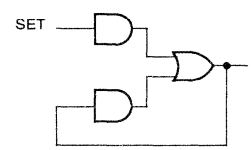
A combinatorial logic circuit which uses positive feedback is a latch. The simplest possible latch is shown in Figure 19a. The output is fed back as an input in its TRUE form. This means, of course, that the output will stay at its present level; hence the name "latch."



a. Completely Uncontrollable



b. Cannot Set Output HIGH



c. Cannot Reset Output LOW

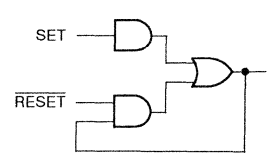
14099-018A

Figure 19. Uncontrollable Latches

The circuit as shown is clearly not useful, since it will always remain in its power-up state. If another input is added, as in Figure 19b, a HIGH output could be made to go LOW by setting the $\overline{\text{RESET}}$ input LOW. However, once the output goes LOW, there is no way to make it go HIGH again. Likewise, the circuit could be modified as in Figure 19c. Now a LOW output can be made HIGH by setting the SET input HIGH. However, once HIGH, the output can never be made to go back LOW.

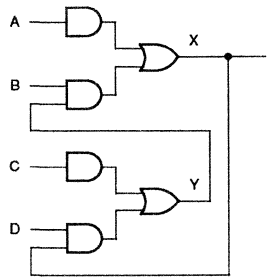
Controllable latches

For a latch to be useful, it must be completely controllable. The previous latches cannot be completely controlled. In order for a latch to be controllable, it must have both SET and RESET controls, as shown in Figure 20.



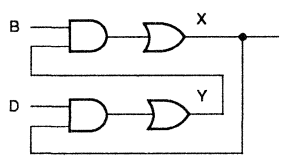
14099-019A

Figure 20. A Controllable Latch



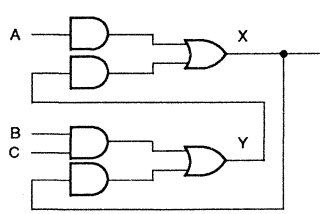
X = A
+ B*Y
= A
+ B*(C + D*X)
= A
+ B*C
+ B*D*X
SET
RESET

a. Latch with SET and RESET



X = B*Y
+ B*D*X
RESET

b. Latch with RESET Only



X = A + Y
= A
+ B*C
+ X
SET

c. Latch with SET Only

14099-020A

Figure 21. More Complex Latches

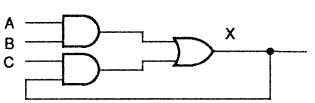
In PLDs, a latch can be detected by simplifying the logic for each function. If an output is a function of itself in TRUE form, then it is a latch. To be controllable,

- product terms containing the feedback should have at least one other direct input in the product (providing RESET control).
- there should be at least one product term with no feedback (providing SET control).

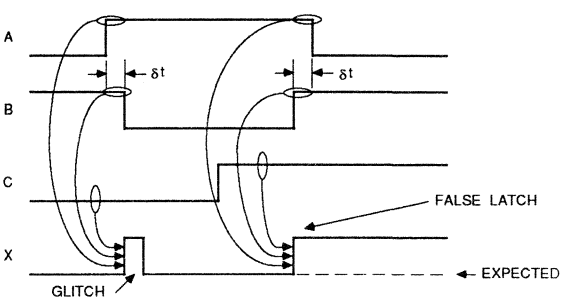
The circuit in Figure 21a provides an example. At first it is not immediately obvious that the circuit is a latch, but when the logic is simplified, we see that indeed it is. It is controllable since it has both SET and RESET controls. If the logic were as shown in Figures 21b or 21c, the latch would be uncontrollable under some circumstances.

Latch hazards

The circuit of Figure 20 can be generalized to have several inputs on both the set and reset controls. Such a circuit is shown in Figure 22. In this case, we have two inputs on the set AND gate. If the two set inputs A and B change from 0 and 1 to 1 and 0, respectively, then there will be a glitch or a false latch at the output if both inputs were 1 at some time during the transition (Figure 22). For this transition, it is important to make sure that the 1-0 transition be made before the 0-1 transition to avoid anomalous output behavior. Merely delaying one input will not help, since it will delay both rising and falling transitions.



a. Circuit



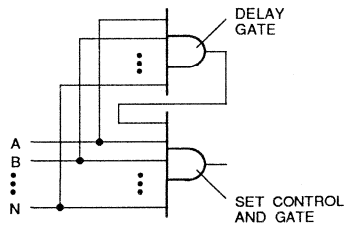
b. Glitch and False Latch

14099-021A

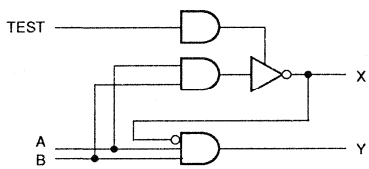
Figure 22. A Latch with More Complex SET Logic

The simplest solution to this problem is the use of an edge-triggered flip-flop to synchronize the signals. This will eliminate any such glitches. If a flip-flop cannot be used, it is possible to delay reaction to a "11" condition to make sure that such a condition is not transitory. A circuit that accomplishes this is

shown in Figure 23a. This is relatively efficient in that only one delay circuit is required regardless of the number of inputs used on the set control (within the limits of the size of the AND gate). It will require an extra output on a PAL device.



a. Circuit Which Delays "11...1" signals



b. Testable Delay Circuit

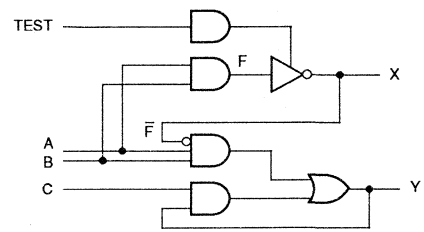
14099-022A

Figure 23. Delay Circuit

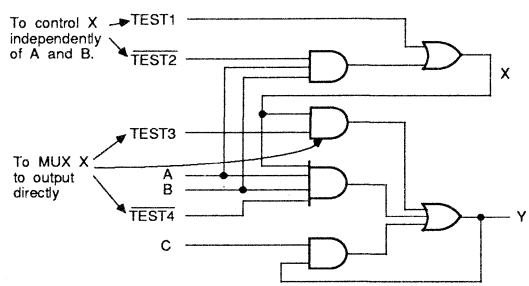
This delay circuit will delay the effect of an "11" input by an extra propagation delay. However, it also provides a window of one propagation delay which will screen out any transitory "11" conditions that occur within that window. This allows up to one propagation delay's worth of skew between inputs during a transition from "01" to "10."

Because we have introduced redundancy, the circuit must be modified to be testable. If the circuit is implemented in a combinatorial PAL device, then programmable three-state can be used to test the circuit, as shown in figure 23b. By enabling output X, the redundant circuit can be observed without regard to Y. Then, to test Y, output X is disabled and then the pin is used as an input to drive the circuitry for Y directly. This provides a simple means of testing the circuit, but it only works if pin X can be measured and driven. The complete circuit is shown in figure 24a.

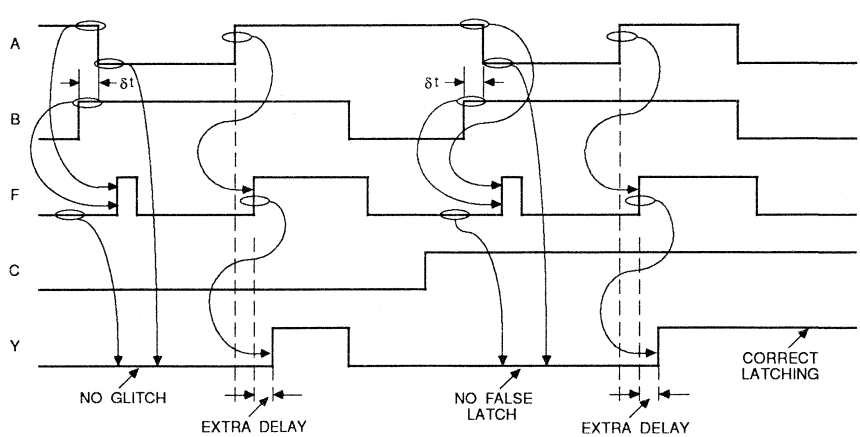
If node X is not so accessible, then additional circuitry and test inputs must be added. In the worst case, if node X is completely inaccessible, the resulting testable circuit is shown in figure 24b.



a. Complete Latch Circuit



b. Circuit if Node X is Completely Inaccessible



c. Latch Circuit Behavior

14099-023A

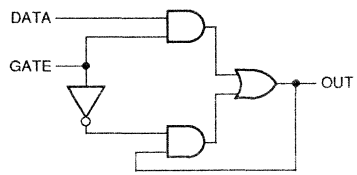
Figure 24. A Testable Glitch-Free Latch

Note that although the three-state capability is not needed, the circuit requires two extra gates, and, worst of all, four test inputs.

Figure 24c shows the behavior of either of the testable glitch-free latches.

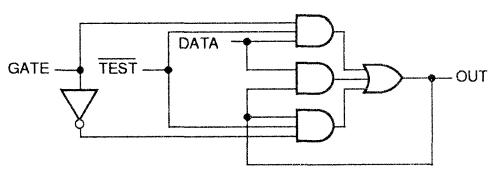
Transparent latches

Many designers like to use PLDs to design standard D-type "transparent" latches. A D-type latch is a very simple circuit, shown in basic form in Figure 25a. As it turns out, however, this is a glitchy circuit of the type discussed in the combinatorial section. The problem is compounded in this case, since, given the right timing, the glitch can actually be latched; the glitching problem is no longer transitory. If this type of circuit is desired, it must be designed to be both glitch-free and testable; the resultant circuit is shown in Figure 25b.



OUT = GATE*DATA
+ /GATE*OUT

a. Glitchy



OUT = GATE*DATA*/TEST
+ /GATE*OUT*/TEST
+ DATA*OUT

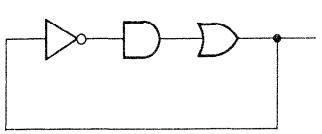
b. Glitch-Free and Testable

14099-024A

Figure 25. D-Type Transparent Latches

Oscillators

Circuits whose outputs are fed back in TRUE form are latches. If the outputs are fed back in COMPLEMENT form, then the circuit is an oscillator. A simple oscillator circuit is shown in Figure 26.

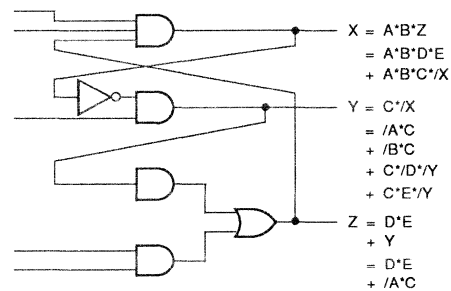


14099-025A

Figure 26. A Simple Oscillator

Latches are very often useful in circuits; oscillators rarely are. Crystals and other specialized oscillators are useful when it is necessary to generate a clock signal, for example. Trying to build an oscillator out of standard logic or PLDs will not yield a very predictable, accurate oscillator; where these circuits occur, it is usually by accident.

An oscillatory circuit may not always be obvious. It also may not oscillate all of the time. The oscillator shown in Figure 26 is uncontrollable; it always oscillates. However, just as we can design controllable latches, we can also design controllable oscillators (on purpose or by accident). This means that there may be an oscillator hidden in the circuit which will sometimes oscillate and sometimes be stable. Such a circuit is shown in Figure 27a.



a. Complete Circuit

X = A*B*D*E TERM 1
+ A*B*C*/X TERM 1

b. The Equation for X

14099-026A

Figure 27. A Conditional Oscillator

Detecting oscillators

The oscillator in the circuit is not obvious. But if we simplify the logic completely, we can see that output X depends on /X; output Y depends on /Y; and output Z depends on /Z. Since the outputs are fed back to themselves in COMPLEMENT form, the circuit constitutes an oscillator.

This circuit will sometimes be stable. If we examine the logic function determining X, we see that it has two product terms, shown in Figure 27b. Term 1 is independent of /X; term 2 is dependent on /X. If inputs A, B, D, and E are all TRUE, then term 1 becomes TRUE, and the output stays HIGH regardless of the status of the rest of the circuit. It is thus stable. However, if signals D and/or E are LOW, then term 1 will be FALSE. If, at the same time, input C is HIGH, then, as long as the output X is LOW, term 2 will be TRUE, making the output HIGH (which makes the product term FALSE, which makes the output LOW, etc.). That is, the circuit oscillates.

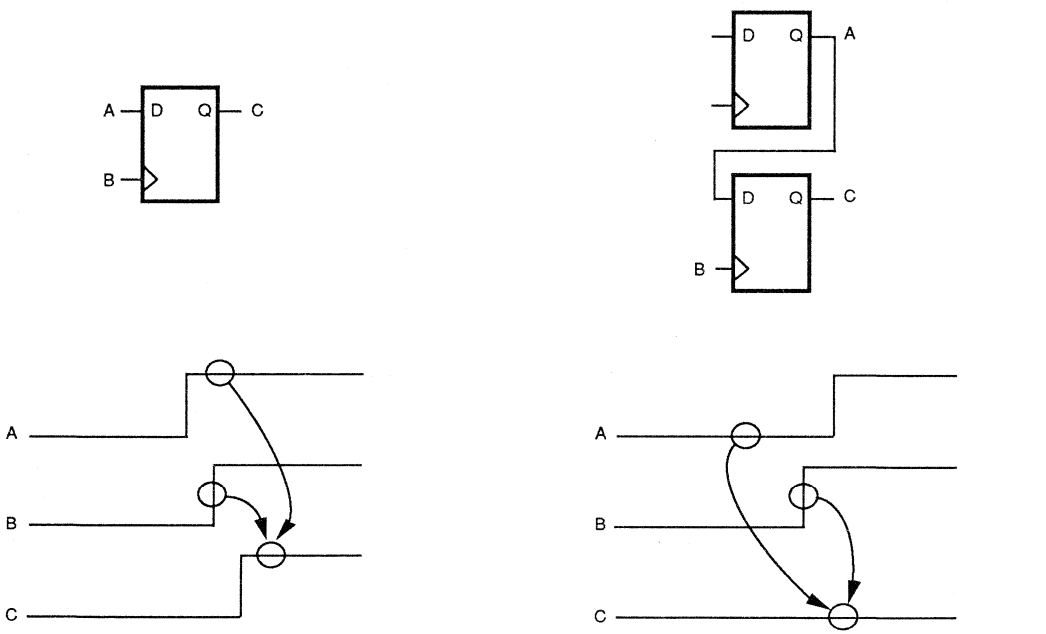
In this manner, we can identify the conditions under which a conditional oscillator will oscillate. The mere presence of an oscillator is usually an indication that the circuit needs to be changed. It may be that the circuit only oscillates under conditions that could never possibly exist. One must be very certain of the impossibility of such a condition, however, if a conditional oscillator is to be tolerated. In addition, a thorough test sequence will usually expose a circuit to conditions that it may never encounter in a real system. Thus oscillators may interfere with the test process even if they do not disrupt the system.

Using a Programmable Clock

When using the programmable clock on an asynchronous device, caution must be exercised with data setup. Refer to figure 28a, where A and B are primary inputs. One setup time (t_s) after signal A goes active, signal B goes active, clocking signal A into the register. In figure 28b, B is a primary input but signal A is fed back from another register. In this case it may be harder to ensure that the proper setup time is allowed before signal B is asserted, possibly causing improper information to be clocked into the register.

This is a simplified scenario. It does not take into account the product term on the clock, which can be programmed with a combination of any of the array inputs. A complex clock term can be a hidden source of frequently-violated setup time when feedback terms are used. Always be aware of which input or combination of inputs and feedbacks will clock each register, and calculate setup time backwards from the last input which will assert the clock term. This is the best and probably the easiest method for determining when data must be made available at the D input of the register.

This is an important testability issue because with a programmable clock, the tester may no longer be in control of the clock timing. Automatic test equipment is capable of handling the timing for dedicated clock pins, but the programmable clock feature does not allow the tester the luxury of a single controlled clock pulse.



a. Using an input to drive the clock

b. Using feedback to drive the clock

14099-027A

Figure 28. Using a programmable clock

Designing Testable State Machines

State machines have their own set of controllability issues. These essentially boil down to the concepts of *initialization* and *illegal states*.

State machine initialization

The nature of a state machine is that there is a well-defined sequence of states through which the machine will traverse as it operates. This implies the existence of a "first" state. Of course, these initial states vary from design to design. One obvious problem is the fact that many flip-flops — especially older varieties — do not power up in a predictable state.

Power-up initialization

Flip-flops that truly power up into a random state must be initialized explicitly. Lately, however, flip-flops have become available which have "power-up reset". This allows the flip-flops to power up into a predictable state every time. This is helpful when the power-up state also happens to be the initial state. But even if it is not the initial state, a predictable initialization sequence can bring the state machine into its start-up state.

Unfortunately, such initialization schemes rely on the ability of the device to initialize itself when being powered up. If the system needs to be re-initialized, it will have to be completely turned off and then turned on again. Anyone who has had to turn off a computer in order to reboot will know that this is not an elegant way of re-initializing. By building initialization into the design, a means of performing a "warm boot" is provided. It is for this reason that initialization must be considered along with all other aspects of the design.

Some devices, such as the PAL32VX10/A, the PAL22V10, and other PAL devices, have mechanisms specifically designed for initializing a state machine. These are usually in the form of global preset and reset product terms. By programming the conditions for initialization onto such terms, the device can be re-initialized at any time. Other devices, like the PLS devices, have pins which can be dedicated as preset pins.

Including initialization in a design

Some of the simpler devices do not have specific provisions for initialization. However, the need is still present in these devices; here the initialization should be included in the design. This is a very simple process; it can be added in after all of the other design details have been worked out. Adding initialization will use up one input pin and potentially one product term on some outputs; this can affect the choice of device for the design.

To provide initialization in an otherwise complete design when Boolean equations are being used:

- determine the start-up state.
- assign each bit as being initialized active or inactive, based on the desired start-up state.
- if a bit is to be initialized inactive, add "/INIT" to every product term for that bit.
- if a bit is to be initialized active, add one product term consisting solely of "INIT."

Here we have assumed that the initialization pin has been called "INIT." "Active" would mean HIGH for an active high device; LOW for an active low device. "Inactive" is just the reverse.

The equation in Figure 29a can be initialized inactive as shown in Figure 29b, or active as shown in Figure 29c. Initialization is accomplished by asserting the INIT pin and clocking once. This "cookbook" approach is very reliable.

```
Q0 := Q1*Q2
    + Q2*/Q3
```

a. Uninitializable

```
Q0 := Q1*Q2*/INIT
    + Q2*/Q3*/INIT
```

b. Initialized Inactive

```
Q0 := Q1*Q2
    + Q2*/Q3
    + INIT
```

c. Initialized Active

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Figure 29. Designing in Initialization

PALASM software also makes it possible to design state machines with a special syntax which essentially allows the state diagram to be transferred directly into a design file. For devices which have no dedicated initialization features, the initialization branches should be explicitly built into the state diagram. The software then performs the remainder of the processing needed.

Illegal states

A state machine is formed by using a set of flip-flops to remember states, and assigning a code to each state. Since there are 2^n different codes that can be assigned to a group of n flip-flops, there is a good chance that some codes may not be used. For example, if a state machine is to have 6 states, 2 flip-flops will not be sufficient; 3 are needed. But 3 flip-flops allow 8 states, which will result in 2 unused states (see Figure 30).

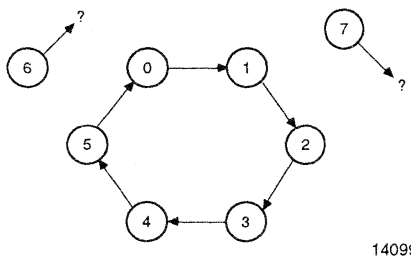

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Figure 30. Illegal States

Assuming that the state machine has been designed correctly, there is no reason why these extra states should ever be entered; therefore they are called "illegal" states. Unfortunately, situations do occur, thanks to noise and other unpredictable occurrences, which result in the state machine being in an illegal state. When this happens, the immediate need is to return to a normal sequence of states: *there must be a predictable means of getting from any illegal states into a legal state.*

Illegal state recovery is a controllability issue which actually affects functionality more than it affects testability. But the concepts used for functionality and testing are so closely related that it is worth treating here.

Recovering from illegal states

There are three basic ways to get out of an illegal state:

- re-initialize
- make sure that one can continue clocking until the machine recovers
- design the machine such that the start-up state is reached from any illegal state in one clock cycle, independent of any conditional inputs

Of course, re-initializing will take the machine back into its start-up state from any state, legal or illegal (Figure 31). The disadvantage here is that outside control is needed to force initialization.

Very often, a path will exist which eventually takes the state machine back into a normal sequence (Figure 32). These paths are not usually designed in; they just happen to be there. In fact, if D-type flip-flops are used, it is surprisingly difficult to get a "closed" set of illegal states (that is, a set such that once one of the illegal states is entered, the machine will forever remain in

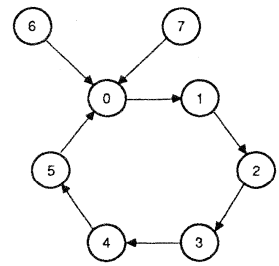

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Figure 31. Using Initialization to Recover

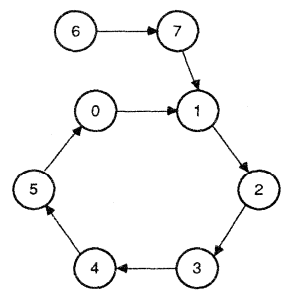

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Figure 32. Cycling Back to a Legal State

illegal states) by accident. In most cases, there will be a path which eventually leads back to a legal state. In these cases, merely clocking enough times will cause the machine to recover.

The drawback here is that one does not know ahead of time how many clock cycles will be needed. This necessitates some built-in way of knowing just when a legal state has been re-entered. And once that state has been reached, further cycling may be needed to get to a point where operation can resume.

Designing-in one-step recovery

The most predictable way of dealing with illegal states is to provide a one-step path back to a legal state. Depending on the state desired, more or less work may be involved to do this. For PAL devices, we can consider three cases:

- all illegal states go to state 00...0
- all illegal states go to one state other than 00...0
- each illegal state goes to some legal state

The cause of poor illegal state recovery can be illustrated conceptually with Karnaugh maps (although realistically, Karnaugh maps are often not used). When calculating the equations for a particular bit, it is tempting to use Don't Care cells from the Karnaugh map (Figure 33) to simplify the logic. The success of illegal state recovery depends on how these Don't Care cells are treated.

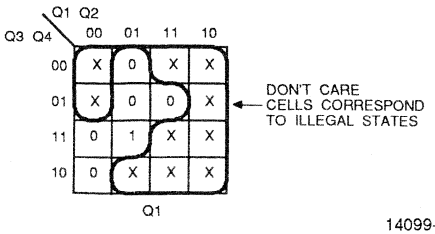
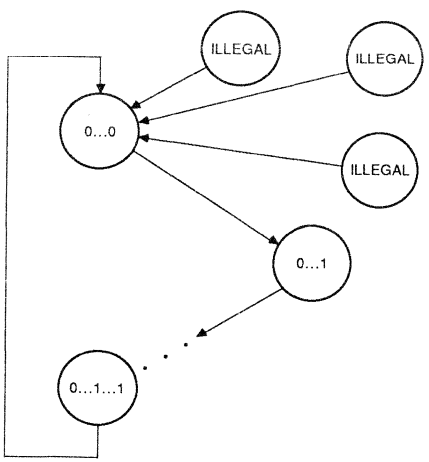


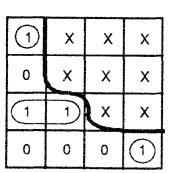
Figure 33. Illegal State

Recovering into state 00...0

This is the simplest case; it is illustrated in Figure 34. It is accomplished by not using any illegal states to generate the logic for any of the bits. Since most PAL devices have only D-type flip-flops, a bit will go HIGH only as a result of legal states. Any illegal states will cause all bits to be LOW.



a. State Diagram



b. Karnaugh Map

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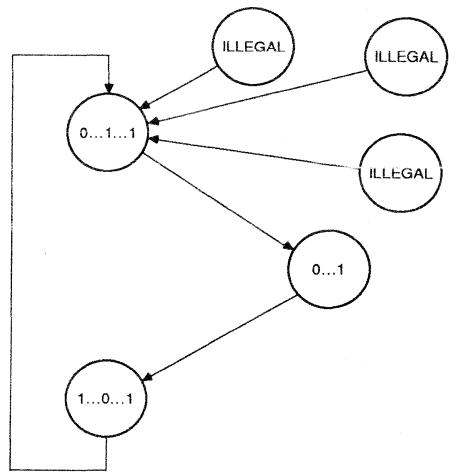
Figure 34. Recovering to State 0...0

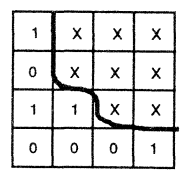
This procedure does not work when J-K or T-type flip-flops are used. In fact, it is deadly. Whereas a D-type flip-flop defaults to LOW, J-K and T-type flip-flops hold their present state as a default. Thus if illegal states are not considered in the transfer functions, an illegal state will cause the state machine to be locked up in that state.

Recovering into one fixed state

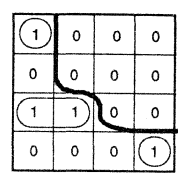
This case is shown in Figure 35a. The procedure can be illustrated conceptually with a Karnaugh map. It must first be decided which legal state will be entered, and the resultant value of each



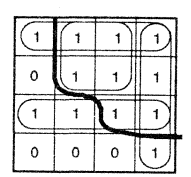
a. State Diagram



b. Karnaugh Map for Bit Qn



c. Bit Qn Recovers to 0



d. Bit Qn Recovers to 1

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Figure 35. Recovering to a State Other Than 0...0

state bit. The Don't Care cells for each bit are then filled with the corresponding next state bit value; if the next state for a bit is to be 1, then Don't Care cells are filled with 1's for that bit's Karnaugh map; the procedure for a 0-bit is analogous. The equations are now taken by including either all Don't Care cells if filled with 1's, or none of them if filled with 0's. This procedure is illustrated in Figures 35b, c, and d.

When Karnaugh maps are not used, the same result can be obtained by explicitly considering all illegal states. When calculating the Boolean equations for:

- a bit that will be 0 after recovery, *no* illegal states should be included.
- a bit that will be 1 after recovery, *all* illegal states should be included.

When J-K flip-flops are used, then the transfer function for either J or K — but not both — will include all illegal states.

- If a bit is to be HIGH after recovery, *J* should account for all illegal states; *K* should account for none.
- If a bit is to be LOW after recovery, *K* should account for all illegal states; *J* should account for none.

This must be done explicitly for J-K flip-flops even if state 0...0 is the recovery state.

When T-type flip-flops are used, there is no easy way out; any recovery must be explicitly designed-in as part of the original function.

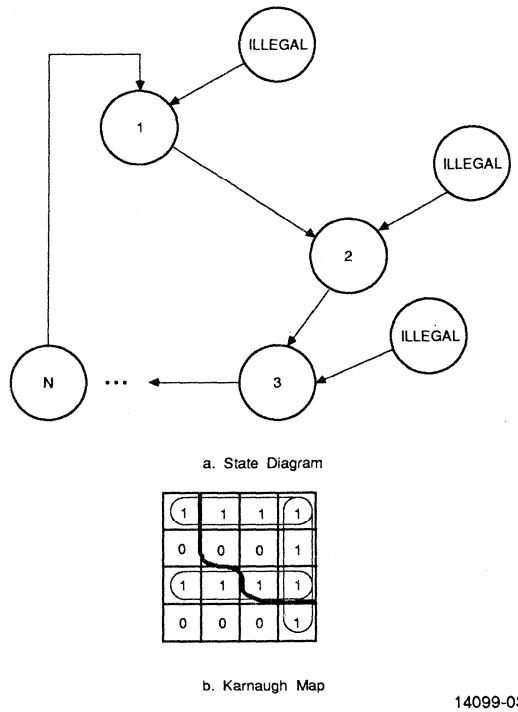


Figure 36. Recovery Such That Logic Functions Are As Simple As Possible

Recovering Into Any Legal State

The third case allows one to fill in the Don't Care cells of a Karnaugh map in such a way that some legal next state is always reached in one clock cycle, but such that the 1's and 0's are placed to keep the logic functions simple. This is shown in Figure 36. The disadvantage here is that since different illegal states result in a different legal state, some additional cycling may be required to allow operation to resume.

When Karnaugh maps are not used, this can be implemented more simply by explicitly including the illegal states as part of the complete state diagram. This is especially simple if the state machine input format for PALASM software is being used.

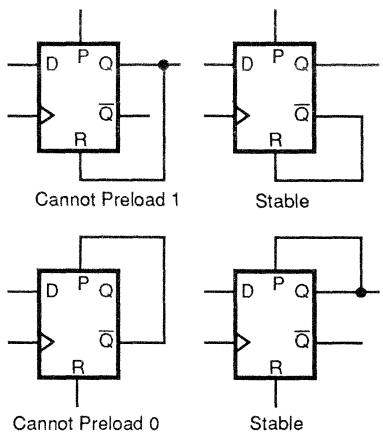
Default transitions

In PLS devices, the complement array can serve as a way of recovering from illegal states. In a design, only legal branches are defined. When in an illegal state, since no legal branch is active, the complement array is activated, allowing for some default state to be reached.

Testing illegal state recovery

One of the difficulties of designing illegal state recovery into a circuit is the fact that it is difficult to test. Because the state is illegal, it is impossible to force the circuit into such a state. The use of register preload circumvents this problem. With preload, any state — legal or illegal — can be loaded into the register. If an illegal state is loaded, then the circuit can be tested to verify that correct recovery does indeed occur.

The use of preload must be considered carefully with devices having programmable asynchronous preset and reset features. If these are driven by feedback from an output, then situations can occur where preloading one state immediately causes a preset or reset to the opposite state (Figure 37). There are two alternatives: either avoid preloading such states, or include a control input in the preset and/or reset product terms which can disable the feature when testing.



Stable Case: Can preload any state
Other Cases: Preloading any state will cause PRESET or RESET to opposite state.

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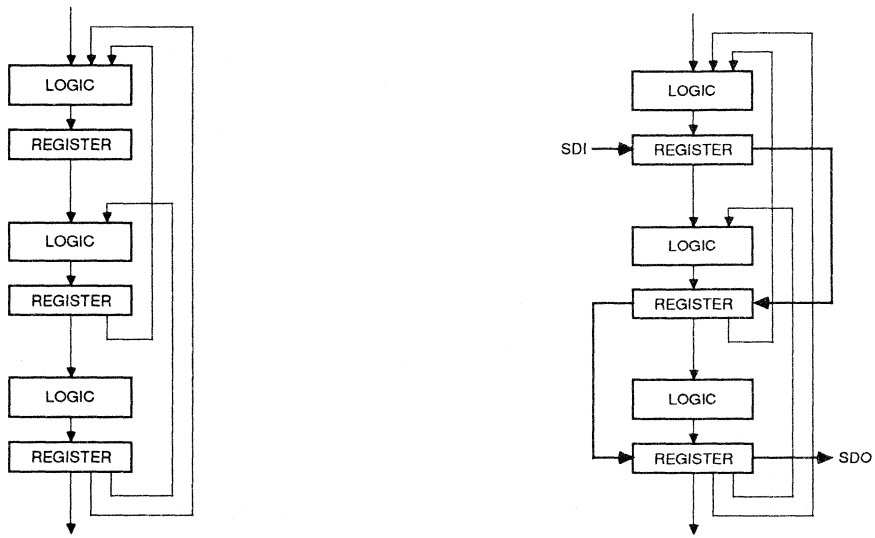
Figure 37. Preloading Registers with PRESET and RESET

Designing for Testability With SSR™ Diagnostics

Today's more complex circuits and systems are becoming prohibitively expensive to test using standard methods. Serial Shadow Register (SSR) diagnostics (also referred to as Diagnostics-On-Chip™, or DOC™) is a test feature provided in several of Advanced Micro Devices' chips as a means of increasing testability at the system, board, and chip levels. SSR is especially useful in the Am29CPL151 and Am29CPL154 sequencers.

SSR Architecture

Testability consists of two basic elements: controllability and observability. In a sequential (registered) system, these two elements are lost when a register is not directly accessible. In Figure 38a, the first register is not observable and the last register is not controllable. Figure 38b shows that the addition of a scan path through each register, as in the SSR method, provides the direct access for controllability and observability, which ensures complete testability.



a. Standard Sequential Logic

b. Sequential Logic with a Scan Path

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Figure 38. Testability Can Be Increased by Providing Direct Access to All Registers

The heart of the SSR circuitry is the shadow register (see Figure 39). The shadow register is a serial/parallel register, equivalent in length to the pipeline register. It is called a shadow register because it is invisible to the device during normal operation. It is clocked by its own clock input, DCLK.

In normal mode (MODE input is LOW), the shadow register operates as a serial shift register (see Figure 40). The Serial Data Input is SDI, and the Serial Data Output is SDO. The pipeline register can operate at the same time while MODE is LOW.

In diagnostic mode (MODE is HIGH), the shadow register operates as a parallel register (see Figure 41). It can be parallel loaded from or to the pipeline register by clocking the receiving register. A swap can be performed by clocking both at the same time.

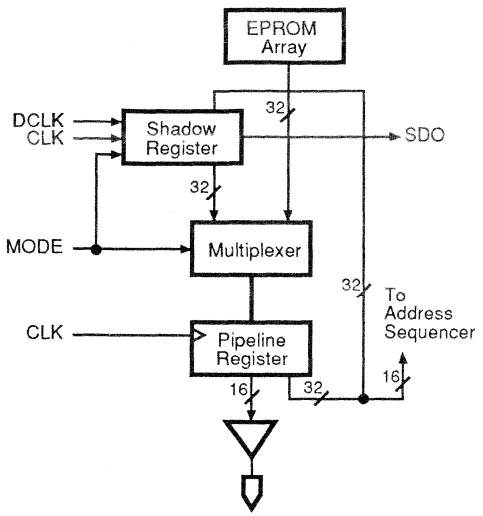

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Figure 39. SSR Circuitry in the Am29CPL151

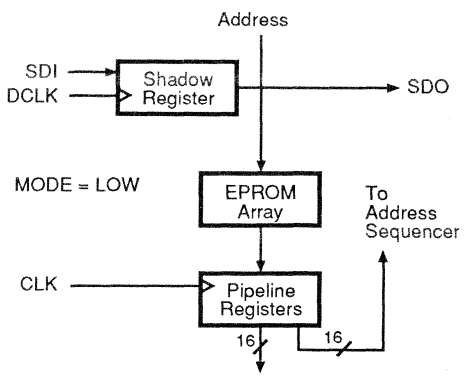

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Figure 40. The Shadow Register Operates as an Independent Shift Register when MODE is LOW

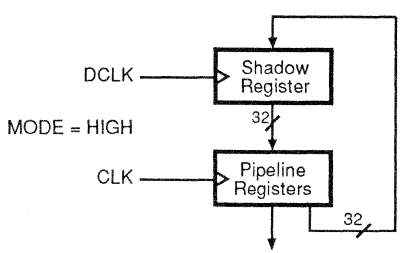

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Figure 41. The Shadow Register Can Parallel Transfer its Contents to and from the Pipeline Register when MODE is HIGH

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Pipeline	Shadow	SDO	
L	X	↑	*	Pn ← PROM	HOLD	S0	Load pipeline register from EPROM array
L	X	*	↑	HOLD	Sn-1 ← Sn S31 ← SDI	S0	Shift shadow register data
L	X	↑	↑	Pn ← PROM	Sn-1 ← Sn S31 ← SDI	S0	Load pipeline register from EPROM array while shifting shadow register data
H	X	↑	*	Pn ← Sn	HOLD	SDI	Load pipeline register from shadow register
H	L	*	↑	HOLD	Sn ← Qn	SDI	Load shadow register from pipeline register
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.
† Reserved operaton for '818 8-Bit Diagnostic Register.

Figure 42. SSR Diagnostics Function Table

All of the functions of the SSR circuitry are described in the function table (Figure 42).

SSR allows access to all 32 pipeline flip-flops in the Am29CPL151 through the serial path, requiring only four pins. A programmable option allows the four SSR control pins to be used. Pins CC, $\overline{ZERO}$, P[7], and P[6] become SDI, SDO, DCLK, and MODE, respectively. These four pins can be controlled directly, or can be connected to other SSR circuits in series. A series connection of several SSR circuits allows the same four signals to address an unlimited number of flip-flops on a board or system (Figure 43).

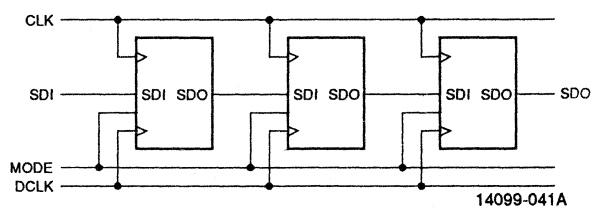

Figure 43. Example Architecture for Use of System-Level Diagnostics

A typical test would be performed as follows:

1. Test vector shifted into shadow register(s)
2. Test vector parallel transferred to pipeline register(s)
3. Device/system clocked desired number of times to run test
4. Test results parallel transferred to shadow register(s)
5. Test results shifted out of shadow register(s)

Note that while shifting, the system can return to normal operation. In addition, while test results are being shifted out, a new test vector can be shifted in.

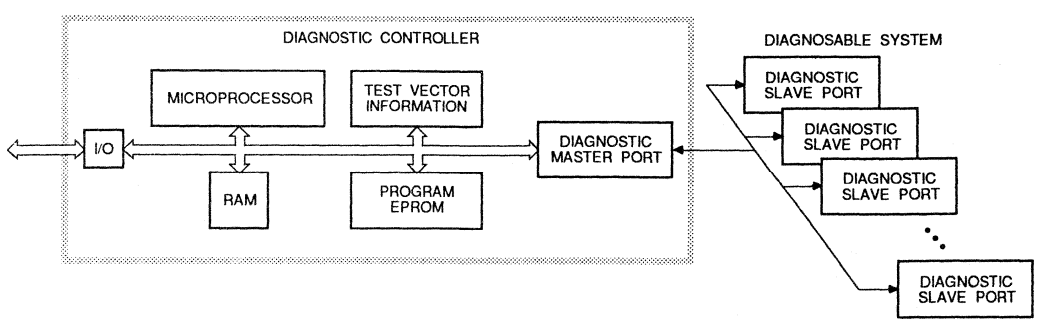

Figure 44. Example Architecture for Use of System-Level Diagnostics

System-Level Testing

At the system level, SSR provides the ability for a diagnostic controller to monitor the interior status of a system. The diagnostic controller could control several scan loops, selecting the loops required for the test needed (Figure 44).

However, many key products, such as microprocessors, are not available with the SSR function and cannot be part of the scan path. This limits the use of SSR for full system-level testing to selected manufacturers who can use this additional testability as an enhanceement to a larger system-level testability strategy.

In addition, little support is available for writing the test vectors that can be run through the SSR scan path. The software that is available is expensive and runs on large computers only. This is another factor that limits the use of SSR on a system level. On the board or chip levels, however, test vectors are much easier to generate and can even be found by running vectors through a known good unit.

A complete system-level test would require that most of the devices in the system incorporate SSR circuitry. Other devices in the SSR family are shown in Figure 45. Devices with circuitry equivalent to the SSR format are available from several other suppliers as well. Also, many gate array and standard cell manufacturers offer standard functions similar to the SSR scan path and can easily be included in custom designs, including boundary scan.

PART NUMBER	DESCRIPTION
Am29CPL151	64-state sequencer
Am29CPL154	512-state sequencer
Am27S85/A	16-K Diagnostic PROM
Am29818	8-bit register

Figure 45. SSR Products Family

Board-Level Testing

SSR in the Am29CPL151/4 is especially useful at the board, or functional, level. The Am29CPL151/4 will usually form the heart of a function, such as a peripheral controller. In addition, it often will serve to off-load the main Central Processing Unit (CPU) and be partially controlled by the CPU. SSR allows direct control of the Am29CPL151/4 device, bypassing a difficult-to-control CPU and taking command of whatever function the Am29CPL151/4 performs (Figure 46). Here, on-board diagnostics can be easily done with the Am29CPL151/4. The alternative is to dedicate edge-connector signals to the SSR path.

The SSR circuitry provides access to the Am29CPL151/4's pipeline register. This can be used to set the outputs to a given state, in order to test the effect on the devices surrounding the Am29CPL151/4. Or, the pipeline register can be set to a given state and then left to run freely, to verify functionality. If combined with control of the device inputs, the sequencer can be stepped through a number of states, to test the response of the surrounding logic. This is especially useful for bed-of-nails board-level testing; the Am29CPL151/4 can be tested completely without having to be backdriven.

Device-Level Testing

On the device level, the SSR circuitry effectively provides a preload function for the register. Instead of loading the register from the outputs, as with standard PAL devices, the register is preloaded from the shadow register. Preload is necessary for testing the device functionality, since the buried flip-flops must be set to a known condition before the device can be tested.

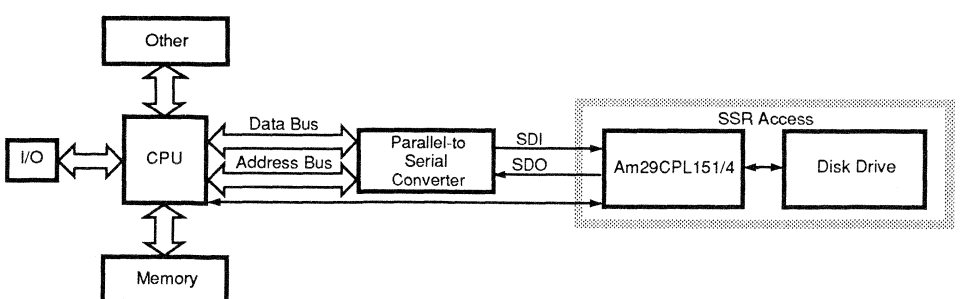

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Figure 46. SSR Allows Direct Access to Peripheral Elements In a System, Bypassing the CPU

The SSR circuitry allows more than just a preload equivalent, however. It also allows observation of the pipeline register, which contains all of the state information. Thus, an individual state transition may be tested by preloading the desired state, setting the inputs, clocking the device, and then observing the resulting state in the pipeline register. State transitions which do not result in a change in outputs are thus easily tested (Figure 47).

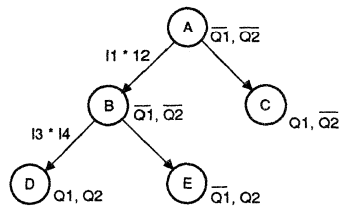

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Figure 47. Buried Flip-Flop Observability Is Required to Verify the Transition from A to B.

Using Test Vectors

Digital systems are generally tested by applying a sequence of test vectors. A test vector is a group of signals which are applied (forced) and measured (sensed) on a device or a board. The vector thus defines all inputs and expected outputs for a given test. As we have noted, the sequence of tests performed greatly affects the quality of the overall tests, as measured by the fault coverage.

In general, we can talk in terms of three kinds of vectors. *Simulation* (or application) vectors, *functional* test vectors and *signature* test vectors.

Simulation vectors are generated during the design process. Their main purpose is to help the designer verify that the design has been correctly implemented. They represent the way in which the circuit was intended to operate. When PALASM software (or almost any other PLD design software package) is used, simulation may be performed prior to programming a device. The software simulates the operation of the circuit, and then generates vectors from the simulation, adding the vectors to the JEDEC file. These vectors can then be used for testing by programmers that have the capability of performing functional tests.

While simulation vectors may be adequate for verifying that the design is operating as expected, they generally do not provide very extensive test coverage. For this reason, we distinguish functional test vectors from simulation vectors.

It is very difficult to generate a complete set of functional test vectors by hand; computer programs are generally used instead. The simulation vectors are often used as a basis for generating a more comprehensive set of functional test vectors; in this capacity, the simulation vectors serve as *seed* vectors. There are many programs which perform this function although many of the programs require larger computers and take a long time to run. AMD also generates functional test vectors for patterns that are used in ProPAL and HAL devices.

More recently, programs which run on the IBM PC-compatible computers have been developed to generate vectors for use in testing PLDs. Most well-known among these are PLDtest™ from Data I/O Corp., and Anvil ATG™ software. These programs use the programming information in the JEDEC file to generate tests.

On most patterns, they can generate test sequences of high quality. If complex internal feedback is used in a particular design, then some manual test generation may still be needed to improve the test coverage. Both of these programs support the use of register preload for initializing states; the Anvil and PLDtest Plus packages can also generate tests for devices which do not have the preload feature.

While functional vectors provide more extensive tests, they may not exercise the circuit in the manner in which it was meant to be used. Thus, for example, a conditional oscillator in a circuit (as discussed previously) may not be a problem during simulation, since the conditions causing oscillation are not thought to be possible by the designer. However, the functional vectors will take all situations (some of which may not be physically possible) into account in the tests. Thus more subtle design problems may become apparent when functional test vectors are generated.

Signature vectors are random vectors which are first applied to a device which is known to be good in order to generate a "signature". This same set of vectors is then applied to a device of unknown quality; if the same signature results, the device is said to be good; if a different signature results, then the device is assumed to be faulty.

Signature vectors can vary greatly in the quality of testing they can provide. Since they are generated with no knowledge of the circuit being tested, many more vectors must be used to perform a good test. The quality of the test depends on the circuit being tested, the number of vectors used, the speed with which the tests are applied, and the algorithm used to generate the vectors. The tester must also be able to apply a preload sequence to devices that have registers; otherwise two devices may power up into two different states. In that case, both devices will generate different signatures even if both are good devices.

Quality signature testing can be very cost effective, since no advance knowledge of a device pattern is needed. This reduces the amount of resources that must be dedicated to test vector generation.

The different types of vectors are summarized in Table 1 below.

TYPE OF VECTOR	PURPOSE	GENERATED BY:
Simulation (Application)	Used for verifying whether or not a design will operate as expected when implemented.	Sequence defined by the design engineer, usually by hand. Actual vectors generated by design software, placed in the JEDEC file.
Functional	Used for verifying that a device is operating correctly.	Usually generated by a computer program such as PLDtest or Anvil ATG. The simulation vectors can be used as seed vectors
Signature	Used for verifying that a device is operating correctly without functional vectors.	The tester generates the test sequence during the test.

Table 1. Test vectors

SUMMARY

The time to start considering ways of testing a circuit is before the circuit has been designed. The key to testability lies in the way the circuit is implemented.

Basic combinatorial logic can be made completely testable simply by minimizing logic. It is not even necessary to analyze the circuit for redundancy or reconvergent fanout; automatically minimizing all logic will eliminate any occurrences.

Where a sequential circuit is generated from simple feedback paths in the logic, the circuit must be analyzed as a combinatorial circuit. All combinatorial logic must be included to determine whether the circuit is a latch or an oscillator. If a latch is desired, it should be completely controllable. If an oscillator is found, it is probably not desired, and will generally indicate a mistake in the design. If a conditional oscillator is to be tolerated, one must be sure that the oscillation conditions can never occur, and that the test procedure will not cause oscillation.

In general, combinatorial circuits should be analyzed completely for the presence of latches and oscillators (wanted or unwanted). This can be done by simplifying each combinatorial logic block to see whether any signal ultimately depends on itself.

When the sequential nature of a circuit is derived through the use of flip-flops to generate a state machine, the two key issues are initialization and illegal state recovery. A combination of device features and careful circuit design will yield circuits that can behave predictably even in unexpected situations.

SSR is a testability feature that is useful in the Am29CPL151/4; it may be used on multiple levels: system, board, and chip. While the system-level uses may be restricted by the limited availability of support products, the board or functional-level uses are exceptionally handy when the Am29CPL151/4 acts as a local controller. And on the device level, the SSR circuitry provides a means of accessing the buried flip-flops within the device for functional testing.

It is important to analyze the testability of a circuit before committing it too far. Thus any changes can be made early on. In particular, if the test analysis software points out any logic hazards in your circuit, you can easily remedy them by modifying the design.

These simple steps, taken early in the design phase, can help avoid later redesigns, and ultimately provide a higher quality system.

Finally, the ultimate test quality depends also on the quality of the test sequence used for production, functional test vectors and high quality signature tests will provide you with the highest confidence in the quality of your system.

INTRODUCTION

Data I/O Corporation currently offers two PLD (programmable logic device) testing tools, PLDtest Plus and PLDtest. These tools are both capable of automatic test vector generation (ATVG) used in testing of manufacturing defects in PLDs and for performing design-for-testability (DFT) analysis. PLDtest has been in existence for several years and is primarily used for preloadable and combinatorial PLDs, while PLDtest Plus, introduced in April of 1989, is used for both non-preloadable and preloadable devices. PLDtest Plus contains all the features found in PLDtest, with additional features required for in-circuit testing. This makes PLDtest Plus useful for both component-level and board-level testing of PLDs. With extensive DFT features, PLDtest Plus and PLDtest

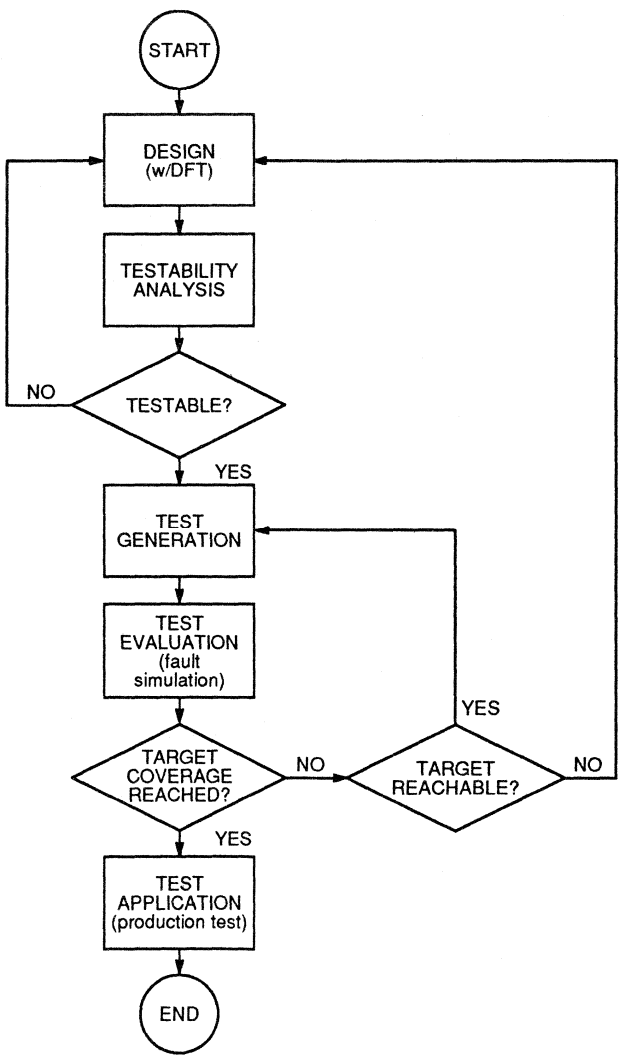


Figure 1. Design and Test Development Activities

are valuable tools for test and design engineers working with PLDs to meet the product quality objectives as well as to reduce management's concern over high costs in testing.

Where do PLDtest Plus and PLDtest fit in the design cycle? As shown in Figure 1, both tools can be used in the design phase, the prototype verification phase, and the testing phase of a product's life-cycle. In the early design phase, PLDtest Plus and PLDtest analyze the testability of the design by fault grading the design engineer's seed (design verification) vectors. This analysis determines fault coverage and identifies untestable faults, as well as portions of the design with low testability. The result of this analysis can be used as an aid in redesign for testability. Seed vectors can also be corrected automatically to ensure all test vectors work correctly. Fault grading is the function that PLDtest Plus performs to determine the exact amount of device test coverage provided by the user-supplied seed vectors. Fault coverage is a measure of how effective a set of test vectors is in detecting potential faults in a PLD.

In the prototype verification and testing phases, PLDtest Plus provides meaningful fault coverage when generating test vectors for all PLDs, including preloadable and non-preloadable PLDs, and PLDs that power up to known and unknown states. A powerful initialization algorithm is used to drive all initializable devices to a known state from any power-up states so that maximum testability can be achieved for both component and in-circuit testing.

GENERAL DESCRIPTION

PLDtest Plus and PLDtest accept files in the industry-standard JEDEC 3A format as input. The only information needed from the user is the fuse map of the PLD used. The output format produced by PLDtest Plus and PLDtest include both the JEDEC 3A format and the ABEL "include" format. As indicated in Figure 2, interfaces with industry-standard logic programmers and ATEs are also provided for functional testing as well as AC and DC parametric testing.

Currently these tools run on a variety of hardware platforms and operating systems including MS-DOS™, PC-DOS, VAX®-VMS®, SUN-3/4™, and Apollo®/Mentor™.

PLDtest Plus and PLDtest perform automatic test vector generation, fault grading, and testability analysis of the device under design or test. PLDtest Plus and PLDtest support a wide selection of devices, including the most popular non-preloadable registered devices, preloadable registered devices, and combinatorial devices. For a PLD design and device, with or without the preloadable feature, PLDtest Plus will:

- Determine how many possible faults there are in the device.
- Determine how many of those faults can be tested.
- Generate automatically the best set of minimum-length vectors to test those faults.

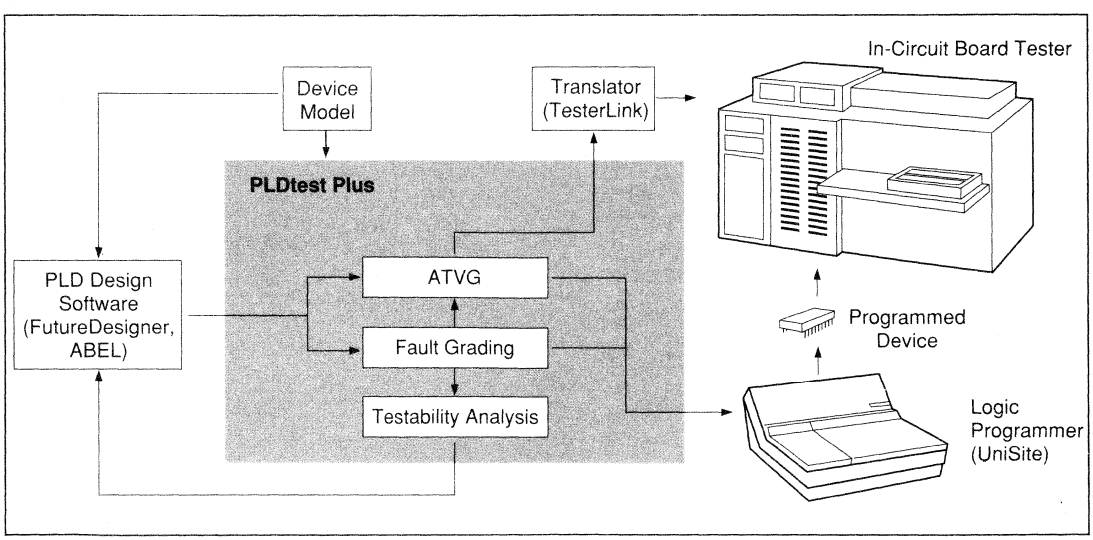


Figure 2. PLDtest Plus Interfaces with Industry-standard Logic Programmers and ATEs

- Generate the best set of test vectors in minimum real time.
- Provide a true and meaningful indication of fault coverage.

For designers, PLDtest Plus analyzes the testability of a circuit design and identifies untestable portions. For test engineers, it verifies that each programmed device is an accurate copy of the master.

Automatic Test Vector Generation

PLDtest Plus, using advanced and efficient algorithms, accelerates the generation of test vectors from days to minutes. PLDtest Plus supplements user-supplied test vectors or creates new test vectors, as required to achieve the maximum test coverage for the design, and for the targeted device.

Fault Grading

Fault grading determines how many points in the device could potentially fail when programmed with the intended design. Potential failures in PLDs are classified as device faults, parametric faults, or logic design faults. Device faults associated with the device's silicon elements are identified by PLDtest Plus in an output listing. The design faults can include fuses, the AND array, the OR array, input/output drivers/buffers, and registers. Any potential faults that go undetected by test vectors are also listed. Undetected faults require the generation of additional test vectors or possibly redesigning the logic equations for testability.

Design for Testability

Both PLDtest Plus and PLDtest contain design for testability features. The program will report if oscillation or race and hazard conditions are detected in the design. If there is low fault coverage, you can run an option to detect and report illegal states. If no illegal states exist, then low coverage is due to logic redundancy, oscillation, or a race and hazard condition. You can check the equations generated for the product terms to determine untested product terms. A modification of the design may be necessary to achieve higher fault coverage.

An option is available to automatically correct user-supplied seed vectors. If seed vectors are included, you can specify whether or not you want PLDtest Plus to correct faulty vectors. The initialization algorithm built into the program initializes registered non-preloadable devices to a known state from any unknown state for testing. It can also detect non-initializable designs and generate vectors from power-up states of all-high or all-low. Other design-for-testability features include printout of Boolean equations, testability per product terms, and illegal states in finite state machines (FSMs).

UNDERSTANDING AND USING PLDtest PLUS AND PLDtest

Fault Coverage and Fault Grading

The fault coverage reported by PLDtest Plus is the percentage of faults detected among all potential faults. The fault coverage can be used to measure the design for testability of the design. PLDtest Plus performs fault grading by using a fault model, and produces detailed documentation that shows specifically which test vectors test which faults for Stuck at 1 conditions and Stuck at 0 conditions. Figure 3 is an example of the report file produced by PLDtest Plus.

The report file includes information such as the input file name and the device type. If you were generating new test vectors along with fault grading, it will tell you if you included the seed vectors or if you generated a complete new set of vectors. It will also tell you if the program generated test vectors for a preloadable or non-preloadable PLD, and if non-preloadable, then what state was specified for the output registers to power up to; high, low or unknown. Next in the report file is a summary of the potential faults located within the device (how many fuses were left intact along which a signal can pass from input to output) and how many were detected by the test vectors, how many seed vectors and how many new vectors were generated.

Later in the output file is a detailed list of which vectors covered which fuses for stuck at conditions of stuck-at-0 and stuck-at-1. If PLDtest Plus or the user-supplied seed vectors detected 100% fault coverage, each fuse used in the device would be listed twice; once for a stuck-at-1 condition and once for a stuck-at-0 condition. Any fuses not detected by a test vector for one of the stuck at conditions would be listed under Undetected Faults in the report file. So how do these report files relate to actual fuse maps in the JEDEC. Look at the implementation of a design to find out. Figure 4 is an ABEL™ source file for a test case that uses only one output and two inputs.

Figure 5 shows how the equation !Out := (A & !Out) # (A & B) gets mapped into the device. In this example the output "Out" is connected to pin 19 and the inputs "A" and "B" are connected to pins 2 and 3. Figure 3 shows that pin 2 connects to the first two columns, the noninverting to column 0 and the inverting to column 1. Pin 19 feedback, which is considered an input, connects to the next two columns, the noninverting to column 2 and the inverting to column 3. Pin 3 connects to the next pair of columns, the noninverting to column 4 and the inverting to column 5. This device can use up to a maximum of 16 inputs at a time for each product term. The example also shows that there are eight possible product terms, or OR terms, which can be used for each output.

```
PLDtest Plus Version 1.12
=========================================================
PLDtest Plus Setup Configuration...
Input file:      RMICZO.JED
Device type:     P16R4
Including seed vectors.
Determine fault coverage of seed vectors.
Generating test vectors for non-preloadable device.
Power up state of registers will be all Low's.
Output file:     RMICZO.JDN
Report file:     RMICZO.RPT
_____________________Summary_____________________
!Pin15 = ((!( !(Pin2) [*]
# Pin15_QN) [*] ));
!Pin16 = ((!( !(Pin2) & !(Pin15_QN) [*]
# !(Pin16_QN) & !(Pin15_QN) [*]
# Pin2 & Pin16_QN & Pin15_QN) [*] ));
* = Full Testability
No Illegal Register States discovered.
Fault coverage:          100.0%
Seed Vector Coverage:      0.0%
Detected faults:         18      Seed vectors:          0
Undetected faults:        0      Generated vectors:    13
Total known faults:      18      Total vector count:   13
Circuit is initializable.
Initialization vector sequence:
V0001 C0XXXXXXXN0ZZHLXHZZN
V0002 C0XXXXXXXN0ZZHLLHZZN
PLDtest Plus complete. Time: 0:00:05
_____________________Detected Faults_____________________
_____Generated Vectors_____
Vector 1
S-A-0 fuse:     832   846    850   1074
Pin Number:      16    16     16     15
Vector 2
S-A-0 fuse:     783   787
Pin Number:      16    16
S-A-1 fuse:    1025  1074
Pin Number:      15    15
Vector 3
Vector 4
S-A-1 fuse:     787   846
Pin Number:      16    16
Vector 5
S-A-1 fuse:     783   801   850
Pin Number:      16    16    16
Vector 6
Vector 7
Vector 8
S-A-1 fuse:     819
Pin Number:      16
... Edited ...
Vector 13
S-A-1 fuse:     832
Pin Number:      16
_____________________Undetected Faults_____________________
```

Figure 3. Sample Report File

```
module fault flag '-r3';
title 'Example to demonstrate PLDtest Plus fault model'
u1 device 'p16r8';
A,B,OUT pin 2,3,19;
equations
!OUT := (A & !OUT) # (A & B);
end
```

Figure 4. ABEL Source File

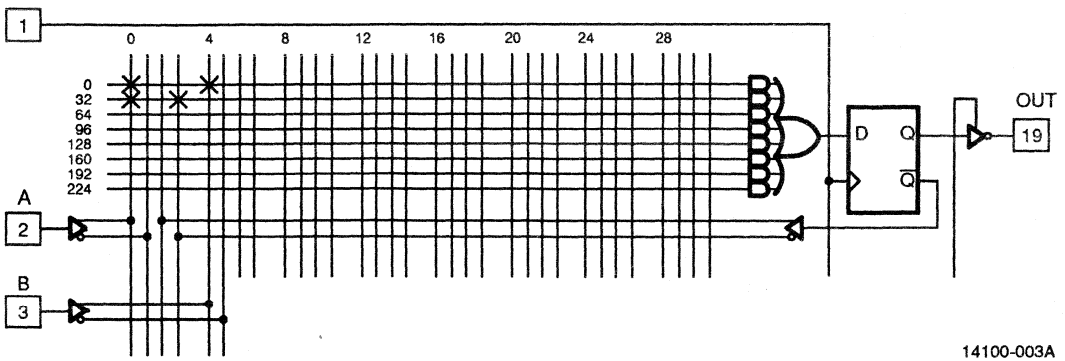


Figure 5. !OUT:= (A & !OUT) # (A & B) Equation as Mapped into a 16R8

The first term is actually the first OR term in the equation, A & !Out. That means that the first and the fourth fuses are left intact and all the rest in this row are opened. This leaves the noninverting input from pin 2 (fuse 0) and the inverting feedback from pin 19, !Q (fuse 3), connected to this product term. The second term, A & B, gets mapped into the second product term; "A" again in the first column (fuse 32), and the B in the fifth column (fuse 36).

As the report file in Figure 3 shows, there is 100% fault detection. The generated vectors test two types of potential faults in a PLD. By "potential faults," we mean all those faults that can occur in a PLD due to its manufacturing process or any other reasons. They do not necessarily occur in a given device, but PLDtest Plus generates vectors to detect them if they do occur. In other words, each intact fuse along these critical paths, or paths which signals can take to get from the input to the output, gets tested twice, once for a stuck-at-0 and once for a stuck-at-1. The report file tells us that test vector number 1 tests fuses 32 and 36 for a stuck-at-0 condition. Test vector 3 tests fuse numbers 0 and 32 for stuck-at-1 conditions, vector 6 tests fuses 0 and 3 for stuck-at-0 conditions and vector 9 tests fuses 3 and 36 for stuck-at-1 conditions. The faults associated with the inputs and outputs of the AND gates and the OR gates, tristates and registers along the output path are equivalent to the stuck-at-faults for these fuses (i.e., they can be detected by applying inputs to detected faults associated with a fuse and see the results at an output pin).

What about the rest of the fuses which were opened in each product term that is being used, how do we test those? There are four possible cases to consider. First, a blown fuse is actually intact and connected to V_{cc}. This is a minor case as unused inputs are pulled high anyway for unused AND gate inputs. Second, an opened fuse is connected and tied to ground. This is equivalent to a stuck-at-0 fault. These faults will be detected because as long as we generate enough vectors to test even one used AND gate, or toggle the output once, we have ensured that no opened fuse is actually intact and tied to ground. If there was an unused fuse tied to ground, the output could never toggle.

The last two cases are where the unused and opened fuse is actually left intact and tied to the input pin or the inversion of the input pin. The test vectors will test one of these two cases. Even if a "don't care" condition existed on all of the unused inputs, there would be an actual value, either a logic 1 or a logic 0, placed on these pins during software simulation, and by the actual device tester. Since the value placed on these pins by the device tester is unknown, it is unknown which condition will be tested, the pin itself or its inversion; but one of the two will be tested. The end result is that we test 75% of the unused fuses in the used product terms. In the cases that we can't test, where an unused and opened fuse is actually left intact and tied to the input pin, or the inversion of the input pin, there is an excellent chance that the fuse verify will catch it anyway if you are using a Data I/O

programmer, since these programmers run the fuse verification automatically.

Initialization

PLDtest Plus generates test vectors that can be used by a programmer and/or a board tester to detect manufacturing and component defects in PLDs. Non-preloadable PLDs can be broken down further into devices in which the output registers power up to a known state of all logic 1's or 0's (highs or lows), or power up into some unknown state. If the target PLD powers up to an unknown state then we must first generate an initialization sequence. The capability to generate test vectors for PLDs that power up to both a known or an unknown state is one of the major strengths of PLDtest Plus.

Initialization is the process of applying a sequence of vectors (V1, V2, ...,VN) to the inputs of a registered PLD so that the device will go from any state (a set of register values) when the first vector is applied, to a common or known state after the last vector is applied. This sequence of vectors is called the "initialization sequence" or sometimes "homing sequence." For example, a two-register PLD can have maximum four states (00, 01, 10, 11). To initialize it, a set of vectors has to be found that drives it from any of the four power-up states to a common final state. The PLDtest Plus initialization algorithm initializes registered non-preloadable devices to a known state for testing. Preloadable and combinatorial devices do not require initialization.

Example

An ABEL state description is shown in Figure 6 for a two-bit, four-state, design. This example will transition from state s0 to state s2 when the input D is equal to logic 1. If D is equal to logic 0, it will remain in state s0. When in state s1, depending on D, it will either go to state s3 or state s0. When in state s2, whatever the logical value of D, it will go to state s1. Finally, in state s3 it will go to either state s0 when D is logic 1, or state s1 when D is logic 0.

```
state s0: case(D==1) :s2;
  (D==0) :s0;
endcase;
state s1: case(D==1) :s3;
  (D==0) :s0;
endcase;
state s2: case(D==1) :s1;
  (D==0) :s1;
endcase;
state s3: case(D==1) :s0;
  (D==0) :s1;
endcase;
```

Figure 6. ABEL Design Description

The initialization sequence that PLDtest Plus generates for this test case is shown below. It comprises two test vectors and will take this circuit from any of the four defined states to a single state; in this case to state s0. Notice that in the test vector sequence it applies the logic value of 0's on pin 2 (this is the D input) in test vectors 1 and 2. Note that pins 14 and 15 are both being tested for L, or logic low, after the initialization sequence.

```
V0001 C0XXXXXXXN0XXXXLXXXN
V0002 C0XXXXXXXN0XXXLLXXXN
```

Figure 7 shows the bubble diagram for this circuit and more clearly defines the sequence of state transitions as defined by the ABEL example. The state values are inside each circle, and the 1 or 0 on the arrow shows the transitions from state to state depending on the logic level of input D. If a sequence of two 0's are applied to the D input, no matter what state you start from, it will always end up in the state s0 (00). This is initialization.

Why is this ability to initialize a PLD important? Not all circuits can be initialized and non-preloadable devices which are non-initializable cannot be tested from an unknown power-up state. This is important from a designer's standpoint because it affects the ability of the system to operate, such as when a microprocessor needs to put the PLD into a known state. The software engineer can also use the initialization sequence in his code to initialize the PLD in-circuit.

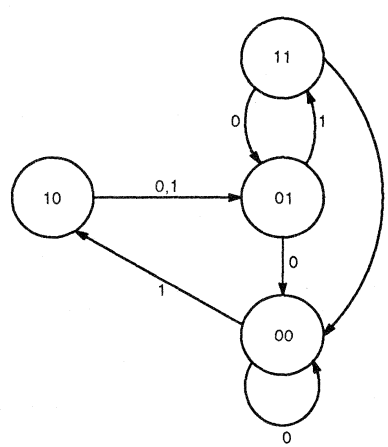


Figure 7. Bubble Chart

To a test engineer, the non-initializable device presents a number of problems. Initialization is important because it directly impacts testability of the PLD involved. The fault coverage for a non-initializable device is generally lower compared to that of an initializable device and therefore the reliability requirements in terms of percent of fault coverage may not be satisfied. For a non-initializable device, there is no initialization sequence of

vectors that can be used to reinitialize or resynchronize test vectors. If the generated vectors have to be segmented due to vector length limitations of a particular device programmer or automatic test equipment, then the test will have to be cut at the point where the vectors reach the upper limit of the test equipment. If using initialization sequences, the engineer can cut the test after one such test sequence, then load more vectors to finish the test process. Also, in doing a series of tests on different PLDs on a board, the PLDs would be tested individually and power must be cycled between device tests in order to satisfy the power-up state requirements for a non-initializable device. This is because all the vectors generated were based on a specific power-up state.

Finally, knowing if a circuit is initializable is important to the production engineer because it will determine what type of PLD is ultimately selected, one which powers up to a known state, or one that powers up to an unknown state. This will have a direct impact on the options a purchasing agent has when procuring devices.

Not all circuits are initializable; it is possible for as little as one-half of the PLDs tested to be initializable. Figure 8 is the ABEL description for a non-initializable circuit. The single control input, D, will either cause this circuit to advance to the next state or remain in the current state.

```
state s0:  case(D==1)  :s1;
               (D==0)  :s0;
           endcase;
state s1:  case(D==1)  :s2;
               (D==0)  :s1;
           endcase;
state s2:  case(D==1)  :s0;
               (D==0)  :s2;
           endcase;
```

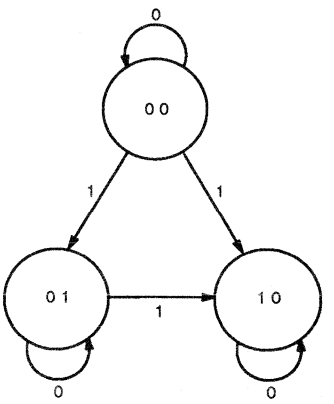
Figure 8. ABEL Description, Non-Initializable State Machine

Note that it is impossible to generate a sequence of vectors that will take this circuit from any of the three displayed states to a single state. Figure 9 clearly shows the interaction of the states and state transitions. We can only test this circuit from a known power-up state, either all 1's or all 0's.

The addition of a reset condition in the original logic description would cure this problem. The decision has to be made to use a device that powers up to a known state, all highs or all lows, or redesign this circuit so that it can be initialized.

When generating test vectors from a known power-up state, the actual power up state can also have an impact on the testability of a design. Using PLDtest Plus can help you determine which device to select.

Before a particular vendor is selected, run PLDtest Plus from both power up high and low and get a difference on



14100-005A

Figure 9. Non-Initializable State Machine

fault coverage. This data can then be used to select a device, from the same vendor or a different one, with a power-up state that satisfies testability requirements.

Specific device power-up state information can be found in the device manufacturers' Data Books or Device Specification Sheets. Once this information is obtained and provided as input to PLDtest Plus, the product will search for vectors starting from the user specified power-up states instead of searching for an initialization sequence.

PLDtest Plus always tests for the initializability of a design as the first step in the automatic test vector generation process. PLDtest Plus does not need user-supplied seed vectors (to test the design) to initialize a PLD, but if seed vectors are provided, PLDtest Plus will generate additional vectors following the seed vectors and will generate an initialization sequence of vectors independent of the seed vectors.

Boolean Equations for Pins

Boolean equations for each output pin are written to show testability for product terms. The equations are written to the report file, and specify whether each product term is fully tested, partially tested, or not tested by the seed and/or generated vectors. With the testability information thus provided, the user can go back to the design equations of the PLD involved to make the necessary changes to improve testability.

Illegal States in FSMs

As an option, detected illegal states for finite state machine design are written to the report file. The user can thus understand why a design may have low testability if too many illegal states are detected in the design, since the faults associated with these states are generally not detectable.

Pins Reported for Stuck-at Faults

In the report file, pin numbers are given below the fuse numbers for each stuck-at fault. The pin numbers refer to the output pin where the fault was detected. This information indicates that all faults along the critical path from the fuse number to the pin number are detected with that vector.

COMPARING PLDtest PLUS AND PLDtest

PLDtest Plus is a new product which handles both preloadable and non-preloadable PLDs, as indicated in Figure 10, while PLDtest handles only preloadable and pure combinatorial PLDs (e.g., P16L8).

Preloadable PLDs have built-in circuitry to allow registers to be set to 0s or 1s as required for testing. A supervoltage is applied to the appropriate pins to force the registers into the desired states. Once all registers are set to known states, the test generation problems are similar to that of combinatorial circuits. Heuristic techniques have been developed to allow efficient test generation for preloadable PLDs, and the vectors thus generated normally achieve high fault coverage.

A preloadable PLD allows all state transitions in a finite state machine to be tested thoroughly because the FSM can be set to any initial state, including an illegal state. Access to these illegal states makes it possible to detect faults that would not normally be detectable. As a result, higher fault coverage can be achieved.

Because the registers can be directly loaded into any desired state, a long initialization sequence of vectors is not needed to drive the registers into a state to detect faults, and therefore a minimum number of vectors are usually generated for preloadable PLDs. In a component tester, or a PLD programmer with preload capability, the test vectors perform well. However, preloadable PLDs cannot always be used in an in-circuit testing environment since the super-voltage applied to the pins in a PLD sometimes damages other devices connected to it. PLDtest Plus was designed specifically to generate test vectors for non-preloadable PLDs.

PLDtest PLUS AND PLDtest DEVICE SUPPORT LIST

AMD Part No.

16L8	20R6
16R4	20R8
16R6	20X10A
16R8	20X4A
18P8	20X8A
20L10	22P10
20L8	22V10
20R4	

For more information, contact:

Data I/O Corporation
(800) 247-5700 or (206) 881-6444

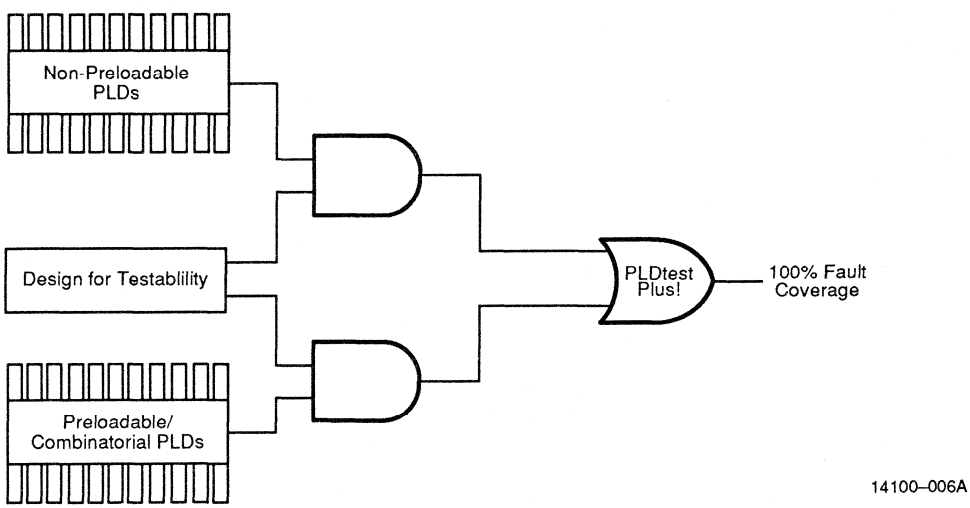


Figure 10. PLDtest Plus Capabilities

AUTOMATIC TEST VECTORS FOR PROGRAMMABLE LOGIC DEVICES

Anvil ATG software, from Anvil Software, Inc., automatically generates high-coverage functional test vectors for all types of Programmable Logic Devices (PLDs), including PAL® devices, programmable logic sequencers, and other architectures. These vectors are applied after programming, either on the programmer, on a device tester, or during in-circuit testing. Testing the PLDs individually, prior to functional board test or system test, results in large savings in testing, diagnosis, repair, and inventory costs.

The Anvil ATG product is composed of an event-driven time-based simulator, concurrent fault simulator, general-purpose automatic test vector generator, a menu interface, and support programs. It is written in C and currently runs on PC-XT™, PC-AT™ and compatibles with 640K RAM and 4MB available disk space, 386-based PCs, and VAX®/VMS® systems. Support for additional host computers will be available in the future.

Functional Tests, No Preload

Anvil ATG software produces functional tests that operate the device as it will be used in the final application. No preload, "jam load," or other testing shortcut is used.

High Fault Coverage

Anvil ATG software typically achieves 90–100% detection, even on highly sequential designs (such as state machines) and designs where feedback creates memory (as in a 16L8). Faults considered are:

- Logic gates stuck-at-0 and stuck-at-1
- Programmed (opened) fuses faulted intact
- Intact fuses faulted programmed

Faults that are undetectable (due to redundancy or because they are in unused circuitry) are removed automatically so they do not obscure the true fault coverage. A typical 16R8 design has about 1200 detectable faults, while a typical 22V10 design has 3500 detectable faults.

Reliable and Repeatable Tests

Anvil ATG software monitors the effects of tester skew during simulation and masks out any output states that are not reliable and repeatable. In addition, any conflicts between the tester and chip are identified and fixed automatically. Any vectors provided by the user are checked for races, conflicts and other problems, and are corrected automatically.

Flexibility

The test generation algorithms support a wide variety of design practices, including multiple clocks, feedback-induced memory elements, asynchronous presets and resets, and any macrocell configuration. Good results are obtained even for asynchronous 20RA10 designs. Test generation uses a general-purpose proprietary algorithm that is fault-driven and uses critical path analysis techniques.

Vector Minimization

Three user-selectable levels of vector minimization solve problems with older testers that have limited vector memory.

Easy to Use

Anvil ATG software is operated through a simple menu and fill-in-the-form interface. The menu can be bypassed in order to run a series of jobs in batch mode without operator attention. An easy-to-read manual is provided with the software, complete with an example, descriptions of the options, and suggestions of how to configure the software most appropriately to match your test equipment and test philosophy.

Run-times for 20-pin PAL devices are typically just a few minutes on a fast PC.

Industry-standard Interfaces

Anvil ATG software reads the fuse information from the JEDEC standard fuse file which all commercial design software produces and which all programming equipment reads. When the vectors have been generated, they are written back to the JEDEC file, again using the industry-standard formats.

Model Libraries

The Anvil ATG products are available in a variety of configurations and prices, based on the number of models

and feature set needed for a particular application. Models available include the following AMD devices:

16L8	16R8	16R6	16R4
20L8	20R8	20R6	20R4
20L10	20X10	20X8	20X4
16V8	20V8	18P8	22P10
16RA8	20RA10		
22V10	26V12*	32VX10*	23S8
105	167	168	
10H/10020EV8		10H/10020EG8	

* These models require 386 or VAX/VMS configurations.

Other models will be developed as needed by customers:

24L10	24R10	24R8	24R4
24V10	22IP6	29M16*	30S16*

* These models require 386 or VAX/VMS configurations.

Tester Support

Translators are available for the following testers:

Sentry, GR 1732, GR125, IMS
GR227x, Schlumberger, Teradyne L200
HP3065/3070, Logue McDonald

Call Anvil for information on these and other testers.

Since a PLD may be constrained by surrounding circuitry on the circuit board, Anvil ATG software can be told which pins are tied high, low, together or are inaccessible, and generate vectors for an in-circuit tester accordingly.

In-circuit board test support includes automatic generation of digital guarding vectors (inhibits and disables).

The power-up state may be specified by the user as "unknown," "all registers low," or "all registers high." Seed vectors may be provided to assist with uninitializable designs.

Update Service

Updates during the first year are included with the product purchase. The update service includes bug fixes and enhancements to the software, documentation and individual models plus telephone support. New models and major new software capability are not included in the update service — they are considered new products.

ANSWERS TO COMMON QUESTIONS ABOUT ANVIL ATG SOFTWARE

Why does Anvil ATG Software use the JEDEC fuse maps instead of equations?

The reason we use the JEDEC fuse map is to allow us to get better accuracy and to avoid incompatibility problems with the many different equation formats that different designers use. The fuse maps tell us the state of every fuse as it is actually programmed in the device. The Boolean equations do not necessarily tell us the exact fuse pattern, because different optimization techniques can be performed by different equation compilers and result in different arrangements of the fuse bits. We feel that you should test the devices exactly as they are programmed in order to get the best test yields.

The other major reason we prefer the JEDEC fuse map is that there are many different equation formats. The JEDEC fuse map format, on the other hand, is an industry standard. All programming equipment reads this JEDEC format and all PLD design software produces this JEDEC format. It is therefore a reliable source to get the information that we need to generate the test vectors.

Why does Anvil ATG software consider so many faults?

Anvil ATG software allows the user to choose what classes of faults are to be considered. Some users may just want to look at, or test for, logic faults whereas others may want a functional test for each of the fuse states. Anvil ATG software can create functional tests to check each intact or programmed fuse. We believe that the most thorough test for a programmable logic device will test each fuse to make sure that it is not incorrectly programmed, or partially programmed, or that there is no short or other defect in the vicinity of the fuse. If you look at the construction of most PLDs, you will realize that most of the chip area is consumed by the fuse array. This means that the fuse array is the most likely place for failures to occur.

Another factor to consider is that programmable logic devices can have a defect rate ranging up to one percent, even after the fuses are read back on a programmer. This means that it is desirable to test for as many faults inside the PLD as possible. That is precisely why Anvil ATG software offers the user the option of testing for thousands of faults inside even small PLDs.

Why isn't fuse verify on the programmer good enough?

Fuse verification on the programmer is done through the same fuse addressing logic as used during programming. A fault in the fuse addressing logic could cause the wrong fuse to be programmed, but the fuse state would look right during readback because the same faulty addressing logic would be used.

Another common problem not caught by fuse readback is programming the wrong part. If a 16R8 is used instead of a 16L8, the fuse readback will pass but the part will not behave as desired in the end application.

Vectors produced by Anvil ATG software will catch both of these failures and many others that are missed by fuse verification on the programmer.

What causes PLD defects?

PLD defect rates typically run up to 1% after programming and fuse verification on the programmer. The actual rate depends on manufacturer, programmer calibration, device handling, and lot-to-lot variations. These defect rates can even occur on some lots from manufacturers who test erasable devices prior to shipment. Some of the reasons for defects are:

- Programming equipment needs to be recalibrated regularly.
- The manufacturer does a generic test, whereas optimum quality is obtained by testing with the specific fuse pattern used in the final application. Manufacturers of erasable parts can only program and test for a limited number of the many possible patterns.
- Devices get mislabeled.
- Wrong device types are sometimes used (e.g., 16L8 instead of 16R8).
- Infant mortality failures are only observable after burn-in.
- Fuses sometimes are not programmed completely, thereby leaving shorts or timing faults. This is particularly likely to be true if the PLD does not make good contact in the programming socket due to dirt or an old socket.

How many vectors does Anvil ATG software create?

The number of vectors created by the software depends on the option settings selected by the user. The user can specify the maximum number of vectors, such as 1023, to accommodate the limitations of some testers and programmers. A second way to control the number of vectors is by selecting the groups of faults to be considered. If the user wants to test for each programmed fuse faulted intact, there will be twice as many vectors generated than if the user just wants to consider logic faults and intact fuses faulted programmed. Anvil ATG software can also accommodate testers that allow multiple bursts. By specifying the tester burst size, vectors will be produced in one or more bursts as necessary.

Anvil Software has recently made improvements to minimize further the number of vectors produced. The types of optimizations performed include: (a) superimposing vectors so that several parts of the chip can be tested simultaneously, and (b) removing vectors that are duplicates or do not detect any faults. Other optimizations are performed during the vector generation to detect as many faults as possible in the early vectors of the test.

How do I know it will work on my parts?

Anvil Software has a number of ways to allow you to evaluate the capabilities of our software. Our customers have generated test vectors for more than 20,000 PLD designs, and several customers have each done more than a thousand PLD designs. We have observed success rates higher than ninety percent on a typical mix of programmable logic designs, and we are willing to put you in touch with some current customers so you can hear about their experiences first hand. Our No Charge Benchmark Test offer allows you to send two JEDEC files and we will generate test vectors for them and send you the results.

Will Anvil ATG software be able to support next year's devices?

There are two aspects of how Anvil Software does business that keeps its customers current with the latest technology. The first is our model development program, where we will develop a model for a new PLD device as soon as a customer is willing to provide us with a purchase order and some sample designs to allow us to verify the correctness of our simulation model.

The other aspect of the way we do business is the annual update service that we offer to our customers. This service allows customers to telephone with questions, to send us PLD designs that they are having difficulties with, and allows them to receive the latest improvements to the software and models that they have purchased from us. This means that when we improve the test generator to work well on a new generation of devices, these customers will receive the improvements.

We depend on our customers to tell us which devices are most important to do and we have found that we have consistently kept up with the devices that are in volume manufacturing. For a complete list of models that we have completed or are under consideration, call Anvil for our latest model status.

How long does the vector generator take to run?

The run time depends on the clock rate of your computer, the number of faults selected, and the complexity of the design. Typical 20-pin PAL devices with logic and intact fuse faults selected, where the design is typical complexity, take between one and five minutes to run on a 20-MHz 386 computer. More complicated devices such as a 22V10 can take several times as long, and, if you wish to consider programmed fuses faulted intact, you can expect to spend twice as much computer time.

The main trade-off that we have made is based on our assumption that users are willing to spend a few extra minutes of CPU time in order to save hours of debug time on the tester. It can be very time-consuming to track down strange behavior on the tester due to races or other problems in test vectors. Anvil ATG software produces test vectors that will run correctly on the tester with no debug, no races and no other problems.

Contact:

Anvil Software, Inc.
427-3 Amherst Street, Suite 391
Nashua, NH 03063
(603) 891-1995

Test Generator™

ATG Associates

ATG Associates has provided Test Generator in response to the need for a fully functional Automatic Test Generation package, which provides:

- High fault coverage
- Fast operation
- Coverage for a wide range of PAL® Devices
- Cost-effective Test Generation

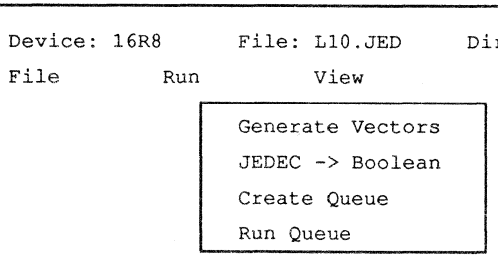
Test Generator works with any valid JEDEC file, with or without existing test vectors. It also works with any PAL device regardless of whether or not the device supports preload.

FEATURES

- Proprietary algorithm provides high coverage with significantly reduced run times
- Runs on any IBM PC™ compatible running DOS 3.0 or higher
- Supports devices that do not have preload and/or power-up reset capability
- For customer concerned about using supervoltage initialization or preload on their parts the following options are supported:
  - No use of supervoltages
  - Use only at beginning of vectors (once)
  - Use when necessary
- Generates vectors for all AMD PAL devices
- Has easy-to-use menu interface
- Convenient batch mode allows user to queue up to 50 jobs to run unattended
- Supports testing of three-state outputs and preset/reset of internal registers
- JEDEC to Boolean disassembly for any supported device

For further information contact:

ATG Associates
Customer Service
3415 Merrill Road
Aptos, CA 95003
(408) 475-5717



Test Generator Menu Interface

Terminating High-Speed PAL® Devices

INTRODUCTION

As system speeds have increased, designers have been requesting increasingly higher performance from their PAL devices. In the past, it has been possible for manufacturers to increase the device speed merely by reducing the internal delays of the part. Now, however, it has become impossible to design a 7.5-ns device with 4- or 5-ns rise and fall times, so the rise and fall times have been decreased to help speed up the devices.

Once the rise and fall times of a signal have dropped to a time that approximates the actual propagation delay of the signal on the wire, the realm of transmission lines has been entered. When this happens, the signal may become distorted due to reflections on the line. If severe enough, these reflections can cause such problems as gross overshoot and undershoot, extended ringing, crosstalk, and increased high-frequency emissions.

The reflections are caused by discontinuities in the impedance of the signal path, otherwise known as "impedance mismatches." In digital circuits, these usually occur at the end of the line; therefore, this becomes an issue of terminating the signals correctly. This application note will describe termination fundamentals, and compare the two basic termination schemes: serial termination and parallel termination.

Transmission Line Model

A transmission line can be represented by a lumped constant RLC circuit of unit length, as shown in figure 1.

When dealing with digital circuitry on a pc board, both the resistive and conductive components are usually insignificant, and are ignored during transmission-line calculations. Called a lossless and loadless transmission line, this model can be represented by the following differential equation:

$$\frac{d^2}{dx^2} v = L_0 C_0 \frac{d^2}{dt^2}, \qquad (1)$$

where: v = velocity

x = displacement along the line

t = time

L_0 = inductance per unit length of the transmission line

C_0 = capacitance per unit length of the transmission line.

Using convolution and Fourier analysis, the solution of this differential equation is as follows:

$$v = \frac{1}{\sqrt{L_0 C_0}}. \qquad (2)$$

The propagation delay, t_{PD}, of a unit length is therefore expressed as

$$t_{PD} = \sqrt{L_0 C_0}. \qquad (3)$$

The inductance and capacitance in the presence of a ground plane are a function of the dielectric medium and pc-board layout. Unit values of the inductance and capacitance can be measured by an LC meter. In general, transmission line effects can be simulated in both time and frequency domains with the SPICE circuit-analysis program.

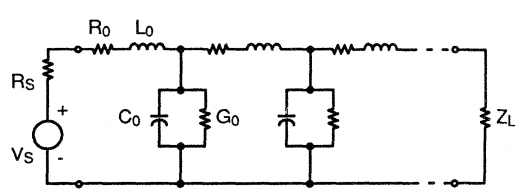


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Figure 1. Equivalent Circuit of a Transmission Line

Transmission Line Geometries

Circuit interconnections for high-speed digital systems generally include the following types:

- connectors
- wire over a ground plane
- twisted pair
- coaxial cable
- microstrip line
- strip line

Connectors generally cause wave-shape distortion when transition times are under 1 ns. The transmission-line effects of wire over a ground plane are uncontrollable; this type of interconnection is usually used for

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prototypes only. Twisted pair and coaxial cable are generally reserved for applications such as differential lines and video cable. The remaining two types of interconnections, microstrip and strip line, are the most practical for high-speed digital systems and will be discussed here in detail.

A microstrip line (figure 2a) is a metal-strip conductor on the pc board, separated from a conducting plane with a dielectric medium. The characteristic impedance Z_0, which is the ratio of voltage to current for a traveling wave at any given point and instant, is

$$Z_0 = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98\,d}{0.8\,w + t}\right), \quad (4)$$

where e_r is the dielectric constant of the board material. This equation is fairly accurate for a w/d ratio between 0.1 and 3.0 and for e_r between 1 and 15. For G-10 fiber-glass epoxy boards, e_r is about 5.0.

The equations for inductance per foot, L_0, and propagation delay per foot of the line, t_{PD}, are

$$L_0 = Z_0^2\, C_0 \quad \text{and} \quad (5)$$

$$t_{PD} = 1.017\sqrt{0.475\,e_r + 0.67} \ \text{ns/ft}, \quad (6)$$

where C_0 is capacitance per foot.

A strip line (figure 2b) is a metal-strip conductor centered in a dielectric medium between two conducting planes. The characteristic impedance, Z_0, is

$$Z_0 = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.67\,\pi\,w\,(0.8 + \frac{t}{w})}\right). \quad (7)$$

This equation is fairly accurate for

$$\frac{w}{b-t} < 0.35 \quad (8) \quad \text{and} \quad \frac{t}{b} < 0.25. \quad (9)$$

The equations for inductance per foot and propagation delay per foot of the line are

$$L_0 = Z_0^2\, C_0 \quad \text{and} \quad (10)$$

$$t_{PD} = 1.02\sqrt{e_r}\,. \quad (11)$$

The characteristic impedance of both microstrip and strip lines can be held within 5% if all the variables (e_r, w, d, t) are controlled. Also, note that the propagation delay of both microstrip and strip lines is not a function of the pc board geometry, but of the dielectric constant only.

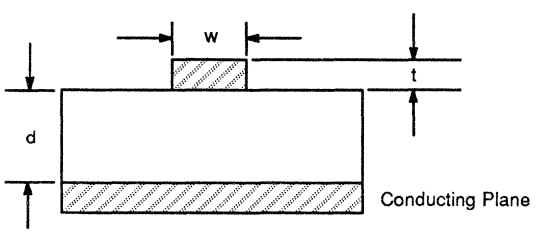

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Figure 2a. Cross Section for Microstrip Line

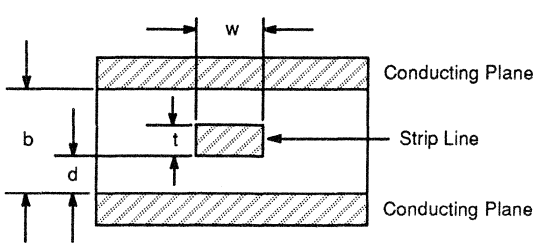

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Figure 2b. Cross Section for Strip Line

Reflections on the Transmission Line

Reflections on the transmission line are caused by a discontinuity of the line impedances, and are a major source of noise in digital systems. The discontinuity can appear as an input device, another circuit, a connector, or another transmission line.

Figure 3 shows the signal reflection and flow-through at the impedance discontinuity between transmission lines TL1 and TL2. The voltage reflection at the point of discontinuity travels back through TL1 with a magnitude of ρV_i, where ρ is the reflection coefficient and V_i is the incident-wave voltage.

The reflection coefficient is the ratio of voltage in the reflected wave to that in the incident wave as follows:

$$\rho = \frac{V_r}{V_i}. \quad (12)$$

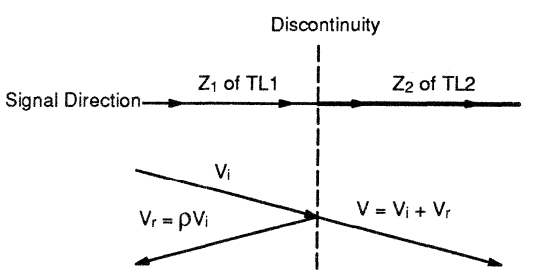

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Figure 3. Signal Reflection at a Discontinuity

The signal flow-through is $V_i + V_r$, where V_r is the reflected-wave voltage. From

$$V_r + V_i = V \quad (13)$$

and

$$\frac{V_r}{Z_1} - \frac{V_i}{Z_1} = \frac{V}{Z_2}, \quad (14)$$

we obtain

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}, \quad (15)$$

where Z_1 and Z_2 are the characteristic impedances of transmission lines TL1 and TL2 respectively.

Figure 4 is an example of a basic transmission line with a discontinuity at both the source and load. In this basic reflection mode, fanout is one. A lattice diagram is widely used to illustrate the reflection effect on a transmission line. Two vertical axes, for the source and load, are the time scales. The signal bouncing back and forth along the transmission line is shown as a diagonal line from top to bottom.

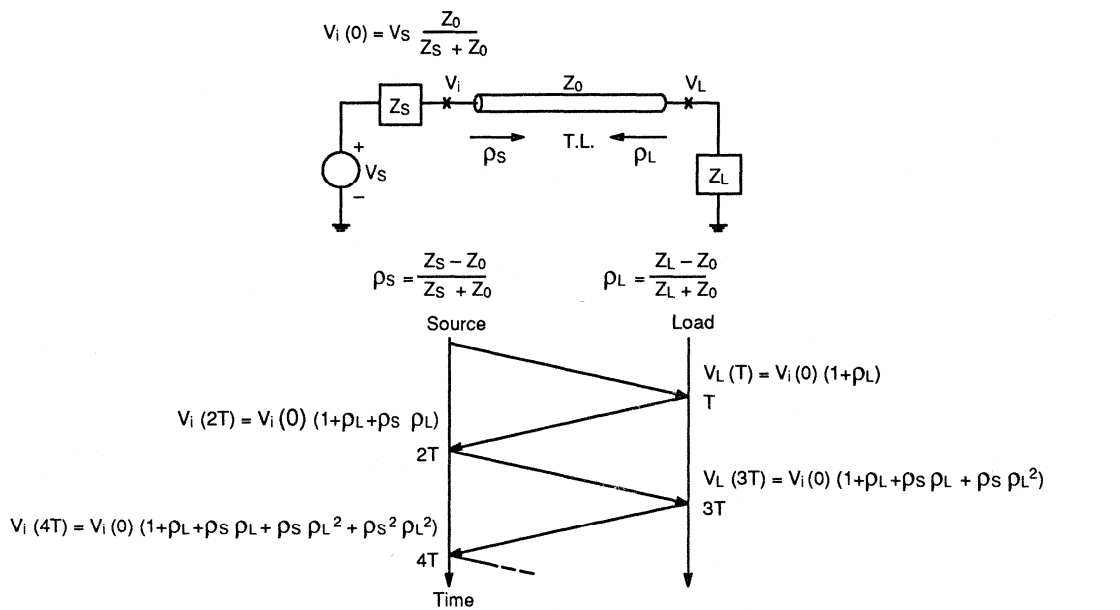

Figure 4. Example of Basic Transmission Line Circuit and its Lattice Diagram

The voltage V_i is the result of a voltage division between the source impedance Z_S and the line impedance Z_0. The voltage at each time interval is the algebraic sum of the reflection voltages from the top to the specific diagonal line. For example, the voltage at 4T is

$$V_i(0)(1+\rho_L+\rho_L\rho_S+\rho_L^2\rho_S+\rho_L^2\rho_S^2), \quad \textbf{(16)}$$

where: ρ_S is the reflection coefficient at the source,

and ρ_L is the reflection coefficient at the load.

Figure 5a is a numerical example of the lattice diagram; note that V_i and V_L eventually reach the same steady-state voltage, as shown in figures 5b and 5c.

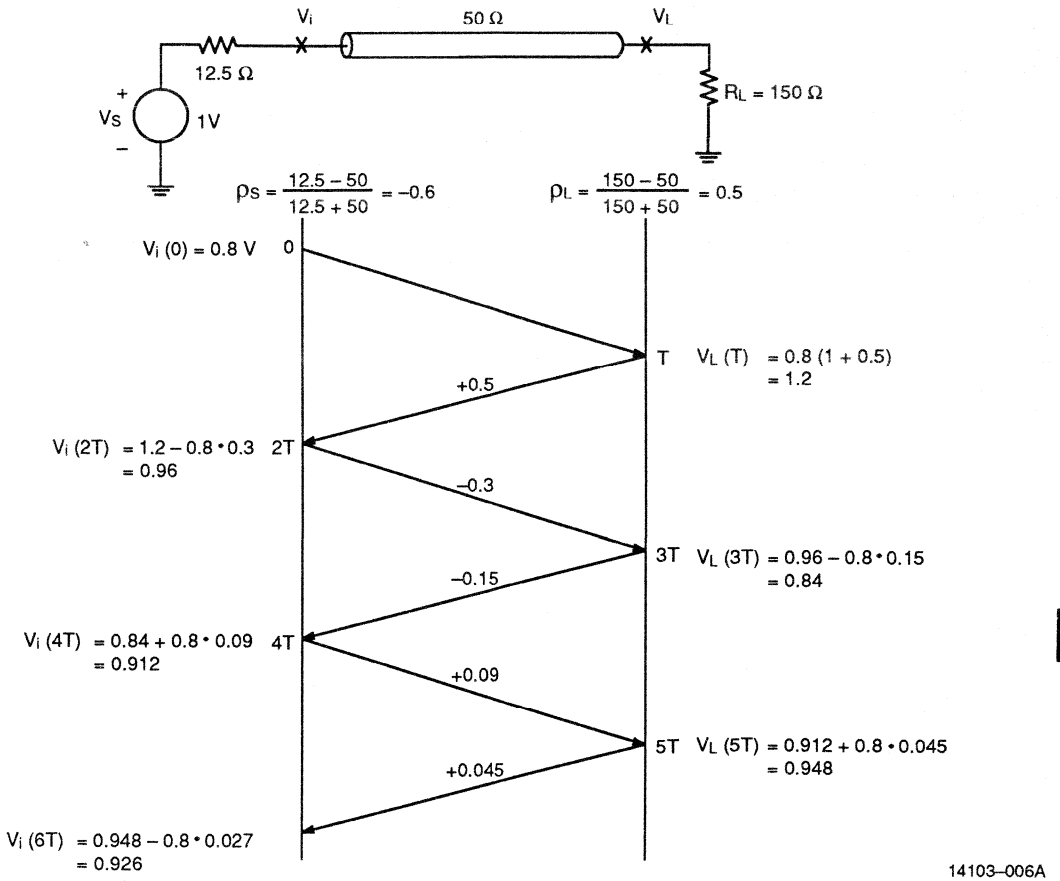

Figure 5a. Numerical Example of Lattice Diagram

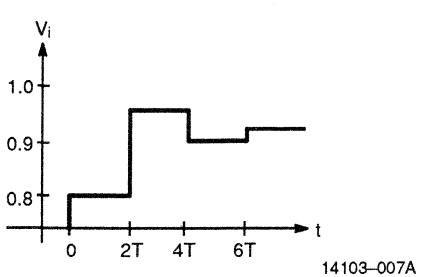

Figure 5b. Voltage at V_i

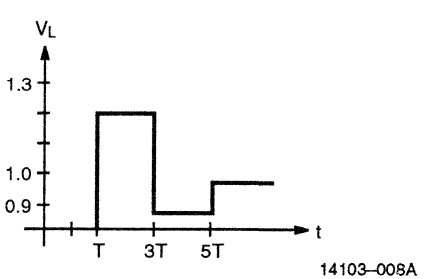

Figure 5c. Voltage at V_L

Only the transmission line effects that cause severe overshoot or undershoot need to be addressed. The rest, as long as they do not degrade the signal or interfere with data transmission, can be ignored.

The terms "overshoot" and "undershoot" are often used in different ways by different people. For this discussion, overshoot is defined as a transient voltage that is outside the expected steady-state logic-HIGH to logic-LOW range; that is, a signal transition that passes, or overshoots, its destination. This can happen on a rising edge or a falling edge. Undershoot is a transient voltage that is inside the expected steady-state logic-HIGH to logic-LOW range. Undershoot normally follows overshoot as the signal tries to stabilize itself, over corrects, and crosses over its destination in the other direction.

The degree of overshoot depends on the ratio of the edge speed of the driving gate, t_R, to the propagation delay of the line, τ. Empirical results show that small changes in the t_R/τ ratio or the decrease in length of the transmission line can cause a significant change in overshoot. Table 1 provides the percent overshoot corresponding to various t_R/τ ratios in a system[2] with $R_0 = 5\ \Omega$, $R_L = 4.6\ k\Omega$, and $Z_0 = 75\ \Omega$. This ratio is directly proportional to the edge speed and inversely proportional to the length of the transmission line. Therefore, the faster PAL device families require shorter line lengths to provide the same $t_R{:}\tau$ ratio as the slower families, which can have relatively longer line lengths.

The tolerable amount of overshoot varies with the type of device being driven. Conservatively, let us assume that less than 25% is tolerable for typical TTL devices. Then, from table 1, a design with edge rate four times the transmission line propagation delay t_{PD} is considered to be a reliable design. In addition, such bus standards as the EIA Standard RS 422/232 Bus require a 4-to-1 ratio of edge rate to line propagation delay.

As we saw in equation (3), the intrinsic capacitance C_0 and inductance L_0 determine the speed of signal transmission on an unloaded line. For a loaded line, the distributed capacitance C_d, which is calculated by adding the input capacitances of all the receiving gates, must be included in the propagation-delay calculation.

$t_R : \tau$	% overshoot at the end of loaded line
1 : 1	87%
2 : 1	63%
3 : 1	30%
4 : 1	10%
6 : 1	5%
8 : 1	0

Table 1. % Overshoot due to Transmission Line Effects

$$t_{PD}' = \sqrt{L_0 (C_0 + C_d)} = t_{PD}\sqrt{\left(1 + \frac{C_d}{C_0}\right)} \quad \textbf{(17)}$$

Therefore, the signal propagation down the line is delayed by a factor of

$$\sqrt{\left(1 + \frac{C_d}{C_0}\right)} \quad \textbf{(18)}$$

Terminating Transmission Lines

As we have seen, faster signal edge rates can be accommodated most easily by shortening line length to keep the t_R/τ ratio at 4:1 or greater. If lines cannot be shortened enough to provide this ratio, termination techniques must be used to reduce the impedance mismatches. Without proper termination, severe undershoot or overshoot may violate the system noise margins, cause unexpected device behavior, or damage the device.

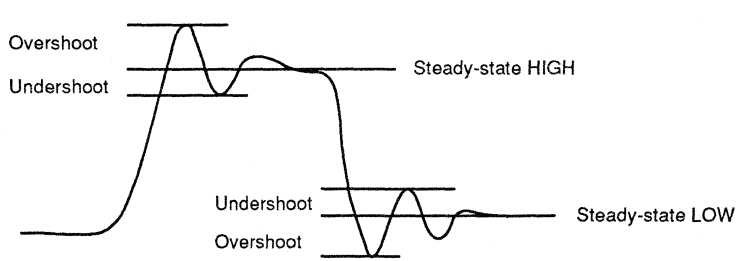

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Figure 6. Overshoot and Undershoot Terminology

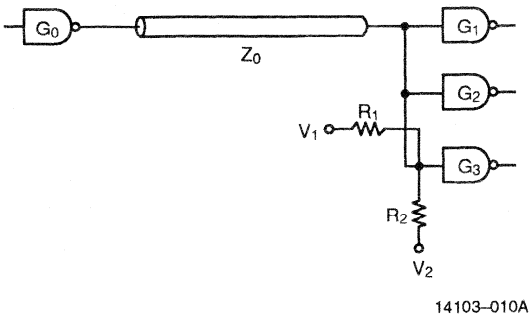

Figure 7a. Lumped Load Termination

	V_1	V_2	R_1	R_2
TTL, CMOS	5 V	GND	$2Z_0$	$2Z_0$
ECL	GND	–5.2 V	1.63 Z_0	2.60 Z_0

Figure 7b. Resistor Values for Different Logic Families

There are several different ways of terminating transmission lines. The two most efficient and most widely used schemes are parallel and serial termination.

Parallel Termination

Parallel termination is used for driving lumped loads or high-speed circuits. Using this technique, the Thevenin equivalent of terminating resistors R_1 and R_2 should be the same as the line impedance. A typical parallel termination scheme is shown in figure 7a. Resistor values for different logic families are given in figure 7b. Daisy-chained routing is suggested for pc design to reduce complicated multi-level reflections. In this example, fanout equals three, and parallel resistors are inserted on the last gate input or at the end of the daisy chain. Fanout is limited by the current that driving gate G_0 can sink from the input gates G_1 - G_3.

The parallel-termination technique in figure 7a uses dual resistors and a single power supply. It is possible to use a single resistor with a Thevenin equivalent of the two resistors. This would require a second power supply which is usually not available, and therefore would be costly.

Parallel termination is also used for driving distributed loads, but the termination resistor values are determined by calculating an impedance adjustment. The adjusted impedance, which is usually different from the intrinsic line impedance, depends on the load distribution along the transmission line, and determines the value of the termination resistors.

Figure 8 shows a 12-inch 64-Ω microstrip transmission line with a distributed fanout of 3. Each load has an input capacitance of 6 pF.

With a lumped load and receiving gates grouped in a daisy chain at the end of the transmission line as in figure 7a, R_1 and R_2 should be equal to 64 Ω x 2 = 128 Ω. However, with a distributed load, an adjusted line impedance Z_0' must be calculated. For a microstrip line with e_r = 4.7, the propagation delay is 1.77 ns/ft.; therefore, the adjusted line impedance for the example is calculated as follows.

Since

$$C_0 = \frac{t_{PD}}{Z_0} = \frac{1.77\ \text{ns/ft}}{64\ \Omega} = 2.30\ \text{pF/inch}, \quad \textbf{(19)}$$

hence,

$$C_d = \frac{6\ \text{pF} \times 3}{12\ \text{in}} = 1.5\ \text{pF/inch}. \quad \textbf{(20)}$$

Therefore,

$$Z_0' = \frac{Z_0}{\sqrt{1 + \frac{C_d}{C_0}}} = \frac{64\ \Omega}{\sqrt{1 + \frac{1.5}{2.3}}} = 49.8\ \Omega. \quad \textbf{(21)}$$

In this case, $R_1 = R_2 = 2\ Z_0' = 100\ \Omega$ (approximately).

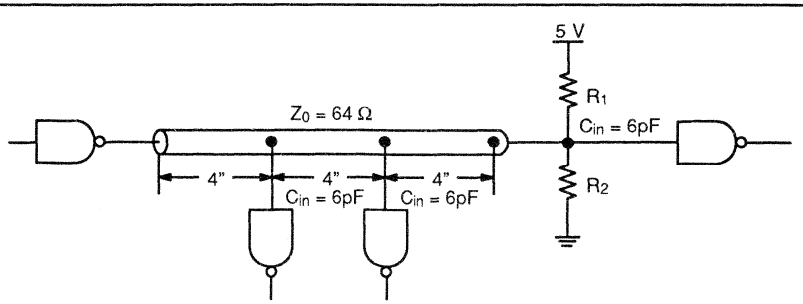

Figure 8. Distributed Loads with Parallel Termination

Serial Termination

A series resistor R_S is useful for dampening overshoot and ringing on longer lines. With serial termination, R_S plus the gate output impedance R_O should be equal to the line impedance Z_0. Since this technique is quite straightforward and applicable to all logic families, most interconnections with uncontrollable line impedance (lines in conjunction with connectors, a circuit board layout without a ground plane, wire-wrapped connections, or lines associated with back plane) use this scheme.

Serially-terminated lines display characteristic AC behavior as the signal switches. Figure 9a shows a simple circuit with a driving gate G_0 connected to gate G_1 with a fanout of 1, via a transmission line with line impedance Z_0. Presumably, as voltage V_A changes from HIGH to LOW at time t_1 (see figure 9b), V_B changes simultaneously, as follows:

$$\Delta V_B = \Delta V_A \frac{Z_0}{R_O + R_S + Z_0} \qquad (22)$$

Since R_S is chosen such that $R_O + R_S = Z_0$, equation (22) yields

$$\Delta V_B = 1/2 \Delta V_A , \qquad (23)$$

a 50% voltage drop.

After the signal has traveled the length of the transmission line, it is reflected back at the impedance discontinuity. In general, the input impedance of the load will be orders of magnitude greater than the line impedance. If we assume this, then from equation (15) we see that the reflection coefficient will be near unity; that is, the signal will be almost entirely reflected. Thus the indicent and reflected waves will combine to provide a low voltage at point C.

As the reflected wave travels back up the transmission line, it eventually brings point B LOW. Since $R_O = R_S$, there is no impedance mismatch at the source, and the reflection is absorbed. This is confirmed by equation (15), which shows that the reflection coefficient is 0 at the source.

The reverse process occurs when the signal changes from LOW to HIGH, as shown in figure 9b.

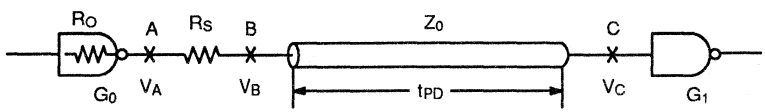

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Figure 9a. Example of Serial Termination

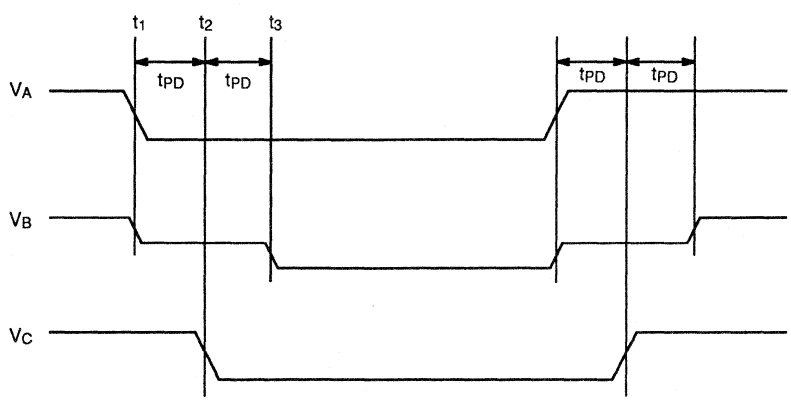

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Figure 9b. Voltage Waveforms of Serial Termination

Because of this behavior, loads cannot be distributed along the transmission line. They must all be lumped together at the end of the line. To compensate for the slower speed of the serial termination scheme with lumped loading at the end, one can add more transmission lines as shown in figure 10. Additional parallel transmission lines, with less fanout per line, provide more speed than a single transmission line with more fanout. However, the total fanout should never exceed the current-sinking capacity of the driving gate.

The value of R_S is

$$R_S = Z_0 - nR_O , \qquad (24)$$

where n is the number of parallel transmission lines. Note that this equation limits the number of parallel lines possible, since R_S will be negative if n is too large.

Comparison Between Parallel and Serial Termination Schemes

- Serial termination consumes less power than the single-power-supply parallel termination technique across the entire frequency spectrum. This is primarily because series termination does not add a DC load to the drivers.
- Parallel termination requires two resistors or one resistor with two power supplies. Serial termination requires one resistor per transmission line.
- With series termination, distributed loading cannot be used along the line because of the 50% voltage drop discussed above. With parallel termination, the waveform is undistorted along the entire transmission line, so that the loads can be distributed anywhere along the line as long as the terminating resistor values are adjusted. In either case, fanout is limited by the current-driving capability of the driving gate.
- If a long line is required or if power consumption is a concern, serial termination can be more advantageous. When speed is a main factor, parallel termination is better. Loading a long transmission line does not increase the t_{PD} of the driving gate nor its edge rate. However, it does increase the line capacitance, and consequently the line propagation delay. It has been proven[1] that delay time with loading increases twice as much with series termination as with parallel termination.

Board Layout Techniques for Transmission Lines

Once the type of transmission line is determined, board layout becomes critical. The following guidelines will help keep signals clean.

- Keep signal interconnections as short as possible to increase the t_R/τ ratio.
- Provide a separate signal plane; at least one ground plane and one power plane are recommended.
- Include a 0.1-µF decoupling capacitor as close as possible to the ground plane and the V_{CC} pin on each high-speed logic device.
- Provide both 0.1-µF ceramic high-frequency and 100-µF electrolytic low-frequency filtering capacitors on the power inputs to the board.
- Use wide line spacing between high-speed lines to avoid crosstalk.

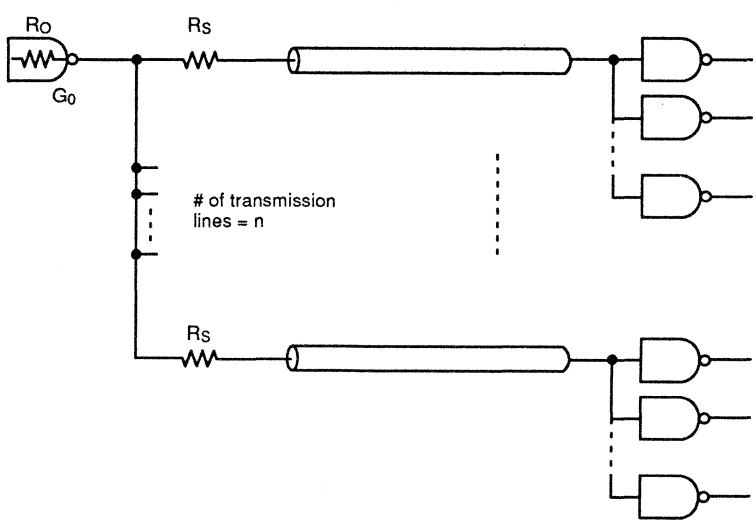

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Figure 10. Serial Termination with Multiple Transmission Lines

- Do not exceed maximum AC loading specifications, which include capacitive and current loading.
- Avoid anything that might cause an impedance mismatch on the line, such as sharp corners or discontinuities on the conducting plane.
- Such critical lines as edge-triggered signals or high-current driving signals should be separated from ordinary level-sensitive signals. In addition, sensitive circuitry, such as a clock oscillator, should have a separate ground to minimize noise interference.

CONCLUSION

As logic speed increases, edge rates becomes sharper; however, transmission line speeds remain the same if loading is not changed. Therefore, to avoid increased ringing, the maximum line length must shrink. As a result, if a line longer than the maximum permissible line length is required, proper termination must be provided. These careful design practices will ensure that your signals are clean, providing your system with better performance and reliability.

REFERENCES

(1) William R. Blood, Jr. "ECL Systems Design Handbook," Motorola Semiconductor Products Inc., Mesa, AZ, May, 1983 (fourth edition); Chapters 3 and 7.

(2) K. M. True, "Reflections: Computations and Waveforms," The Interface Handbook, Fairchild Corp., Mountain View, CA, 1975, Chapter 3.

(3) Ramo, Whinnery, and Van Duzer, "Fields and Waves in Communication Electronics," John Wiley & Sons, 1965, Chapter 1.

Ground Bounce

INTRODUCTION

The development of fast PAL® devices has increased the importance of analog considerations the digital designer has been able to overlook in the past. One of these is ground bounce. Ground bounce refers to the ringing on an output signal when one or more outputs on the same device are being switched from HIGH to LOW. This ringing can be in excess of 3 V. The system cannot consider the data valid until the ringing settles to below the V_{IL} of the receiving devices. The ringing in a fast device can last so long that a slower device with less ground bounce could actually be a faster solution.

The phenomenon of ground bounce is associated with the inductance and resistance of the ground connection in the integrated circuit. As there is always some inductance and resistance, ground bounce cannot be totally eliminated; however, it can be reduced to a level tolerable to the system.

This article will discuss the mechanism of ground bounce in CMOS circuitry and the utilization of slew-rate control used by AMD to keep ground bounce down to reasonable limits.

Mechanism

Figure 1 shows a schematic of an output driver and load including parasitic elements. The load capacitor is charged to the HIGH-level voltage. When the transistor turns on, the capacitor discharges into the transistor and lead impedance. The resultant RLC circuit will have a damped ringing (Figure 2). The peak amplitude depends on the edge rate of the switch and the RLC values, while the frequency of the ringing and the rate of decay depend only on the RLC values.

The ringing caused by a single output switching is normally below the LOW-threshold voltage. However, the voltage at the ground pad of the device is proportional to the number of outputs switching simultaneously. In addition, the voltage at the ground pad is coupled to any LOW output through its output transistor. Therefore, if enough outputs switch, ringing on the ground pad will be coupled to LOW outputs, causing the detection of false HIGHs.

Most PAL devices used today have relatively low output drive current: 16 mA or 24 mA. It is tempting to think that the low current level will somehow limit the switching en-

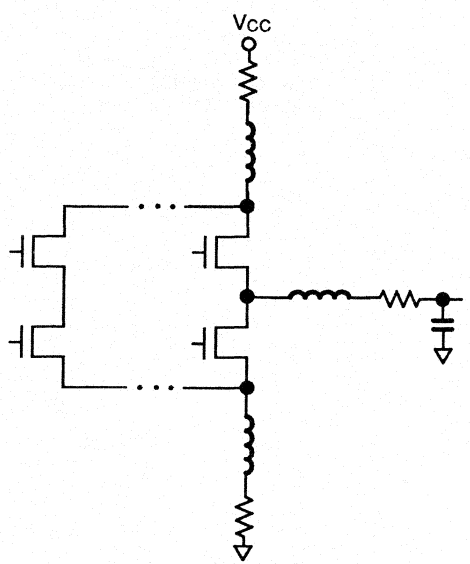


Figure 1. Simplified Schematic of an Output Driver

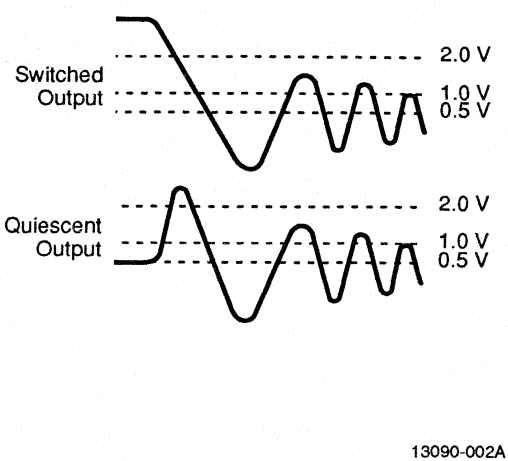


Figure 2. Ground Bounce

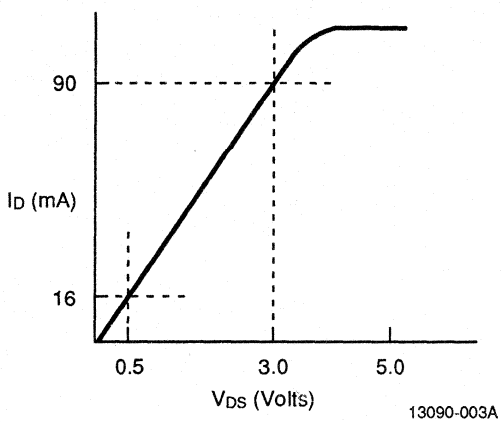
ergy and therefore ground bounce. Actually, even a low-power transistor can pass a relatively large current. The transistor I-V curve in Figure 3a shows that a MOS transistor designed for 16 mA at 0.5 V will pass 90 mA at 3.0 V. Figure 3b shows the V/I path when the output transistor switches between HIGH and LOW. Notice that the transistor switches from 3.5 V at 0 mA to 3.0 V at 90 mA. If eight outputs were to switch simultaneously, 90 mA X 8, or 720 mA, would flow through the ground lead.

This sudden current surge is actually self-limiting. As the ground-pad voltage rises due to the high current change, the internal V_{DS} and the available gate bias voltage are reduced, lowering the drive current. However, the ringing can still exceed 3 V.

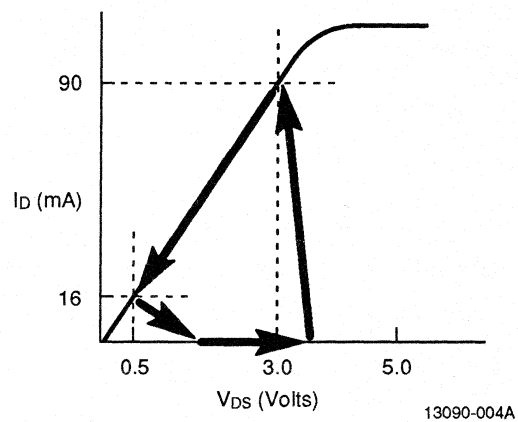
Controlled Edge Rate

The parameters that influence ground bounce are the inductances and resistances of the device, the capacitance of the load, and the edge rate. Of these, the only one that the chip manufacturer can directly control is the edge rate.

Turning on the output-driver transistor is equivalent to switching the charged load capacitor to ground. This can be represented by a step-voltage source in series with the capacitor (Figure 4a). Slowing down the rate that the output transistor can turn on changes the voltage source from a step to a ramp (Figure 4b). With a

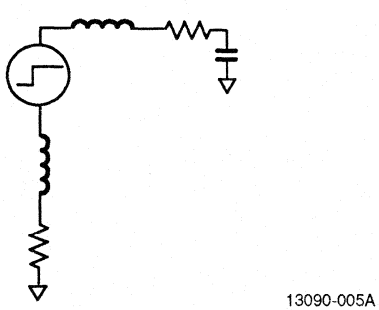


3a. The DC Curve of an Output Driver Transistor

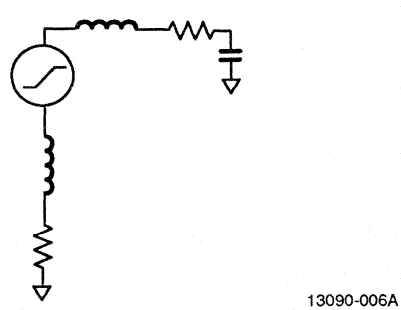


3b. The Path Followed as the Transistor Switches between the HIGH and LOW Levels

Figure 3.



4a. Equivalent Circuit of an Output Driver Transistor with a Capacitive Load



4b. Output Driver Circuit with Slew-Rate Limiting

Figure 4.

shallower slope, less energy is available for ringing and the ground-bounce amplitude is reduced.

A Spice simulation (Figure 5) illustrates the effect. The device without risetime control will have a very high charging current with a large di/dt: 2.1 X 10^7 A/s. Risetime control reduces the di/dt about 25%. This will result in a corresponding reduction in the voltage that can develop across the ground inductance.

AMD has a proprietary technique that slows the edge rate of the output transistor, thereby reducing the amplitude of the ringing. Slowing down the fall time will add about a nanosecond to the output delay, but the system speed will still be greatly increased. On a high-capacitance load, a non-edge-rate-controlled device could ring for more than 25 ns. The additional delay required to allow for the ringing would be intolerable.

System Ground Bounce Solutions

There are some things that the system designer can do to reduce the ground bounce to a tolerable level.

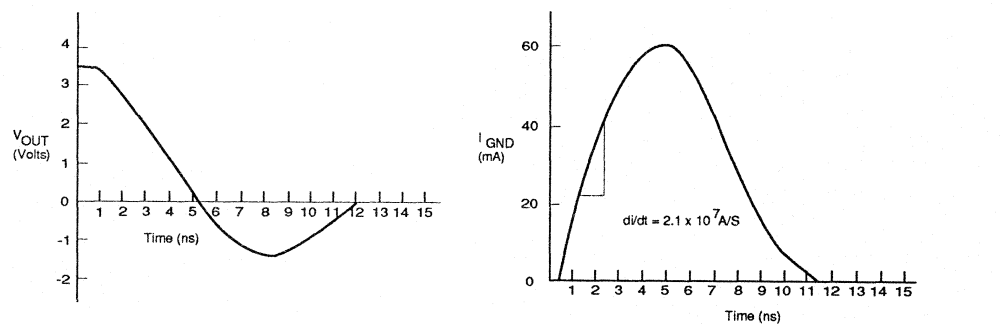
1) Use AMD PAL devices that incorporate edge rate control. This the first line of defense against ground-bounce-related problems, and the most effective.

2) Use shorter lead packages. The bonding wires in a PLCC are 1/4 the length of the ground bonding wire in a DIP. The inductance is reduced proportionally. Any reduction in inductance will reduce the amplitude of the ringing.

Some devices have center power and ground pins. The ground pin will be substantially shorter and have a proportionately reduced inductance. This will reduce the coupling between outputs. A good example is the PALCE26V12.

3) Reduce capacitive loading. Capacitive loading in any system should be reduced as much as possible. This may involve consideration of the transmission line characteristics of the layout.

4) Limit the number of outputs switching simultaneously. If the load naturally has high-capacitance such as a bus or memory board would, ground bounce can be reduced by limiting the number of outputs that can switch simultaneously in a single device. Many system designers consider 4 to be an acceptable upper limit.



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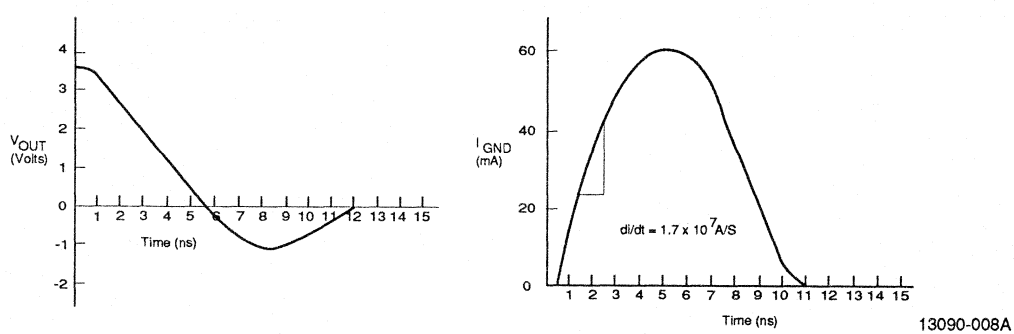
5a. Without Risetime Control



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5b. With Risetime Control

Figure 5. Effect of Risetime Control

Metastability

INTRODUCTION

A significant number of digital systems must deal with inputs not synchronized to their own internal clocks. These asynchronous signals can arise from any of the various asynchronous protocols, such as are often used in bus designs; they can be the result of trying to share signals from systems with different clocks; or they may be the response of a system user, who is of course not synchronized with the system. The result can be metastability, a problem which can plague unwary designers. It is not a newly discovered phenomenon, but is normally dealt with somewhat qualitatively, and, unfortunately, is usually ignored as much as possible.

Causes of Metastability

The flip-flop setup time is the parameter that is most often at the root of metastability. The setup time is basically a requirement that data be made available at the input to the flip-flop before the clock signal arrives. The data must not only be there, but must also be stable.

In a PAL® device, the use of an array for the data adds to the setup time. The data passes through the array on its way to the flip-flop (Figure 1). The clock signal, on the other hand, goes directly from the clock pin to the flip-flop. Its path is much shorter than the data path. The setup time is therefore essentially a requirement that the data signal must be given more time to get to the flip-flop before the clock signal.

If the published setup time is satisfied, the data arrives at the flip-flop well before the clock, and the output to the flip-flop will change as desired (Figure 2). If the setup time is violated, then no guarantee can be made about what the output will do. The output may be normal, since the published setup time is a worst-case number. However, if the timing between the clock and data is just right, the output will be unstable for some time before it settles into some state. Neither the time the output remains unstable nor the final state is predictable (Figure 3). This condition is metastability.

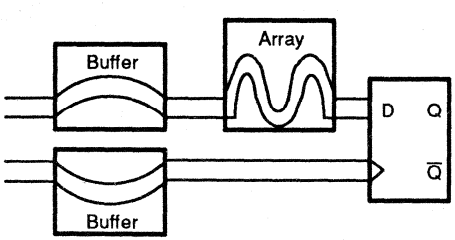

Figure 1. The clock and data paths in a PAL device

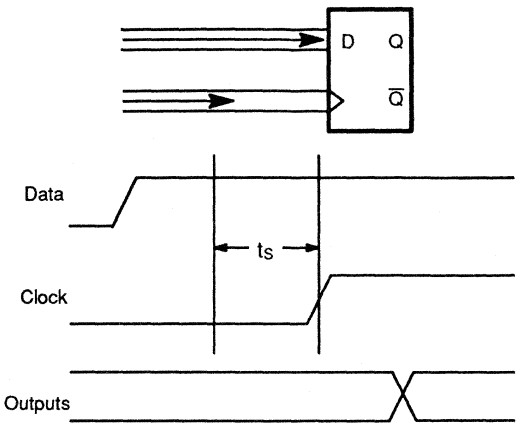

Figure 2. Output response when the setup time is satisfied

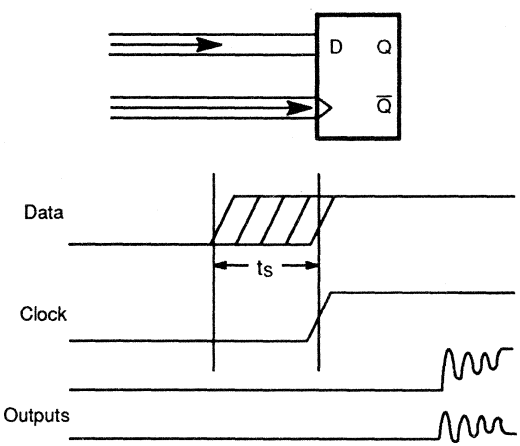

Figure 3. Possible output response when the setup time is violated

Ways of Dealing with Metastability

The most common way of dealing with this problem is to synchronize the inputs with an extra flip-flop (Figure 4). If the first flip-flop goes metastable, hopefully the delay between clock pulses will allow the ringing to die down

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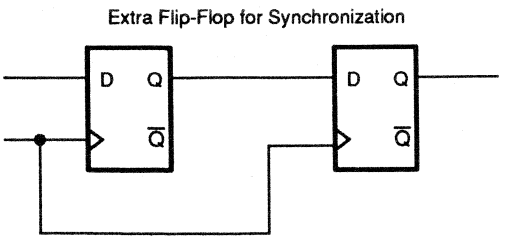

Figure 4. Dual synchronizer

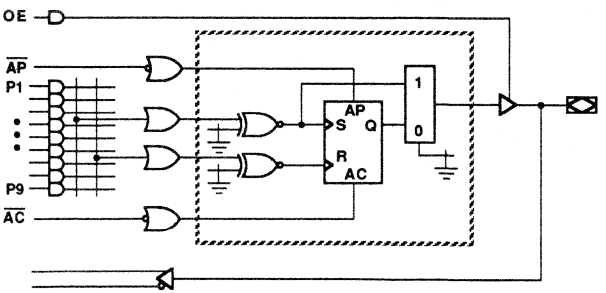

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Figure 5. Edge-triggered S-R macrocell

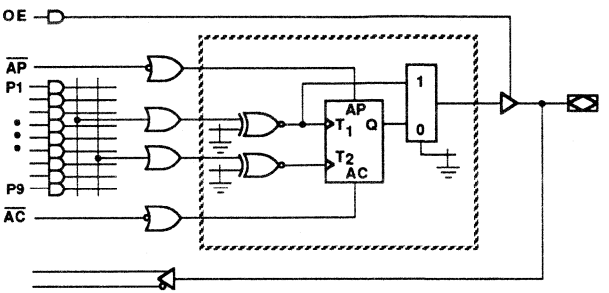

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Figure 6. Edge-triggered 2-T macrocell

before clocking into the next flip-flop. This improves the chances of having good data in the second flip-flop.

This method is not without its costs. Each extra stage of flip-flop means an extra clock delay of the data which must be absorbed by the system. Moreover it is not foolproof. The possibility of metastability is reduced, but not eliminated. A flip-flop can go metastable if the preceding stage does not recover quickly enough.

The best way to avoid metastability is to avoid synchronization when possible. Many applications, such as bus arbitration schemes, use synchronization not because synchronization itself is necessary, but because until now it has provided the only convenient way to store data. This unfortunately takes a system that is inherently asynchronous and adds some synchronizing elements in the middle. If some way could be found to eliminate the synchronizing clock, the setup time would be eliminated, taking with it the major cause of metastability.

The PAL22IP6

To help designers avoid unnecessary synchronization, AMD has developed the Interface Protocol Asynchronous Cell™ (IPAC) PAL device: the PAL22IP6. The key to the IPAC device lies in the edge-triggered S-R and 2-T flip-flop macrocells. With the S-R flip-flop (Figure 5), the output goes true on the rising edge of the S input and false on the rising edge of the of the R input. With the 2-T flip-flop (Figure 6), the output toggles on the rising edge of either T input; the T inputs are completely independent. For both flip-flop types, the major implication is that the need for a clock has been eliminated — since the output is triggered by the rising edge of the data, the data itself has become the clock. Therefore this device has no setup time.

The benefits of the IPAC device can be demonstrated by a simple interface design. A microprocessor generates a chip select signal (CSL) which is converted to a peripheral request (REQL). REQL is removed when the peripheral responds with a grant signal (GRANTL). The conventional approach is to register REQL. The device could go metastable either because of CSL or GRANTL, since both are asynchronous (Figure 7).

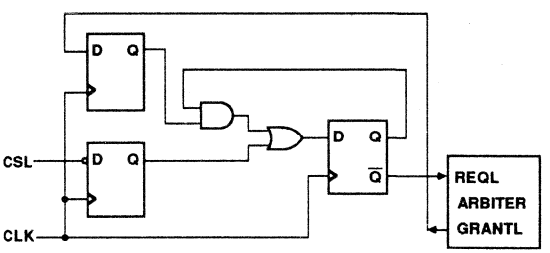

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Figure 7. Interface design: conventional solution

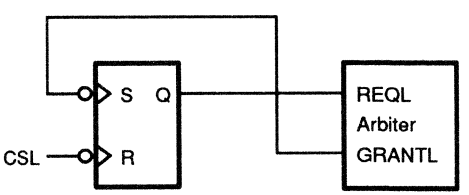

Figure 8. Interface design: the IPAC device solution

With the IPAC device, REQL is generated at the falling edge of CSL and removed at the falling edge of GRANTL. This is done using only one S-R flip-flop. Because S and R are in essence their own clock inputs, there is no possibility of metastability (Figure 8). In addition, since no intervening synchronizing stage is needed, a clock cycle delay has been eliminated.

Summary

Metastability can occur in a number of different kinds of asynchronous systems, usually due to the inability to guarantee that the setup time of the flip-flops will be satisfied. In standard synchronous systems, where the setup time (along with all other timing requirements) is specifically designed in, metastability will never be a problem.

In some situations, metastability is caused by the need to interface systems with different clocks. In this case, it will never be possible to completely eliminate the possibility of metastability. Instead, the designer must take steps to reduce the probability of a system failure due to metastability.

In other systems, however, signal storage is necessary, but synchronization is not. In this kind of design, the cause of metastability can be eliminated by using the PAL22IP6, which provides edge-triggered S-R and 2-T flip-flops. Because these flip-flops have no separate clocks, there is no setup time, and the major source of metastability has been eliminated.

Latchup Circuit

Latchup is caused by an SCR (Silicon Controlled Rectifier) circuit. Fabrication of CMOS integrated circuits with bulk silicon processing creates a parasitic SCR structure. The behavior of this SCR is similar in principle to a true SCR. These structures result from the multiple diffusions needed for the formation of complementary MOS transistors in CMOS processing. The SCR structure consists of a four layer device formed by diffused PNPN regions. These four layers create parasitic bipolar transistors illustrated in Figure 1.

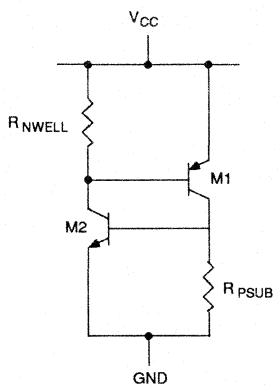

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Figure 1

Figure 2a shows a typical CMOS inverter layout with the schematic of the parasitic bipolar SCR structure. Figure 2b is a cross sectional representation of the CMOS inverter, again with the schematic of the bipolar SCR structure.

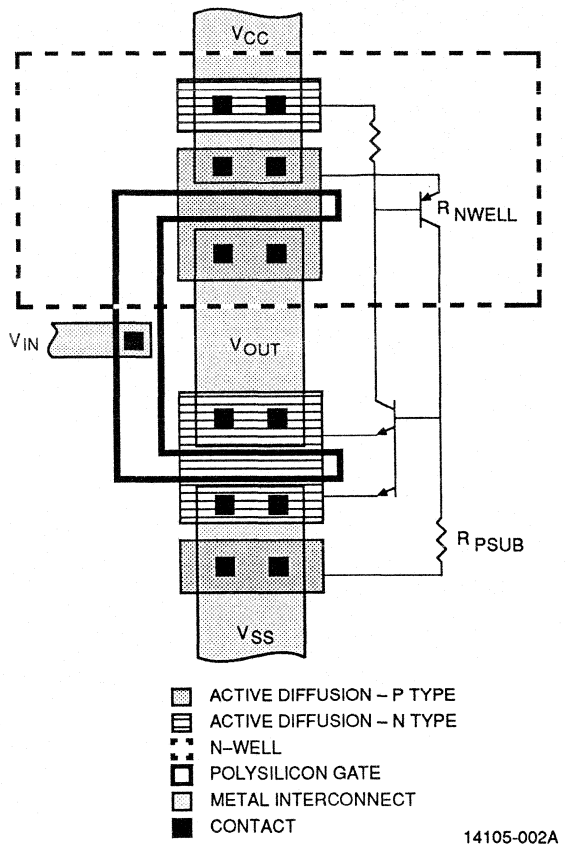

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Figure 2a

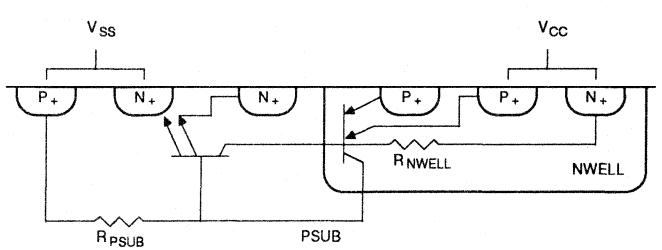

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Figure 2b

Any CMOS diffusion can become part of the parasitic SCR structure, since all of these parts are interconnected through the bulk silicon substrate resistance. Other parasitic resistors shown result from doped regions of the semiconductor. The magnitude to which the resistors resist current flow depends upon geometric size and doping level.

As illustrated in Figure 1, the complementary PNP and NPN transistors are cross-coupled, having common base-collector regions. The vertical PNP device, M1, has its base composed of the N-well diffusion while the emitter and collector are formed from P-type source-drain and substrate regions, respectively. The lateral bipolar transistor, M2, base is the P substrate with emitter and collector junctions formed from N-type source-drain and N-well diffusions, respectively.

Latchup Conditions

Under normal bias conditions the SCR conducts only leakage current and the SCR structure is in the blocking state. However, as current flows across any of the parasitic resistors, a voltage drop is developed, turning on the parasitic bipolar base-emitter junction. The forward bias condition of this junction allows collector current to flow in the bipolar transistor. This collector current flows across the base-emitter resistor of the complementary bipolar transistor, creating a voltage sufficient to turn on the transistor.

A regenerative loop is now created between the complementary bipolar transistors such that current conduction becomes self-sustaining. Even after removal of the stimulus that triggered this action, the current conduction can continue. This region of operation is a high-current, low-resistance condition characteristic of a four layer PNPN structure. This is referred to as latchup. Once initiated, the excessive latchup current can permanently damage an integrated circuit by fusing metal lines or destroying junctions.

Causes Of Latchup

Latchup may be initiated in numerous ways. Just the critical causes frequently encountered in a system environment will be discussed. These include power up, supply overvoltage, and overshoot/undershoot at device pins.

Power-Up

Caution must be exercised when powering up CMOS ICs to avoid driving device pins before the supply voltage has been applied to the circuit. Placing a device or board in a "hot socket" will create this situation. When subjected to hot socket insertion, voltage conditions at the device pins are uncertain such that the input diodes may be forward biased. Forward biasing the input diodes with a delayed or uncontrolled application of V_{CC} could cause the device to latch up. Advanced Micro Devices' CMOS circuits have substantial immunity to hot-socket power up, but since this condition is uncertain, and difficult to characterize, test, and guarantee, it should be avoided.

Supply Overvoltage

Supply levels exceeding the absolute maximum rating can cause a CMOS circuit to latch up. Elevated supply voltage may cause internal junctions to break down, producing substrate current capable of triggering latchup. Latchup is just one of the reasons overvoltage should be avoided; other undesirable effects may result from this.

Overshoot/Undershoot

Generally the I/O pins experience the noisiest electrical environment. Fast switching signals with a large capacitive load may overshoot, creating a transient forward bias condition at the I/O junction. These junction diodes are illustrated in Figures 3 and 4. Typically this is where latchup is most likely to be induced. Proper design of the input and output buffers is essential to minimize the risk of latchup due to overshoot.

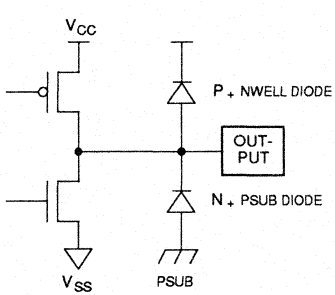

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Figure 3

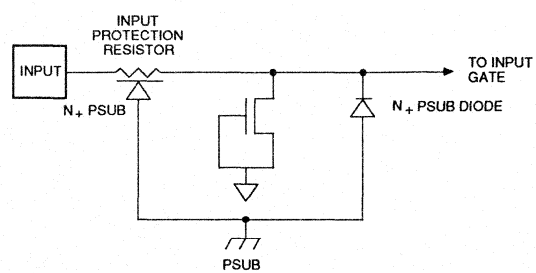

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Figure 4

Testing For Latchup

Advanced Micro Devices characterizes the latchup sensitivity of its devices before they are released to the market. Testing is done in such a way as to completely cover every possible latchup condition, including V_{CC} overvoltage, pin overcurrent, and pin overvoltage.

V_{CC} Overvoltage Test

The V_{CC} overvoltage test is applied to all power (V_{CC}) pins. The test is performed at the highest guaranteed operating temperature of the device. All inputs and I/Os acting as inputs are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open).

V_{CC} max is applied to the V_{CC} pin. A positive high voltage pulse is then applied to the V_{CC} pin and returned to V_{CC} max. The occurence of latchup is detected if the voltage across the device is less than V_{CC} max, and the current through the device is greater than the normal DC operating current.

Pin Overcurrent Test

The pin overcurrent test is performed on every output, I/O pin, and non-current-limited input pin. Non-current-limited inputs are inputs which present a diode-like (or otherwise "infinite") current characteristic for input voltages in the range (GND – 5 V) < Vin < (V_{CC} + 5 V).

The pin overcurrent test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs should be floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. A three-state output under test should be disabled. A non-three-state output type under test should be a logic High when applying a positive current and a logic Low when applying a negative current. An I/O pin should be placed into the input mode.

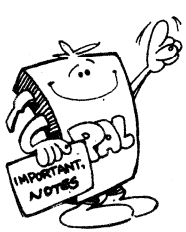
A high current pulse is then applied to the pin under test. The magnitude of the pulse is stepped until latchup is induced. Both positive and negative currents are tested. Latchup is observed as described previously. The sensitivity of the device is the worst case sensitivity found on any pin of the device.

Pin Overvoltage Test

The pin overvoltage test is performed on current-limited inputs. Current-limited inputs are inputs which present a resistor-like (or otherwise "limited") current characteristic for input voltages in the range (GND – 5 V) < Vin < (V_{CC} + 5 V).

The pin overvoltage test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. Both positive and negative voltage pulses are applied to the pin under test. Latchup is observed as described previously. The sensitivity of the device is the worst-case sensitivity found on any pin of the device.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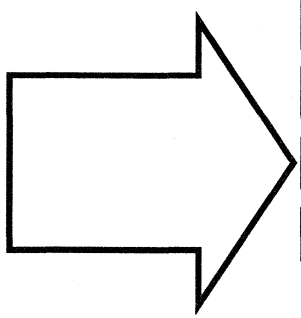

Quality and Reliability

IMOX™ PRODUCT TECHNOLOGY AND RELIABILITY

In order to meet the next generation requirements for speed and density in PAL devices, an advanced bipolar technology has been developed called IMOX-III. Although IMOX-III represents a major breakthrough which will allow further scaling to the sub-micron region, the technology also shares many features in common with prior generations of technology, IMOX-II and IMOX-IIS.

The revolutionary breakthrough of IMOX-III is the use of reactive-ion-etched grooves, called slots, to isolate the transistors. These slots are 1.5 microns wide, over 6 microns deep, and are filled with dielectric material (Figure 1). Because the transistors are not isolated by junctions, space for depletion spreading is not necessary. Also, since the slots are etched anisotropically, thicker EPI layers can be isolated without increasing the isolation widths. Essentially, no density penalty is paid to achieve high breakdown voltages. Higher breakdown voltages are needed to support the programming voltages required to program fuses in bipolar PAL devices.

Smaller device sizes translate into faster circuits through smaller die sizes and reduced capacitances of active devices and metal interconnect. Another advantage of the slot isolation is reduced collector to substrate capacitance, which offers improved performance in many circuit configurations.

Overall, the IMOX-III process is a major step forward from IMOX-IIS. In addition to the slot isolation, stepper lithography and dry metal and via etching have been implemented, resulting in a dramatic reduction in device sizes. The slot isolation allows the silicon pitch to be reduced by one-third. The steppers and plasma metal etching allow the metal pitch to be shrunk by one-third also. Furthermore, the IMOX-III process was designed with a 20% shrink in mind. This scaling can be accomplished simply by shrinking the masks.

The IMOX-III process shares many familiar features with its predecessor, IMOX-IIS. Oxide-walled bases and emitters are used to reduce the size and parasitic capacitances of transistors. Ion implanted emitters and bases are used to achieve the profile control necessary for high performance transistors. The reliability of the transistor structure used in IMOX-III has been proven over millions of hours of high-temperature tests on products that use IMOX-II and IMOX-IIS processes.

Another key feature familiar to users of older generation IMOX PAL devices is the fuse technology. IMOX-III uses platinum silicide fuses, identical to the fuse technology used on older generation IMOX PAL devices. Programming yields are the highest possible, and programming times are extremely short (about 300 ns).

The IMOX-III technology also features two levels of metallization, as does IMOX-II and IMOX-IIS. However, with IMOX-III technology, both layers are stepper-defined and plasma-etched.

IMOX-III technology will enable third and fourth generations of PAL devices that will be significantly faster and more complex than the current devices. It will also reduce the cost of the new

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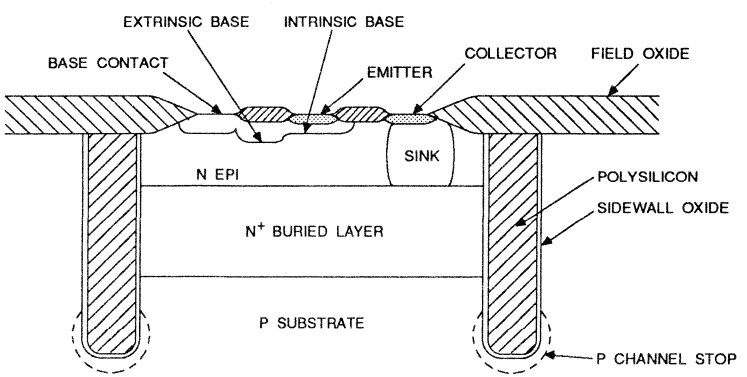

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Figure 1. Slot Isolation

devices by significantly reducing die sizes or allowing more features to be added without increasing present die sizes. Faster and more complex PAL devices will permit system designers to build advanced computers, communications systems and instrumentation systems at a much lower cost.

IMOX Product Reliability

IMOX bipolar Programmable Array Logic (PAL) devices are based on two key technologies with many years of high volume production experience behind them.

1. IMOX—The basic process technology employed is IMOX, an advanced ion-implanted, oxide-isolated structure. IMOX provides very high performance devices with predictable manufacturing yields. It has accumulated many millions of hours of life test history through its application to the Am27S series of PROMs and the Am2900 family of bipolar microprocessors.

2. Platinum-silicide fuses—This fuse structure was originally developed for use on junction-isolated PROMs. It quickly established a standard of excellence for high programming yields and long-term reliability. Several years ago it was applied to a new generation of ultra high performance PROMs based on the IMOX process.

This combination of IMOX and platinum-silicide fuses has an outstanding record of reliability which has been verified repeatedly through in-house life testing and by high-reliability customer qualification testing and system use.

IMOX PAL devices are fabricated with this same combined process technology. Not only is the technology for building PAL devices and PROMs the same, but also the programming algorithm and programming circuitry used to program the platinum-silicide fuses are the same in all characteristics of importance. The result is that the conditions seen by an IMOX PAL device fuse are the same as those seen by an IMOX PROM fuse.

Due to the common process technology, fuse design and fuse programming circuitry design, reliability and programming yield results are expected to be the same for PAL devices and PROMs. Data accumulated to date on PAL devices confirms this expectation.

This report describes the characteristics of the platinum-silicide fuse and programming conditions for the fuse, along with a description of the ongoing reliability monitor program.

Platinum-Silicide Fuse

Fusing Technique

IMOX PAL circuits are designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to program the platinum silicide links quickly and reliably.

The sequence of events to program a fuse are:

1. V_{CC} power is applied to the chip.

2. The address of the fuse to be programmed is selected by TTL levels on the appropriate address pins.

3. The outputs are disabled. (Pin 1 serves this purpose on PAL devices).

4. The programming voltage is then applied to one output.

5. A fuse enable is accomplished by raising an input to a level above normal TTL operating voltage. (Pin 11 is used for this on PAL devices.) This action gates the current flow through the proper fuse, resulting in an open fuse in a few microseconds.

6. The output programming voltage is lowered and then removed.

7. The device is enabled and clocked if required. The output state then indicates whether successful programming has occurred. If programming has not occurred a sequence of much longer pulses is applied until programming occurs.

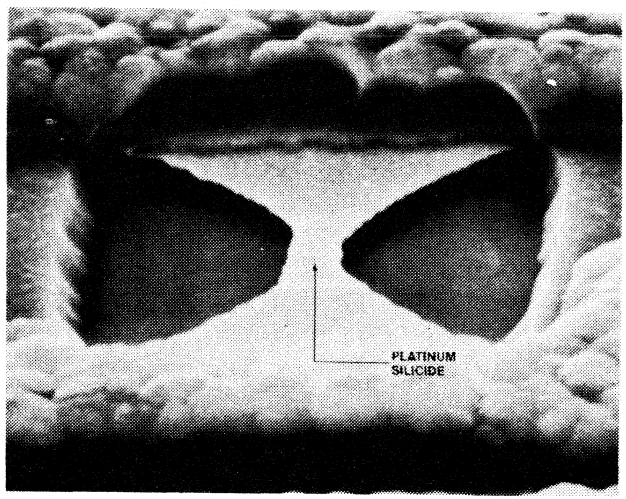
8. The sequence of 2 through 7 is repeated for each bit that must be programmed.

There are several advantages to this technique. First, the two high current power sources, VCC and the voltage applied to the output, do not have critical timing requirements. As the programming current is gated through the fuse actively, there is no dependence on the rise rate of the programming voltage. A fast application of programming current is desirable for optimum programming. Since the output programming voltage does not have to be applied rapidly, breakdown and latchback problems attributed to fast voltage rise times on the output are avoided.

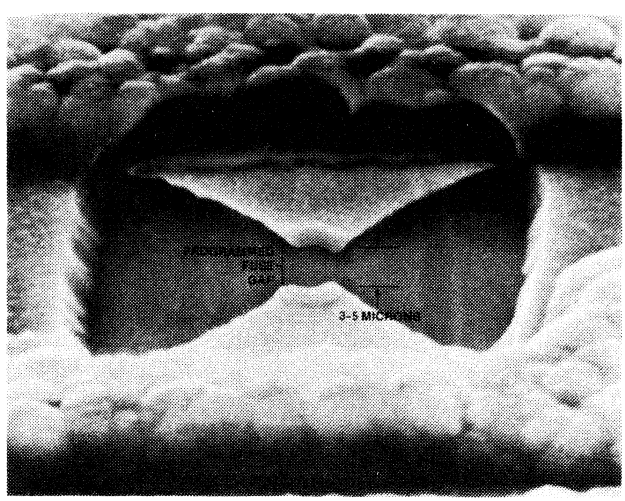
This programming procedure has a second major advantage. If the fuse does not open during the first programming pulse, longer programming pulses are used. With the platinum-silicide fuse, long programming pulses may be safely applied with no danger of developing a reliability problem. The algorithm can therefore be designed to minimize the time required to program by using a fast first pulse followed by a longer pulse if needed to program the occasional fuse that does not open with the first short pulse. Most devices do program satisfactorily with all short pulses.

Fuse Characteristics

When a fast (less than 500 ns rise time) current pulse is applied to a fuse, the fuse voltage rises abruptly to a value determined by the room temperature resistance. However, it then quickly falls to a value of approximately 2 V. This value is nearly independent of the applied current. During the period of time the fuse is molten, the fuse current drops very abruptly to zero indicating the separation of the platinum-silicide into two distinct sections. Scanning Electron Microscope photographs of the resulting fuses (Figure 2) indicate that the typical case is a sharp clean separation in excess of a micron. This separation occurs in the center of the fuse because the "bow-tie" structure (Figure 3) concentrates the energy density in the center away from the aluminum interconnect lines. The energy density in the center of the fuse creates temperatures substantially greater than those required to melt the silicide. Melted material is then "wicked" from the center of the fuse to either side due to surface tension.



Unprogrammed Fuse



Programmed Fuse

Figure 2. Scanning Electron Microscope Photo–Unprogrammed and Programmed Fuses

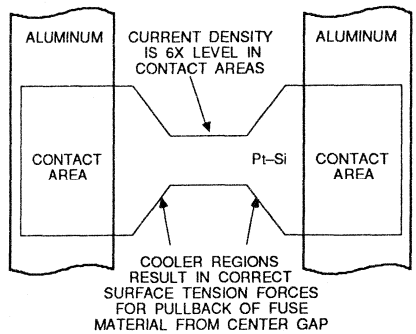


Figure 3. Bow–Tie Fuse Design

Reliability Testing Data

Data on the reliability of PAL and PROM devices with platinum-silicide fuses is gathered via the Reliability Monitor Program (RMP). The RMP is an ongoing program conducted on all device types across all product lines, and is designed to ensure that all IMOX devices meet acceptable reliability levels. A summary of the RMP tests for hermetic and plastic molded packages are shown in Tables 1 and 2.

Data on IMOX PAL and PROM devices has been gathered over millions of device hours and more than 40 billion fuse hours of high temperature operating life tests (HTOL). The life test circuits used in this work conform to MIL-STD-883 method 1005 conditions C and D. This data indicates a projected unit failure rate (at 60% confidence) of 0.0002%/1000 hrs. at 70°C.

Results of the IMOX RMP are updated periodically and can be obtained through inquiry to any of the Sales Offices listed in the back of this handbook.

TEST	CONDITIONS	TYPICAL SAMPLE SIZE
Infant Mortality	160 hours at 125°C ambient. Initial and end-point electrical tests.	300
Operating Life	1000 hrs (1160 total) at 125°C ambient. Initial and end-point electrical tests.	120
Temperature Cycle	1000 cycles, (–65°C to 150°C), 30 min/cycle. End-point-hermeticity and electrical tests.	50*
150°C Operating Cycle	1000 hours at 150°C ambient. Initial and end-point electrical tests.	50

* These units are hermetically tested prior to commencement of test.

Table 1. Reliability Monitor Program for Devices in Hermetic Packages

TEST	CONDITIONS	TYPICAL SAMPLE SIZE
Infant Mortality	160 hours at 125°C or 85°C ambient (Tj <150°C nominal). Initial and end-point electrical tests.	300
Operating Life	1000 hrs (1160 total) @ 125°C or 85°C ambient (Tj <150°C, nominal). Initial & end-point electrical tests.	120
Temperature And Humidity	85°C/85% RH/low power bias, 500 hours and 1000 hrs. Initial, interim, and end-point electrical tests.	50
Temperature Cycle	1000 cycles: –65°C to 150°C, 30 minutes/ cycle. High temperature (75°C min) functional end-point electrical test.	50
Pressure Cooker	121°C, 15 psi, 160 hours, unbiased, initial end-point electrical test.	50

Table 2. Reliability Monitor Program for Devices in Molded Packages

MONOX 3™ OXIDE-ISOLATED PROCESS

The MONOX 3 process is an evolution of the junction-isolated process used in the popular 15 nanosecond PAL family. The 15 ns PAL device process is a shallow-junction, ion-implanted, diffused isolation technology.

When the time came to advance PAL device speed through improved process technology, the decision was made to evolve from and benefit from the proven reliability, simplicity, and manufacturability of the 15 ns PAL device process. Only fully recessed oxide isolation and stepper design rules were to be added for the new technology. The fully recessed oxide isolation technology to be used had already been proven in earlier processes.

MONOX 3 Process Description

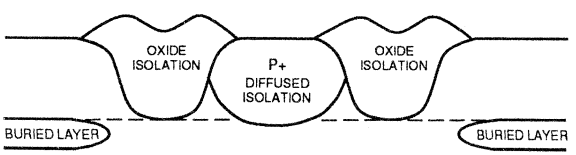
The unique feature of MONOX 3 is the isolation structure (patent pending) which combines the best features of fully recessed oxide isolation (FULROX) and diffused isolation, while maintaining a very dense structure. The advantages of FULROX, low capacitance and high density, are well known to the industry.

Diffused isolation has an important advantage for transistors that are driven hard into saturation, as in the case where minimum size array transistors are used to program fuses in PAL devices. In this case, substantial current is injected into the substrate, and this may adversely affect nearby circuitry. While this substrate injection can be reduced in FULROX, it has an adverse effect on capacitance and perhaps density.

In MONOX 3, the diffused portion of the isolation acts as an excellent substrate contact and as a sink for the injected substrate current. This permits the FULROX to be optimized both for density and for low capacitance, lower than is typical for industry-standard oxide isolation. The typical density disadvantages of diffused isolation are minimized by containing the diffusion within the FULROX. This isolation structure results in a die that is substantially smaller than some trench-isolated products, and that has lower capacitance than other oxide-isolated products.

Other features of the MONOX 3 process are:

- Fully ion implanted except for buried layer—This permits excellent control of the layers for a consistent product, and permits a base width of 2000Å which yields a cutoff frequency f_t of 4.3 gigaHertz.
- High-pressure oxidation—This is used for the recessed isolation to minimize process temperature and crystal defects.
- Oxide walling all devices—This eliminates potential leakage paths that might cause reliability problems.
- Planarization of the isolation "bird's head" shape—This improves lithography and metal step coverage.
- N+ and P+ sink diffusions—These lower parasitic resistances.
- Dry (plasma) etch—This improves control and density of most layers including metal.
- Platinum silicide Schottky diodes—These prevent saturation of the logic transistors for improved speed.
- Titanium Tungsten fuses—These are simple and reliable.
- Double layer metal, with intermetal planarization—The first metal pitch is 4.5 microns and the second layer metal pitch is 6.0 microns.
- Stepper lithography with 1.5 micron minimum design rules (1.3 micron fuses)—This not only makes the die more compact, but significantly improves the fuse programming (see next section).



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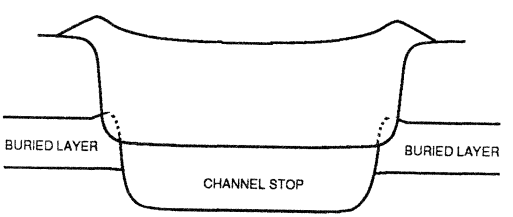
MONOX 3 Isolation



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Typical Oxide Isolation

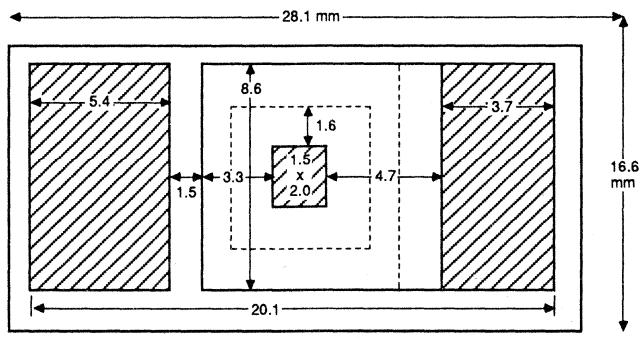
MONOX 3 Fuse Technology

The fuse technology in MONOX 3 is Titanium Tungsten (TiW). This fuse technology has been used for years in millions of chips that have proven to be the industry's most reliable programmable logic parts.

In MONOX 3 the fuses are further enhanced by using stepper lithography to print them 1.3 microns wide. This significantly lowers the programming current from 70 milliamps to 35 milliamps maximum. A lower programming current means less power and heat are needed, leading to increased reliability and a denser chip design.

MONOX 3 Summary

In conclusion, MONOX 3 was designed to be and is both high-performance and simple. Only thirteen masking layers, two diffusion cycles, and four oxidation cycles are used. This yields a process that competes with, and out-performs, other currently available programmable logic technologies. The relatively few steps needed to manufacture MONOX 3 devices mean fewer potential problems and increased reliability.



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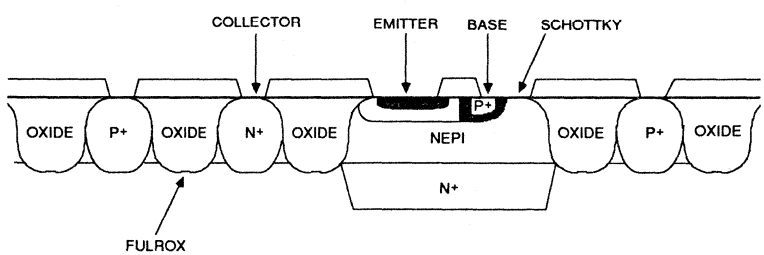
MONOX 3



14106-006A

NPN Transistor

PRODUCT TESTABILITY

Thorough testing of programmable logic devices by the manufacturer is important to both the performance of programmable logic and its cost of use.

Field programmable logic devices are different from other semiconductor products in that the user must complete the manufacturing process by programming and functionally testing the parts.

Programming is normally accomplished on commercially available programming equipment. Functional testing may be performed on a programmer, on automatic test equipment or at the board or system level. Figure 4 illustrates where device failure detection can occur. Clearly, the cost implications of failure become more serious with each advancing step.

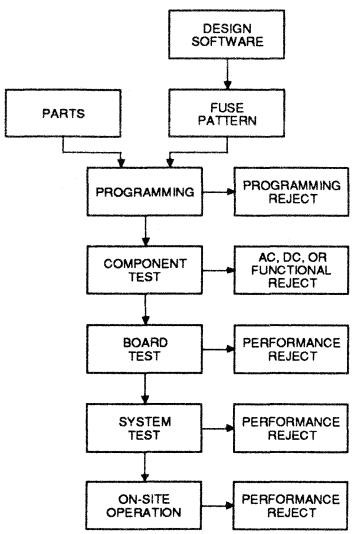


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Figure 4.

As a result of assuming the responsibility of programming and test, the user gains all the benefits of a custom function with the cost and availability advantages of a standard product. However, the user must also deal with those parts that do not program successfully or do not function to advertised specifications after programming.

Testing before shipping can make a difference to the user in:

1. Programming yield
2. Post-programming functional yield (PPFY)
3. Uniformity of performance

This paper describes the techniques used on IMOX process PAL devices to allow testing of these three important attributes on every device before shipment to the user.

Programming Yield

Programming yield is the measure of the success of the programming operation. Large volume users of programmable logic keep records of the programming yield history of their suppliers' parts. Programming yield is considered by these users to be an important element in judging the overall suitability of different suppliers' parts.

Post-Programming Functional Yield

Experienced PROM and EPROM users are sometimes puzzled by the fact that not all programmable logic devices function correctly even though they have successfully completed a programming operation and fuse verification check.

With PROMs, a one-for-one relationship exists between address states and programming elements (which can be fuses, floating gate MOS devices, open-base NPN transistors, etc.) That is, the state of each output for each address is dependent on the condition of only one fuse. Sensing a desired fuse state after programming therefore practically guarantees correct functional operation (at least at the voltage and temperature conditions of the programming operation).

With programmable logic devices the relationship between programming success and post-programming functionality is not one-for-one. Except for the simplest of patterns and devices, the relationship is highly complex. Feedback buffers allow the creation of more than one level of logic; latches, counters, shift registers, and even oscillators can be created. Special fuse functions such as polarity control, output enables, register/combinatorial path selection and buried registers complicate the relationship further.

This is the power of programmable logic—but the testing challenge that results from this versatility can be substantial. Logic states for programmable logic devices can depend on multiple fuses. The fuse verification procedure that examines each fuse uniquely is therefore not sufficient, as it is with PROMs, for guaranteeing functionality.

All programmable logic devices contain special on-chip programming circuitry and modes to allow programming and verification of each individual fuse. The complexity of programming may vary significantly, but all have one thing in common—successful programming by itself cannot guarantee functionality.

The user's job does not end then with the programming operation. To be assured of a functional part, a comprehensive set of test vectors must be applied to the part. Many device programmers accept test vectors along with fuse programming vectors and will apply the test vectors to the part following the programming operation. The PRELOAD feature greatly simplifies the test generation problem for registered parts.

Uniformity of Performance

The buyer of a programmable logic part has the right to expect that the performance specifications appearing on the manufacturer's data sheet will be met for all legitimate applications of the part. This applies to each and every logic path and function.

A glance at the logic diagram for an unprogrammed part shows that, with the array in its unprogrammed state, no amount of activity of the inputs can make any output switch. Without any programmed fuses, the AND gates see both the true and complement of all inputs.

If post-programming performance is to be guaranteed with absolute confidence, test circuitry must be provided to allow each path to be tested to data sheet performance.

Approach to Designing in Testability in PAL Devices

The approach to the design of programmable logic was strongly influenced by the goal to provide users with the best programming yield, post-programming functional yield, and uniformity of performance.

Designing programmable logic can be viewed as a three-dimensional task involving high-performance logic design, fuse programming circuit design and test circuit design.

The first dimension is the design of a high-performance logic circuit with SSI/MSI competitive switching speeds and very high output drive for bus environments.

The second dimension of programmable logic design is the programming circuit design. The emphasis of this design is to provide circuitry that will deliver large programming currents to individual fuses. Special decoders, demultiplexers, buffers and mode select circuitry are needed. The circuits need not be fast since programming occurs at microsecond speeds. Because the circuitry is not used after programming, it is desirable that it consume power only during programming and not during operation. Since large voltages are required to generate programming current, survival under high voltage is also required. All of these requirements are quite different from the logic circuit requirements but must be achieved within the same part.

Testability is the third dimension of programmable logic design. This overlay of circuitry provides the means to exercise the part through all of the possible paths that might be activated by programming. Test circuitry is also needed to insure that the programming circuitry will function properly. Testability is thus important to achieving high programming yields, post-programming functionality, and performance to data sheet specifications through all possible paths.

The unique challenge of programmable logic design is to integrate these three dimensions in the most efficient manner.

Testability in the Programming Circuitry

Good programming yields are in the high ninety percent range. Advanced Micro Devices PAL device programming yields are typically higher than 98%.

Three things contribute to the high success rate in programming IMOX fuses:

1. Uniform fuse cross sections.
2. Pretesting of the current delivery and sink capability of column drivers and row drivers through use of wafer sort test pads.
3. Sample fusing of test rows.

Uniformity of Fuse Cross Sections

The IMOX process gives consistently uniform platinum-silicide fuse cross sections. Uniformity is monitored by measuring fuse resistance test patterns on a sample basis in every wafer lot. The data is processed for mean and standard deviation and trend plots are maintained. Material not meeting fuse width control limits is scrapped.

Testing for Fusing Current Delivery Capability

On every IMOX PAL device there are two extra pads that are probed at wafer sort. These extra pads are used to gain access to the fuse array for special testing at wafer sort. The connection of these pads to the fuse array is shown in Figure 5.

The programming process involves selection of individual column and row drivers to deliver and sink programming current through selected fuses. The extra test pads allow easy access for individually testing the source and sink capability of each column and row driver. Also a reverse leakage check of all of the Schottky diodes in the array is possible by applying bias between the pads. Without the test pads, all of these tests would be impossible or would have to be accomplished in a less direct and less effective manner.

Sample Programming

To further assure programmability, the IMOX PAL devices include an extra test input buffer with fuses connected to each of the array columns.

Programming one test buffer fuse per column accomplishes two important things. First, a sample fuse has been programmed using each of the column drivers. The sample fuse is exactly the same dimension as all of the normal array fuses, and the test buffer drivers sinking the programming current are identical to all of the normal drivers. Before shipment each IMOX PAL device has had a sample of fuses programmed on the test buffer.

The second purpose in programming the sample fuses is to create a pattern for AC and functional testing.

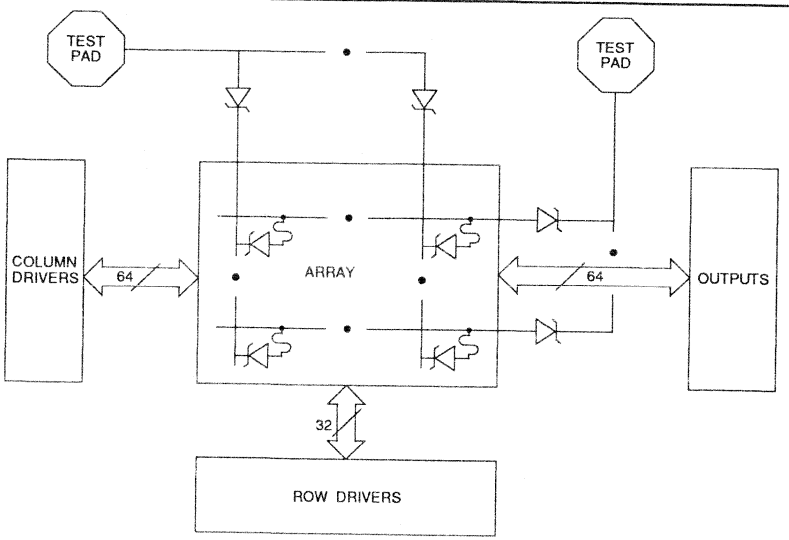

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Figure 5.

Testability to Guarantee Functionality After Programming

A typical PAL device, the PAL16R4, is shown in Figure 6. Not shown in the logic diagram are the components located at each horizontal and vertical line intersection. For IMOX PAL devices, a fuse and a Schottky diode reside at each cross point as shown in Figure 5.

The horizontal or "Product Term" line is then the common anode connection for a 32-wide diode AND gate. The user's job is to figure out which of the 32 inputs should be connected to the AND gates. The inputs not needed must be disconnected by programming the fuse shown in series with the diode.

The obvious problem from a manufacturer's test standpoint is: How can it be guaranteed through testing that the device will work after fuses are programmed? If the only logic in the device were that shown in Figure 7, testing would be nearly impossible. With 16 LOW levels and 16 HIGH levels presented to each AND gate, the LOWs win. All 64 AND outputs are thus always stuck LOW, and there is no way to get the output to toggle for AC or DC test purposes. This is the raw state of any device before programming.

Necessary Testability Requirements

Something more is needed in every PAL device to assure close to 100% functional yield after programming. The IMOX PAL devices have an overlay of test circuitry that accomplishes the following:

1. Each input and feedback buffer can be checked for functionality.
2. Each of the AND gates can be switched HIGH and LOW and uniquely sensed by an output.

These two tests are necessary to the guarantee of close to 100% post-programming functional yield.

Under normal operating conditions the test circuitry is inactive and consumes very little power. Supervoltages cause it to come alive. Supervoltages are levels substantially higher than Vcc so that under normal operating conditions accidental activation of a test mode cannot occur.

In this paper a double line on the input side of a logic symbol indicates that the HIGH level must be a supervoltage to activate it.

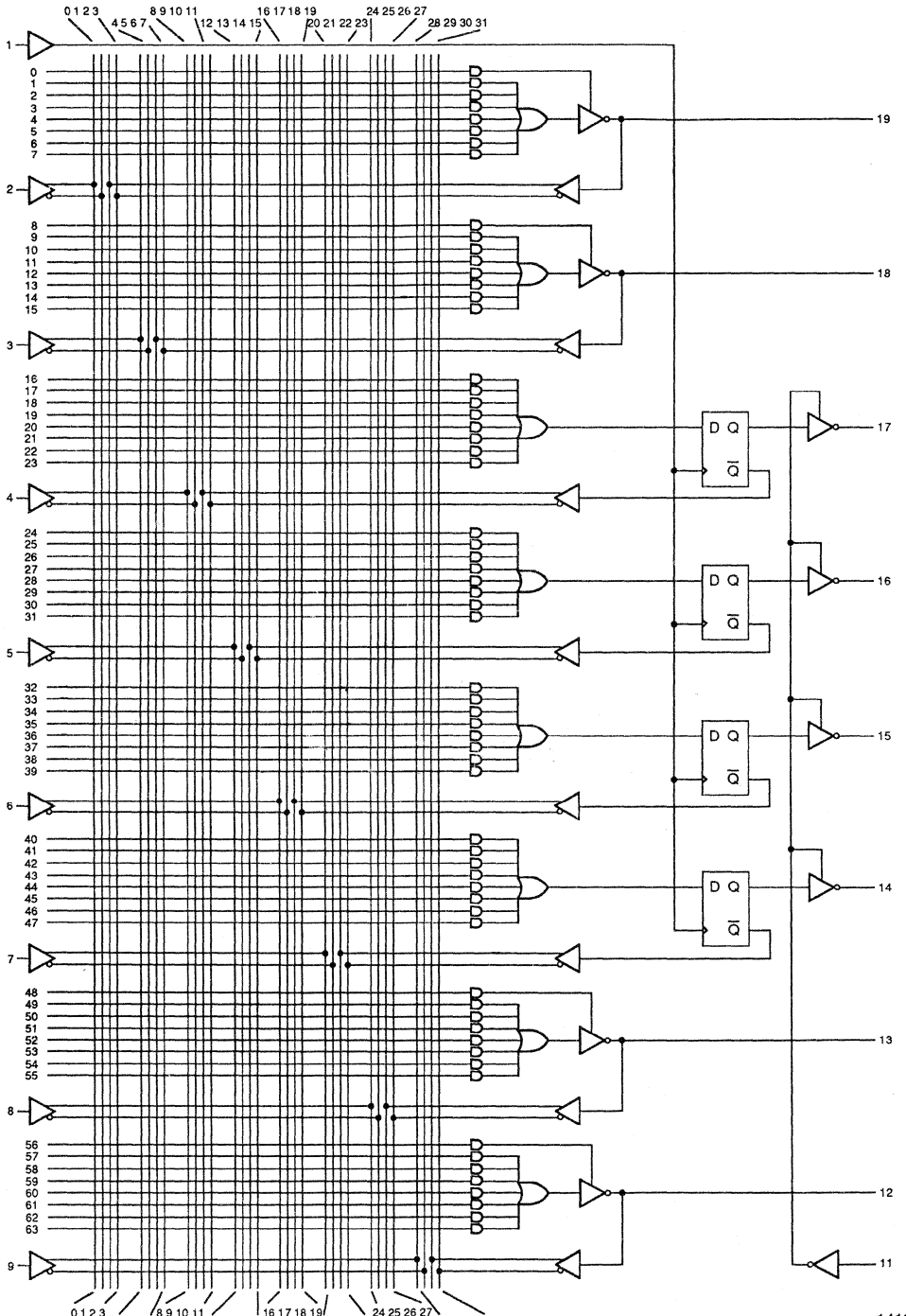
Checking the Input and Feedback Buffers

Functionality of the input and feedback buffers is checked with the aid of the extra AND gate dedicated to this function. Figure 7 illustrates the AND gate and its associated enabling circuitry.

The non-inverting or true side of each input and feedback buffer is connected to the special test AND gate. The AND gate is activated by a supervoltage on one of the input pins. The function actually takes two activating inputs to implement since the use of one for activation prevents that pin from being tested for functionality. Having an alternate pin to activate the function solves this problem.

Only the non-inverting side of each buffer is hooked up to the AND gate because each buffer is constructed from two inverters in series. The first inverter must work for the second one to work, so that checking the second one is sufficient to prove that they both work.

The feedback from the output used for the test cannot be fed to the test AND gate; such a connection would make the test output oscillate. For this reason its feedback input is not connected and is tested by creating another test AND gate on a different output and routing it there.


0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
16 17 18 19
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24 25 26 27
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Figure 6.

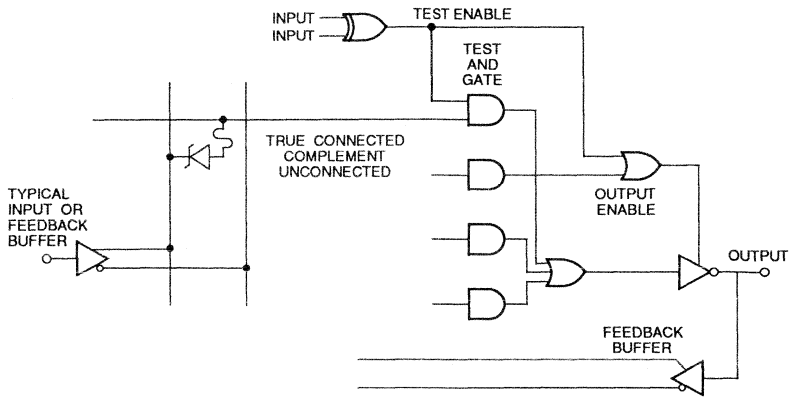

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Figure 7.

Since the special AND gate used to test all of the buffers is identical to those used in the normal operating path, switching each input through this path provides the means for testing the switching performance of each buffer.

Testing the AND Gates

The next important test requirement is to make sure that all of the AND gates work and will switch at data sheet speeds. This test challenge is little more complex.

What is needed in this case is:

1. A means of decoding one AND gate at a time in each output.
2. A way to force all input and feedback buffers to a HIGH level on both true and complement outputs.
3. A special input of identical design to a normal input that can be used to switch the decoded AND gates.

These requirements are met by the circuitry shown in Figure 8.

The decoder to select one AND gate at a time in each output serves a dual purpose. It is the same decoder that provides unique selection of product term lines for programming and fuse verification. It responds to binary combinations of TTL signals at three input pins; only one of the eight outputs will go high at a time, thereby isolating each AND gate.

The special test input that is used in this mode also serves a dual purpose. It was mentioned earlier in this paper that a programming sample was performed on each part. This special test input is the input that carries the test fuses. During the sample programming operation the fuses are programmed in a pattern that allows switching of all 64 AND gates, one in each output, for each of the eight decode states.

The input to the special buffer for AND gate testing is one of the normal input pins, but the buffer is inactive for normal operation and must be activated by supervoltage levels applied to two other inputs.

The supervoltage levels also provide the signal to force all of the buffer outputs HIGH, which is one of the three necessary requirements for AND gate testing.

Since the design of the special buffer is identical to all of the normal input buffers, it serves as a surrogate buffer for speed-testing all of the AND gates. In the AND gate test mode, all eight outputs are switched at once, since one AND gate is selected in each output. For registered outputs the AND gate switching path provides a means of testing setup and hold times.

SUMMARY

All IMOX programmable logic devices have designed-in testability and are achieving yields of greater than 98% for programming and better than 99.9% functional and AC test yields after programming. Even higher goals have been set for future products.

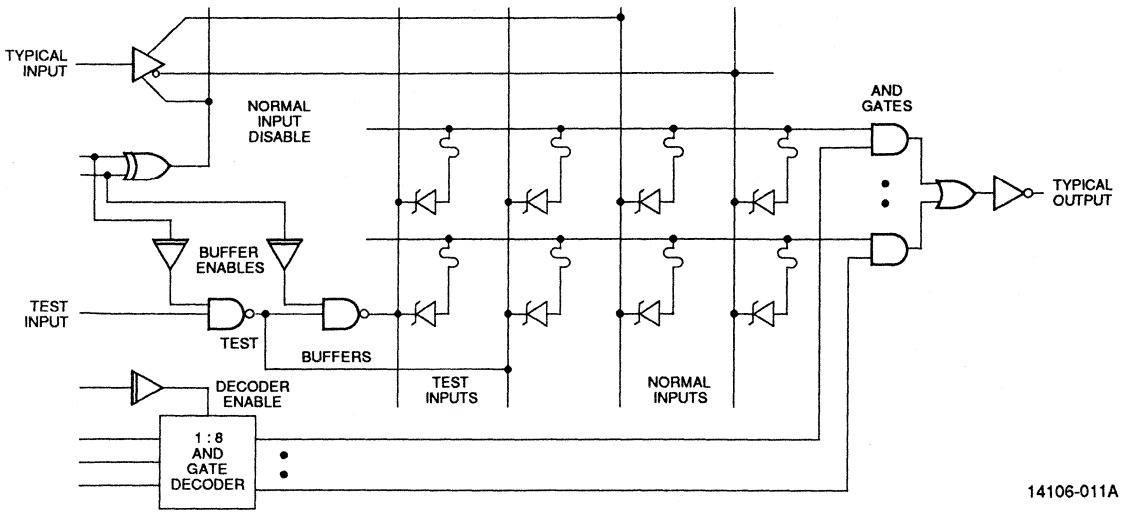

TYPICAL INPUT
NORMAL INPUT DISABLE
AND GATES
TYPICAL OUTPUT
BUFFER ENABLES
TEST INPUT
TEST
BUFFERS
TEST INPUTS
NORMAL INPUTS
DECODER ENABLE
1 : 8 AND GATE DECODER
14106-011A

Figure 8.

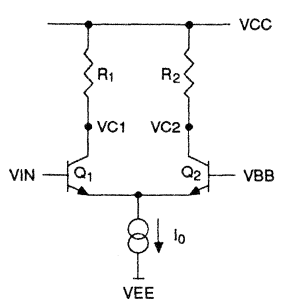
Emitter-Coupled Logic (ECL) delivers high speed, high input impedance, and low output impedance. These features are ideal for system designers who want to improve system performance. ECL achieves high speed by operating the transistor in a non-saturation mode, so that the storage-time delay associated with saturating logic is not present. When high input impedance is combined with low output impedance, large fan-in and fan-out can be achieved; in addition, low-impedance transmission lines can be driven.

Current Switch

The differential amplifier (Figure 1) is the basic building block for ECL logic; it functions as a current switch. Current I_0 is steered either through resistor R_1 or R_2 depending on the input voltage (VIN). A difference of 150 mV between VIN and VBB will cause the current I_0 to flow entirely through the transistor with the higher base-emitter voltage (VBE), due to the exponential relationship between the collector current and VBE.

When VIN is 150 mV less than the reference voltage (VBB), the collector voltage of Q_2 (VC2) will equal VCC- I_0R when $R_1=R_2=R$, and the collector voltage of Q_2 (VC1) will equal VCC. When VIN equals VBB, the two collector currents will be equal and VC1=VC2=VCC- $I_0R/2$. When VIN is 150 mV higher than VBB, VC1=VCC- I_0R, and VC2 = VCC. Although the switching threshold is 300 mV centered about VBB, the signal swing is made larger (approximately 850 mV) to provide noise immunity and to provide for differences between input thresholds of one circuit and output voltage levels of another. The values of R and the current source are chosen to determine the voltage swing and ensure the charging and discharging of parasitic capacitances at a given switching rate.

If we consider VCC to be a high logic level, and VCC- I_0R to be a low logic level, then VC1 will always be the inverse of VC2. That is, they are complementary outputs.



Emitter-Follower

To keep the current switch out of saturation, VIN must not be greater than VCC-αI_0R. For matched switching speed the voltage swing should be centered around VBB, which must also be below VCC-αI_0R by at least one half the voltage swing. To meet these restrictions, an emitter-follower is added to the current switch (Figure 2). This shifts the level of VC1 and VC2 down by a diode, and allows the logic gate to have compatible input and output levels. The emitter-follower also isolates the collector switch nodes from the output load, and provides the low output impedance that is beneficial to this logic family. On outputs, the emitter-follower can drive a 50 Ω load to –2.0 V. This allows a terminated transmission line, preventing reflections.

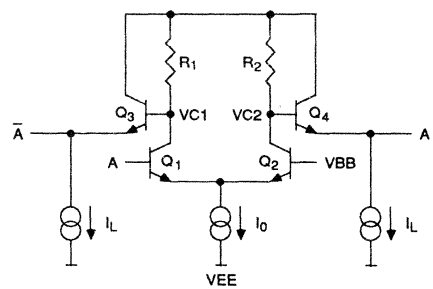


Figure 2. Gate with Emitter-Followers

OR Logic

The buffered switch in Figure 2 functions as a buffer or an inverter. By adding a second input transistor to the buffered switch (Figure 3a), a wired-AND of the collector impedances is formed at VC1. By using DeMorgan's rule, this AND function is inverted into the NOR of the two inputs. The inverse of VC1, the OR function, is generated at VC2.

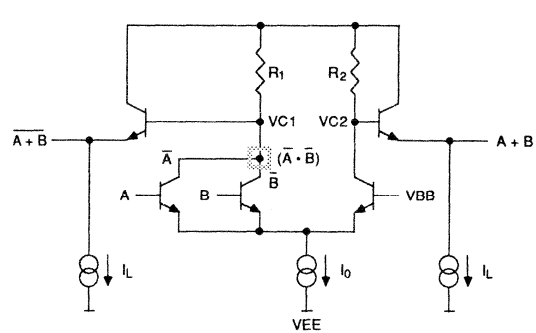


Figure 3a. OR/NOR Gate

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Additional parallel input transistors can be added to this gate to create multiple input gates (Figures 3b and 3c). The limit of the number of parallel input transistors is set by the speed of the gate; additional input transistors add more capacitance to the collector switch node forming the NOR logic. Given enough capacitance difference between the two collector switch nodes, a skew in the two outputs will occur.

Current Source

The current source used in 10KH and 100K ECL circuits is illustrated in Figure 4. The source current I_0 is set by the reference voltage VCS, the emitter resistor R_3, and the base-emitter voltage of Q_3. VCS is internally generated and is at a fixed voltage with respect to the negative supply VEE. The source current is

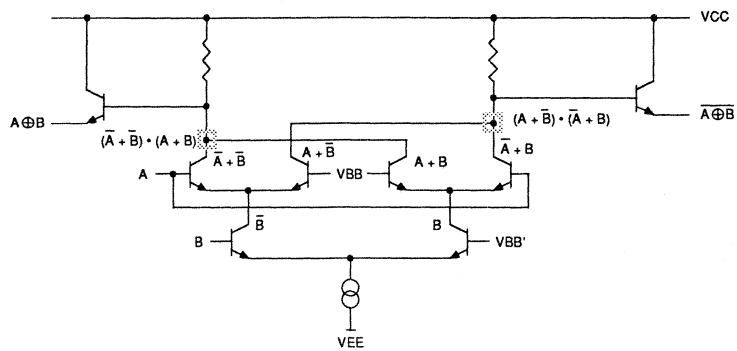

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Figure 3b. 2-Input XOR/XNOR Gate

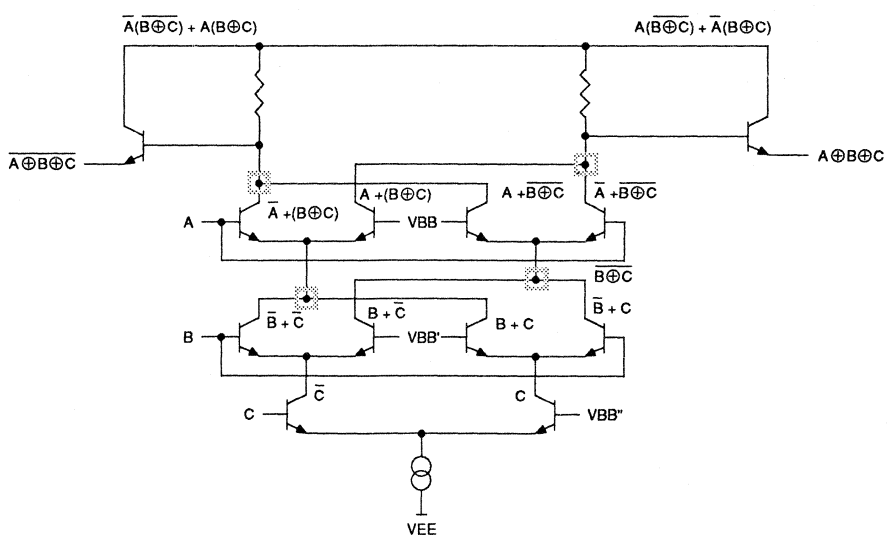

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Figure 3c. 3-Input XOR/XNOR Gate

independent of the VEE supply voltage because of this fixed voltage. The output levels are primarily determined by the collector voltages of Q_1 and Q_2. As discussed earlier, these voltages are VCC-$\alpha I_0 R$ or VCC. This relationship between the output levels and the source current makes the output levels practically insensitive to VEE variations. Thus these ECL circuits are said to be voltage compensated. The variation of output voltages with respect to VEE for the 10KH and 100K families is shown in Table 1.

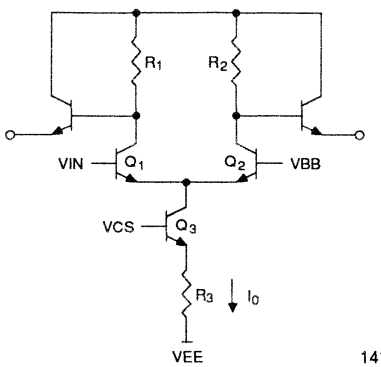

Figure 4.

	10KH	100K
ΔVOH / ΔVEE mV/V	–20	7
ΔVOL / ΔVEE mV/V	20	15
ΔVBB / ΔVEE mV/V	10	10

Table 1. Voltage Sensitivity

Input Threshold Regulation

The input threshold region is centered around VBB. VBB is internally generated and is at a fixed voltage with respect to the positive supply VCC. Variations in VEE have minimal effect in the value of VBB. The relationship between VBB and VEE is also shown in Table 1.

10KH Temperature Tracking

The output levels of 10KH circuits vary over temperature. The input threshold voltage VBB also varies over temperature to track the output variation. The temperature tracking characteristics of the 10KH output levels and input thresholds are shown in Table 2.

	10KH	100K
ΔVOH / ΔT mV/°C	1.3	<0.1
ΔVOL / ΔT mV/°C	0.5	<0.1
ΔVBB / ΔT mV/°C	1.0	<0.1

Table 2. Temperature Sensitivity

100K Temperature Compensation

The output levels and input thresholds of 100K circuits are temperature compensated. The input threshold is compensated in the bias network by referencing it to the extrapolated energy band-gap voltage of silicon (VGO = 1.3 V), which is generated in an on-chip regulator. The output levels are compensated by a cross-connect network in the current switch and a temperature-regulated current-source driver (Figure 5). The cross-connect network adds a negative temperature coefficient to the base of Q_4 when the true output of the gate is in the VOH state, which compensates for the positive temperature coefficient developed by the base-emitter junction of Q_4. Additionally this same circuit adds a positive temperature coefficient to the base of Q_4 when the gate is in the VOL state, thereby compensating for the dominant negative coefficient introduced by the gate's current source. The temperature dependence of the 100K output levels and input thresholds is shown in Table 2.

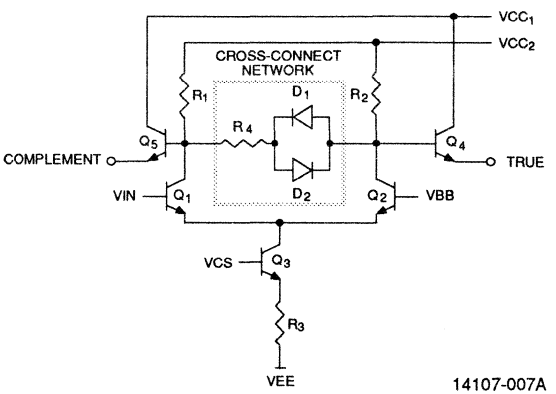

Figure 5. Output Temperature Compensation

Voltage Supply Range

Because the outputs switch high currents very rapidly, they can generate a lot of noise on the VCC line. The circuitry operates with small voltage swings, so this noise can disrupt the rest of the circuit. For this reason, multiple VCC lines are used to isolate the internal "clean" VCC from the VCC that drives the outputs, (Figure 6). If the device has many outputs, several "dirty" VCC pins may be used. As a general rule, provide one VCC for each group of four outputs.

Because of the necessity for a clean VCC supply, it is desirable to connect it to the most stable voltage in a system, which is normally ground. Thus VEE is normally negative. The normal ECL VEE supply ranges are shown in Table 3.

	NOMINAL (V)	RANGE
10KH	–5.2	±0.5%
100K	–4.5	±0.3 V

Table 3.

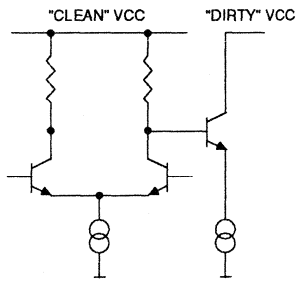

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Figure 6.

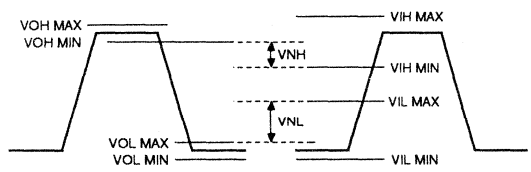

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Figure 7. Noise Margins

Noise Margins

Noise margins between circuits with different supply voltages do not degrade more than 30 mV because of the insensitivity of both the output voltage and the threshold voltage to changes in VEE. This simplifies the requirements for the system power regulation and distribution. The minimum noise margin is defined by the difference between the Min VOH and Min VIH, or VNH, and the difference between the Max VOL and Max VIL, or VNL (Figure 7).

In Table 4 the input and output electrical characteristics are shown for the 10KH family. Both VNH and VNL are 150 mV for two parts at the same temperature. With one part at 0°C driving another part at 75°C the VNL drops to 50 mV. This happens because the input thresholds and output voltages of 10KH circuits are not temperature compensated. The 100K circuits have temperature compensation and provide better noise margin for parts operating at different temperatures. Table 5 shows this; notice that input and output characteristics are specified for difference in power supply and not in temperature as is Table 4 for 10KH characteristics. The worst-case VNH for 100K parts is 115 mV. This occurs when one part has a VEE of –4.8 V and is driving a part whose VEE is at –4.2 V. The worst-case VNL for 100K parts is also 115mV. This occurs when one part has a VEE of –4.2 V and is driving a part whose VEE is at –4.8 V. The system designer must also take into account any variations in VCC from one part to the other as this will have direct affect on the system performance with respect to noise.

10KH Electrical Characteristics V_{EE} = –5.2 V ± 5%, Outputs Terminated With 50 Ω to –2.0 V

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High output voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	V dc
V_{OL}	Low output voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	V dc
V_{IH}	High input voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	V dc
V_{IL}	Low input voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	V dc

Table 4. 10KH Input and Output Characteristics

100K Electrical Characteristics $0°C < T_A < 85°C$, Outputs Terminated With 50 Ω to –2.0 V

SYMBOL	PARAMETER	TEST CONDITIONS					UNIT
			V_{EE}(V)	MIN	TYP	MAX	
V_{OH}	High output voltage		–4.2	–1.025	—	–0.880	Vdc
			–4.5	–1.025	–0.995	–0.880	
			–4.8	–1.035	—	–0.880	
V_{OL}	Low output voltage		–4.2	–1.810	—	–1.605	Vdc
			–4.5	–1.810	–1.705	–1.620	
			–4.8	–1.810	—	–1.620	
V_{IH}	High input voltage		–4.2	–1.150	—	–0.880	Vdc
			–4.5	–1.165	—	–0.880	
			–4.8	–1.165	—	–0.880	
V_{IL}	Low input voltage		–4.2	–1.810	—	–1.475	Vdc
			–4.5	–1.810	—	–1.475	
			–4.8	–1.810	—	–1.490	

Table 5. 100K Input and Output Characteristics

EE CMOS Technology

In addition to bipolar TTL and ECL and UV CMOS technologies, AMD programmable logic devices are manufactured using an advanced CMOS EEPROM-based technology. This technology offers the advantages of low power, low cost, and electrical reprogrammability for customer prototyping and code changes. In addition, since the EE cells can be reprogrammed, these devices can be 100% tested at the factory before being shipped to the customer.

Most AMD CMOS PAL® devices are manufactured with a high-performance, electrically erasable process technology called EE2. This technology has been specifically designed to fulfill the following requirements of fast programmable logic:

1. High performance
2. Low cost, high manufacturability
3. High reliability
4. Improvement path through scalability

EE2 is a single-poly double-metal CMOS process that uses an AMD-patented EE cell. This cell has a very high coupling ratio (>80%) and separate read and write paths to optimize programmability and reduce the parasitic capacitance in the speed path. Table 1 summarizes EE2's main characteristics.

Table 1. EE2 Technology Summary

CMOS N well	
Substrate	Grounded
Polysilicon	Single
Metal	Double
Minimum Feature Size	1.2 µ
Gate Length on Wafer	1.2 µ
Gate Oxide	225 Å
Contact Dimension on Wafer	1.8 µ
Metal 1 Pitch	4.0 µ
Metal 2 Pitch	4.8 µ

The single-poly solution has been chosen for the following reasons.

COST AND MANUFACTURABILITY

Being a single-poly process, the number of masking steps is reduced. The process is very comparable to high-performance, high-volume logic and SRAM processes. This allows the devices to benefit from the economies of scale and extremely high yields associated with high-volume manufacturing.

PERFORMANCE

The single-poly solution makes it easier to implement very tight dimension controls, required for high performance, in high-volume manufacturing.

RELIABILITY

With the single-poly solution, the traditional interpoly dielectric is replaced by a high-quality gate oxide. The thermal stress on the tunnel oxide is reduced by the absence of interpoly dielectric and second-poly deposition steps. This increases both data retention and endurance.

AMD specifies an endurance of 100 cycles for EE2-based CMOS PAL devices, which is sufficient for logic applications. The data retention specification is 20 years at the absolute maximum operating temperature and 10 years at the absolute maximum storage temperature.

SCALABILITY

Being very close in architecture to a standard high-performance logic process, EE2 will very easily benefit from the progress made on technology drivers such as SRAMs. This guarantees a smooth evolution from one generation to another, providing higher performance and lower cost.

In summary, by considerably simplifying the process, the single-poly solution allows the use of very high-performance CMOS technology for low-cost programmable logic devices.

Publication #	Rev.	Amendment	Issue Date
14108	A	/0	1/90

INTRODUCTION

Product Assurance consists of Quality Control, Reliability Assurance, Quality Assurance for Military Products and Quality Assurance for Commercial Products.

Quality Assurance

Quality Assurance for the Commercial Products includes customer support and failure analysis, outgoing inspection and factory support, document control and quality information.

In order to support customers, QA provides actual data generated during various monitors and inspections throughout the factory. Non-proprietary data is available upon request. If the specific data is not immediately available, experiments can be run to collect the necessary information subject to resource and time limitations.

Another aspect of customer support is the performance of failure analyses. Failure analyses are broken down into three levels. Level 1 analysis consists of failure verification using an automatic tester. The result is only whether or not the device under test is good or bad with a datalog pointing out the potential failure mode. Level 2 analysis consists of Level 1 plus the verification at a bench top setup which results in confirmation of the failure mode with detailed specific data. Level 3 adds to Level 2 a decap and physical analysis to isolate the failure mechanism. Advanced Micro Devices has the capability to perform the total analysis in house, but occasionally sends analyses to outside sources whenever circumstances deem it necessary. Quality Engineering goals for cycle time are to complete Level 1 analyses within seven days, Level 2 within 14 days, and Level 3 within 30 days.

Not all customers want or need a full Level 3 analysis every time. The level can be specified at the time of submission. A failure analysis should be requested through the Sales person or Field Applications Engineer (FAE). A failure analysis request form will be completed at that time and the request form and suspected failure(s) will be forwarded to Quality Assurance.

Upon completion of the analysis, a formal report will be made to the requester. The report will summarize the results of the analysis and enumerate the steps followed in performing the analysis. In most cases, a statement of the corrective action taken to prevent future occurrences will be included for valid failures. In those cases where no failing condition is found, the device(s) and report are forwarded to the requester.

Quality Assurance supports the factory with periodic auditing of the various processes, areas and products. The Discrepant Material Reporting system (DMR) provides the factory feedback on the level of quality it is producing as well as providing protection to our customers via a gating of the product. The Quality Inspection group takes a 200 piece sample (.065% AQL for lot sizes according to Mil–HDBK–105D) from each production lot for visual and mechanical testing and electrical testing. The lot is returned to production for rescreening if a defective unit is found in the sample. The results of the inspections are summarized and reported weekly. Through programs aimed at solving the causes of the defects, Advanced Micro Devices has improved quality levels significantly.

As a customer, you can learn from our experience. Our data suggests that handling is the number one cause of defective material. Whether it is human handling or not, the product flows should be engineered so as to minimize the number of separate handling steps. By ordering completed product in even box quantities, no handling should be necessary after the product has been packaged by the factory. Product can be placed into boards upon receipt.

By placing product directly into boards without incoming inspection and handling, ship-to-stock has been accomplished. Ship-to-stock, also known as dock-to-stock or certification, is an electronics industry goal. It accomplishes minimum cost objectives of our customers. The ship-to-stock decision is a customer decision that is based on the confidence one has in their supplier to provide consistent, high quality. Advanced Micro Devices has mechanisms in place to support ship-to-stock programs and has a generic recipe for the certification process for those who would like to get a head start on a such a program. Refer to the outline of Guidelines for Product Certification.

Quality Improvement Programs

The Product Quality Objective is divided into the following components:

- Reliability
- Electrical Performance
- Programmability
- External Visual/Mechanical
- Internal Die Visual
- Total Quality Process
- Quality Partnership Program

Reliability

The reliability program consists of new product, package and process qualifications, qualifications of product, package and process changes, and product, package, and process monitors. Most reliability testing is performed on site in Santa Clara.

Qualification requirements are generally customer driven. Advanced Micro Devices has developed a procedural specification that attempts to cover most of the requirements of our numerous customers. Most test methods follow the Mil-Std 883 method if applicable.

The most common stresses are operating life, temperature cycling, and temperature and humidity testing. Advanced Micro Devices performs operating life at 125 degrees Celsius, 5.25V Vcc, and 1000 hours per method 1005, condition D. In some instances the time will be extended for information only. Operating life is performed dynamically by applying 100KHz to the inputs of the devices under stress. Interim readouts are generally made after 168 hours. The junction temperature is kept below 175 degrees Celsius. Temperature cycling is performed from –65 to 150 degrees Celsius for 100 cycles per method 1010, condition C.

Temperature and humidity, usually referred to as 85/85 testing, is performed with devices biased. Both Vcc and ground are held at ground potential while the rest of the pins are biased to 5 volts. The name 85/85 comes from the temperature and humidity settings of 85 degrees Celsius and 85% relative humidity. Devices are stressed for 1000 hours.

Many other stress tests are performed including ESD testing. Advanced Micro Devices has a complete ESD control program in all post wafer fabrication areas. All necessary facilities are in place and training is carried out on a routine basis. Audits are also made of the manufacturing areas to ensure adequate control is maintained at all times.

The monitor program is intended to continually look at production products, packages and processes. Each month a series of product, package, and process combinations are selected to be monitored. Each quarter one product from each process and package is thus checked. Any defects are analyzed in the manner previously presented.

Whenever a major change is made to a product, process, or package, a re-qualification test is run. In addition to requalification, notification is made through the sales organization to those customers that have such notification requirements. Advanced Micro Devices generally notifies customers at least 90 days prior to implementation of a major change.

All the data are summarized and published twice per year in the Reliability Report. Copies of the report are available upon request.

Electrical and Visual/Mechanical Quality

The basis of the quality improvement program has been thorough analysis of and corrective action for defective units found in four main areas. The Discrepant Material Reporting system stems from outgoing sampling performed by the QA Inspection group on each production lot of devices. QA uses a 0.065% AQL sampling plan per Mil Std 105D which generally results in a 200 piece sample. Any lot with a defect in the sample is returned to manufacturing for rescreening.

The Parts Per Million monitor is a unique effort to emulate the results that our customers find by using our products. The significant feature of the monitor is that the parts utilized are pulled from finished goods, the point closest to the customer but still within the factory. Devices are tested at room and hot temperature to arrive at an electrical PPM and visually inspected to arrive at a visual/mechanical PPM. In addition, samples are sent for programming and static burn in. In this way programming yield and infant mortality information are generated.

Defective devices from either of these factory locations are analyzed, summarized and have corrective actions generated by manufacturing and engineering. Formal reports are made to corporate management in the bimonthly Product Quality Review, which is a general meeting dedicated to reporting progress toward quality goals.

Two sources of customer feedback are the Customer Material Returns and failure analysis systems. Customer Material Returns (CMR) are generally returns by customers who are concerned with receiving credit or replacement of defective units they have found. These units are verified by a level 1 analysis as explained previously and summarized weekly and monthly in formal reports to management.

The fourth area of feedback is through the failure analysis system which has already been presented.

The results of the efforts have been the steady reduction in PPM levels to below 250ppm electrical, below 500ppm visual/mechanical, and below 0.1% infant mortality failures.

Programmability

In addition to improving product quality, we have improved programming yields to higher levels. Improvement has come through algorithm revisions, random defect reduction, redesigns of products and programmer qualification. Once we began focussing on the programmer suppliers, we were able to better understand their programming processes and work much more closely with them to develop optimal programming algorithms. While this in itself helped to improve yields, we also made some design "tweaks" and manufacturing improvements that contributed further toward reaching levels generally above 99.5%. Post programming functionality was also improved.

Some of the issues that should be considered when considering performing your own programming are to maintain adequate calibration of programmers including replacing sockets after 10,000 insertions, inventory handling costs, human handling errors, and lack of post programming testing. Advanced Micro Devices can provide programmed product with minimum cost and handling that falls below 100ppm. This can be a significant reduction in the cost of quality and make it easier to move to a just-in-time manufacturing system.

Internal Die Visual

It is Advanced Micro Devices' intent to supply die quality that meets or exceeds the Mil-Std 883, method 2010, class B. Toward this goal, Advanced Micro Devices has made significant improvements through random defect reduction in our manufacturing areas and through the use of statistical process control techniques. Significant defect reduction was gained by automating the assembly process to remove human handling. Similarly, automation in the wafer fabrication areas has also been effective. One significant improvement was made by putting pelicles on all

photolithographic wafer masks. In addition to preserving the plate indefinitely, the pelicle causes any particle that should happen to fall onto the plate to be out of focus on the wafer. Therefore, a perfect print is made every time.

Die visual quality has improved to over 97% conformance to method 2010, class B in molded packages and to 100% conformance in hermetic packages. The die visual improvement has also contributed to the improvement in infant mortality and the improvement in programming and post programming functionality.

Total Quality Process

Up to this point, the discussion has centered around detection and inspection to find quality problems and fix them. However, the long term trend is toward prevention. Statistical process control is a preventive measure that allows for building in quality by quickly heading off problems before they occur. Statistical process control (SPC) is the mainstay of a total quality approach.

Total Quality means the molding of attitudes through continual education, training and awareness in all areas, and to establish SPC in all manufacturing areas. The vehicles for accomplishing total quality are the bimonthly Product Quality Review, Quality Improvement Teams, Deming seminars, in house SPC training, use of SPC consultants, and an automatic data collection and analysis.

The actual use of SPC in manufacturing can be seen in both the U. S. and in the assembly facility in Penang, Malaysia. The assembly areas are leading the way with on line monitoring and real time charting in most operations. The wafer manufacturing areas have attained various levels of penetration.

The future holds more automation in store for SPC. We have implemented a computer integrated system of data collection and analysis that will eventually allow for on line analysis, automatic data collection and automatic line control. We will be pushing ahead with more Taguchi techniques and with an SPC program to address non-production areas. And the bottom line will be to reduce our cost of quality through reduction in inspection and detection costs and to eliminate rework.

Quality Partnership Program

Several years ago Advanced Micro Devices developed the Quality Partnership Program in order to facilitate quality improvement through enhanced feedback from a few customers that had good reporting mechanisms in place. Today, the program is basically the same with one very important exception. Advanced Micro Devices has attained quality levels below 250ppm as we measure ourselves. Through pareto analysis of your supplier base, you may not want to make the commitment necessary to sustain a true partnership relationship with a supplier that does not rank as one of your problems. But if you should, we are always ready to participate toward mutual improvement in quality. We have mechanisms in place to provide rapid and thorough failure analysis and outgoing inspection data on a regular basis. All that is needed is a commitment from our customers to provide us with rapid feedback and to be willing to work in tandem toward zero defects and minimum costs. The usual result of a successful partnership is reaching ship-to-stock and building a working relationship based upon trust and mutual understanding.

The quality programs described have been in existence for several years. The results have been dramatic. You will find us to be very honest and responsive to your needs. If you should need some information, please don't hesitate to contact us.

GUIDELINES FOR PRODUCT CERTIFICATION

Characteristic Accountability

- Process Flow
- Product Specification
- Monitors and Controls
- Place of Manufacture
- Establish Correlation

First Article Inspection

- Electrical Conformance
- Visual/Mechanical Conformance
- Variables Data

Lot Monitoring Inspection

- Lot Acceptance or Defect Rate Maintenance
- Period of Time or Number of Lots Criteria

Factory Audit

- Customer

Certification

- Certification Maintenance Program
- Disqualification and Recertification Program
- Periodic Reports, Data, and Timely Feedback
- Special Outgoing Inspection and Verification
- Change Notification

PRODUCT ASSURANCE

Quality Assurance-Military

- Facility Certification
- QPL Qualifications
- JEDEC 13/13.2 (Gov't Liason Committee)
- 38510 Quality Conformance Inspection

Product Acceptance

- Electrical Test Gates
- Visual/Mechanical Gates
- Traceability Verification
- Government/Customer Liason
- Final Outgoing Inspection
- Inspection Activity Reporting
- Verifies Conformance With MIL-M-38510 QCI Requirements

Quality Assurance Eng.

- Self Audits
- Corrective Action
- Calibration Control
- Customer Return Disposition, Reports and Failure Analysis
- Technical Resource
- Major Programs Support
- Division Quality Assessment Program
- Quality Partnership Program
- Configuration Control

Reliability Assurance Eng.

- Customer/Gov't Quality Conformance Inspection
- Package, Process and Reliability Studies (New/Revised)
- Division/Reliability Reporting
- CECC Reliability Programs

Quality Control

- Incoming Inspection/Vendor Evaluations, Ratings and Corrective Action
- In-Line Procedural Audits (Fab Through Final Seal)
- In-Line Operational Audits (Fab Through Final Seal)
- In-Process Wafer Fab Inspection
- In-Process Wafer Sort Inspection
- In-Process Assembly Inspection
- Offshore Assembly Surveillance
- Offshore/Surveillance Correlation Program
- Analytical Lab Services (Di Water, Chemical Analysis)
- Environmental Audits (Temp., RH, Particle Counts and Flow Hood Velocity)
- In-Process CSI/GSI
- Quality Engineering Failure Analysis
- Statistical Control, Product Quality Analysis

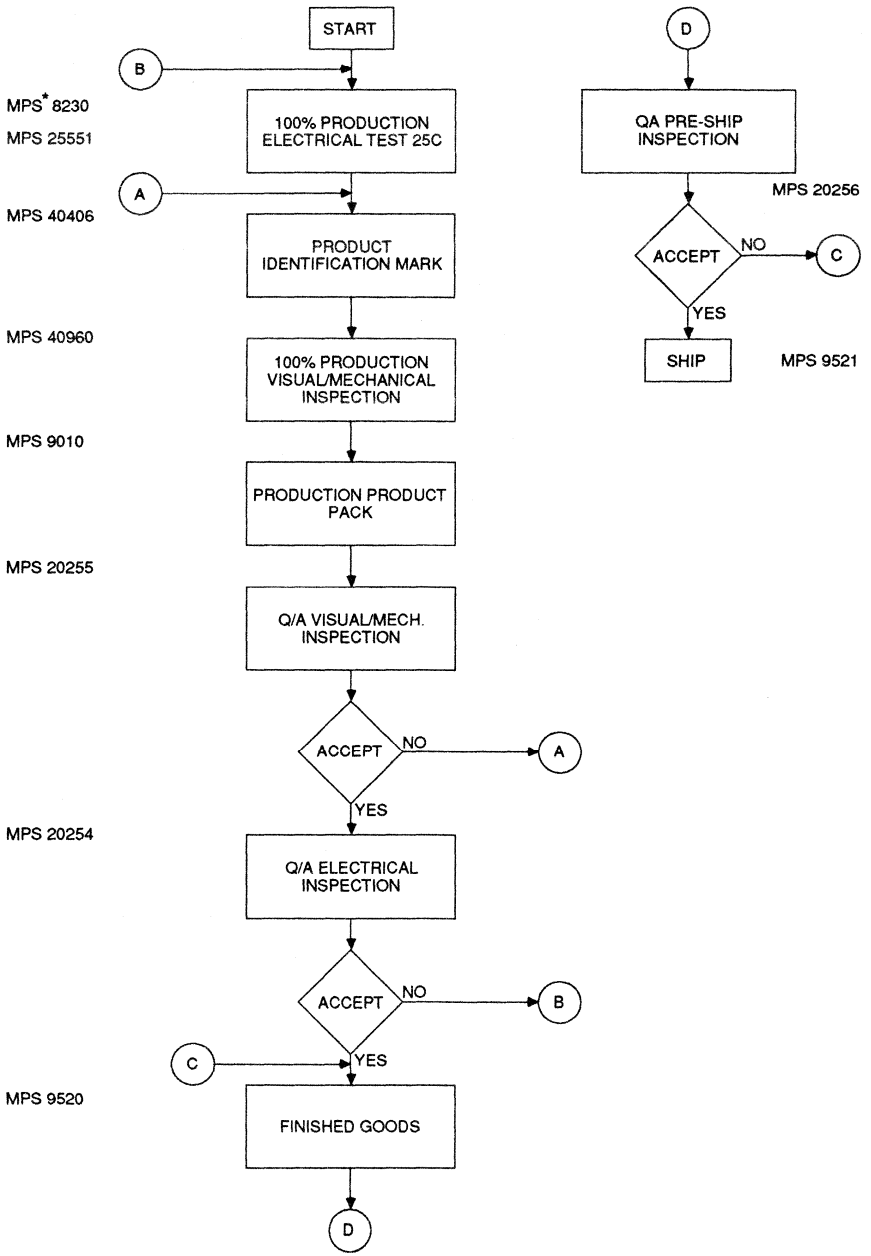
Quality Assurance-Commercial

- Self Auditing
- Customer Material Returns Analysis and Corrective Action
- Discrepant Material Analysis and Corrective Action
- Technical Support
- Major Program Support
- PPM Monitor Support
- Quality Partnership Program
- Electrical Test Inspection
- Visual/Mechanical Inspection
- Final Outgoing Inspection
- Inspection Activity Reporting
- Commercial Traceability
- Conformance Verification of Special Commercial Specifications
- Document Control (Commercial)

Reliability Assurance

- Device/Design Qual (New/Revised)
- Package Qualification (New/Revised)
- Process Qualification (New/Revised)
- On-Going Device/Package Reliability Monitors
- Extended and Accelerated Life Testing
- Qualification Test Lab Per MIL-STD-883 Method 5005
- 38510 Device Qualification and 883 Quality Conformance
- Failure Analysis Lab (SEM/EDAX and Engineering Services)
- Early Failure Mode Detection and Corrective Action
- Reliability Reports (In-House and Field)

STANDARD POST ASSEMBLY PROCESS FLOW



14109-001A

* Internal Manufacturing Process Specification Number

Advanced Micro Devices' test and finish operations utilize state of the art electronic testing equipment as well as Electro-Static Discharge safeguards in all handling areas. Inventory is maintained and controlled via computerized database systems assuring one of the best on-time delivery systems in the industry. The product quality is monitored continually throughout the process to provide feedback necessary to support factory corrective actions.

Electrical Testing/Pre Burn-In

The electrical test of integrated circuits starts long before a batch of parts is dispatched to the test area. Product and process characterizations must be performed to understand the parametric distributions and the test conditions that are necessary to provide full compliance to datasheet specification. When the customer order requires programming, functional test vectors are computer generated and evaluated for array coverage. Test software is validated for performance margin before being handed over to the Test area for use in production. The electrical test software is maintained through revision control and sign-off procedures.

Devices are delivered to the Test area for initial electrical testing. The product is 100% production tested to guarantee the databook requirements and functionality. The parameters specified include electrical and switching characteristics. In addition Advanced Micro Devices performs these tests at various ambient temperatures in order to eliminate marginal devices. Additionally, test program forcing conditions and test limits have been guardbanded to reduce the effects of system variability and parameter shift at temperature. All test equipment is calibrated to standards traceable to the National Bureau of Standards.

For reduced costs and improved quality due to the elimination of human handling errors, Advanced Micro Devices is incorporating bulk loading equipment into the Test and Finish areas. These machines can load and unload product from a handler with great speed, efficiency, and accuracy.

Burn-In

Semiconductor failures over time are known to manifest themselves during the earliest stages of useful life. This phenomenon is known as "Infant Mortality." During burn-in, stresses are applied that accelerate failure for those devices which are prone to Infant Mortality. The elimination of these failures not only improves the reliability, but also results in substantial cost savings for system manufacturers by reducing rework and repair loading.

Typical conditions for burn-in are:

Static Condition C
Temperature: 125°C
V_{cc}: 5.25 V

The typical infant mortality phase is defined as 168 hours, with 75% of the defectives found in the first 48 hours.

Advanced Micro Devices has reduced mechanical handling defects during board load and unload by utilizing robotic handling/loading equipment.

Electrical Test/Post Burn-In

The devices which are burned-in are again electrically tested to remove any failures that are a result of the Burn-in accelerated stresses. Production and engineering monitors have shown that the typical failure rate for this stress is approximately 0.05%.

Marking

The devices are marked to provide identification of part number, AMD or MMI logo, assembly location, and date codes. In addition to standard marking, special customer required items are available. A photolithographic process is used to produce exceptional character clarity. Every lot is tested for marking permanency.

Traceability of all raw materials, equipment, operators and processes are identified by two unique date code numbers found on the top and bottom of the package. A six-digit code marked on the top-side of the device allows traceability of the test and finish operations, and an eight-digit bottom-side code for traceability of assembly processing and raw materials back to wafer lot.

Visual/Mechanical Inspection

Visual and Mechanical inspection is performed on all production units. The inspection includes package outline dimensions, and lead and marking quality. With the aid of production monitors and statistical process controls, marginal processes are eliminated.

Pack

Packaging of devices is no simple matter. One must provide mechanical strength, and identification of contents as well as electrical protection (from ESD). Advanced Micro Devices utilizes carbon impregnated boxes for the intermediate containers of a shipment, which act as faraday cages in dissipating the built-up electro-static charges. The box label has printed on it the part number, package type, quantity of devices, QA stamp of acceptance, specification number, date of pack, and bit pattern (if programmed). Many of the above items are also printed in machine-readable bar code format to assist in product movement and control.

Quality Assurance Visual/ Mechanical and Electrical Inspections

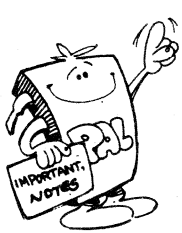
The Quality Assurance department sample inspects the devices to a 0.065% AQL sample plan in accordance to Mil-HDBK-105D.

The visual/mechanical inspection consists of physical dimension checks along with lead, marking, and packaging verification to ensure quality.

Paperwork is also reviewed for accurate and complete processing to specification and customer requirement.

The devices are electrically tested to databook and/or specific customer conditions and limits to validate the electrical and functional integrity.

Any non-conformities that are found during QA inspection are verified and tracked through the appropriate product/assembly engineering group to obtain corrective action. This information along with inspection volume and failure rates is reported to management, operations and engineering regularly for long-term trend visibility and improvement.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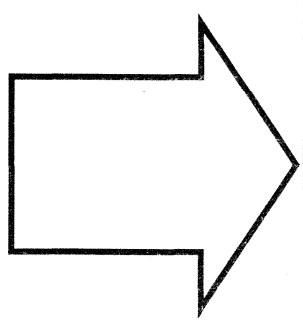

Appendices

AMD PLD Conversion Chart

This conversion chart lists all AMD PAL® devices and other PLDs that have been removed from the previous version of this data book. These products are either not recommended for new designs or discontinued, and have appropriate replacement devices listed. For details and assistance in converting from any of these devices, or for any questions you may have, contact your local AMD sales office.

Not Recommended for New Designs	Use Instead
PAL10H20G8 PAL10H20P8	PAL10H20EG8
PAL10H8 PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	PALCE16V8
PAL16C1	Contact AMD
PAL12L10	PALCE22V10
PAL14L8 PAL16L6 PAL18L4 PAL20L2	PALCE20V8
PAL20C1	PALCE22V10
PAL16L8A-4 PAL16R4A-4 PAL16R6A-4 PAL16R8A-4	PALCE16V8Q
PALC16L8Q PALC16R4Q PALC16R6Q PALC16R8Q	PALCE16V8Q
PALC16L8Z PALC16R4Z PALC16R6Z PALC16R8Z	PALCE16V8Z
AmPAL16L8 (all options) AmPAL16R4 AmPAL16R6 AmPAL16R8	PALCE16V8
PAL16P8A PAL16RP4A PAL16RP6A PAL16RP8A	PALCE16V8
PAL16X4	Contact AMD
AmPAL18P8Q	PALCE16V8Q
PALC18U8	PALCE16V8Q
PAL20L8Z PAL20R4Z PAL20R6Z PAL20R8Z	PALCE22V10Z
PALC/E20RA10Z	PAL20RA10
AmPAL20RP4 (all options) AmPAL20RP6 AmPAL20RP8	PALCE20V8
AmPAL20RP10	PALCE22V10
PAL20S10 PAL20RS4 PAL20RS8 PAL20RS10	PALCE22V10
AmPAL20XP10 (all options) AmPAL20XRP4 AmPAL20XRP6 AmPAL20XRP8 AmPAL20XRP10	PALCE22V10
PAL22RX8A	PAL32VX10A
PALC22V10	PALCE22V10
PAL32R16	PALCE29M16
PAL8L14A PAL6L16A	Contact AMD
PMS14R21/A	Am29CPL151
Am29PL141 Am29LPL141 Am29CPL141	Am29CPL151
Am29PL142 Am29CPL142 Am29CPL152 Am29CPL144	Am29CPL154
ZHAL™ Family	PALCE16V8Z PALCE22V10Z

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Glossary

10KH (adj.) A family of ECL devices. Circuits are temperature compensated. See also: ECL, 100K, temperature compensation.

100K (adj.) A family of ECL devices. Circuits are both temperature and voltage compensated. They have lower power dissipation and higher speed than their 10KH counterparts. See also: ECL, temperature compensation, voltage compensation, power dissipation, 10KH.

A

active high (adj.) See polarity.

active low (adj.) See polarity.

ALS (adj.) Advanced Low-power Schottky TTL family. Characterized as a lower power version of the AS family, and actually faster and lower power than the LS family. See also: AS, LS, TTL, Schottky TTL.

AND 1. (adj.) One of the three elementary logic functions. Result of the AND operation is true if and only if all operands are true. 2. (v.t.) To perform the AND operation.

AS (adj.) Advanced Schottky TTL family. High-speed versions of the standard Schottky TTL family. Generally use oxide isolated technology for very high speed. See also: Schottky TTL, TTL, oxide isolation.

assertive high (adj.) Same as "active high". See polarity.

assertive low (adj.) Same as "active low". See polarity.

astable (adj.) Describes a system which has no stable state. Such a system will oscillate. Astable circuits can be used to generate timing and synchronizing clock signals. See also: bistable, monostable.

asynchronous 1. (adj.) Describes a sequential logic system wherein operations are not synchronized to a common clock. 2. (adj.) Describes signals whose behavior and timing are completely unrelated to a particular clock. Such signals can either be random or based on another clock which has a different frequency. 3. (adj.) Describes a communication protocol whereby the timing of various operations is not determined by a system clock, but rather by events whose relationships are known, but whose exact timing cannot be precisely predicted. See also: sequential, clock, synchronous.

B

BCD (n.) Binary Coded Decimal. Decimal numbers in 4-bit binary.

binary (adj.) Having only two possible states, which can be variously called on/off, 1/0, true/false, high/low, etc.

bipolar (adj.) One of the two basic types of transistor. In logic design, used for TTL, ECL, and I^2L families. See also: TTL, ECL, I^2L, MOS.

bistable (adj.) Describes a system which has 2 stable states. Any other state is unstable, and will eventually change to one of the stable states. A flip-flop is the most common electronic bistable circuit. See also: flip-flop, astable, monostable.

bit 1. (n.) Binary Digit. One unit of binary information. 2. (n.) A measure of the storage capacity of a memory chip. See also: binary.

blank (adj.) Describes the state of a programmable cell after manufacturing, and before any programming, or, in the case of an erasable device, after erasure. Opposite of "programmed". See also: programmable cell, programmed, program, erase.

buffer (n.) A logic gate which performs the logic identity function; i.e., the input is passed through unchanged. Used to isolate various parts of a system, or to provide voltage or current amplification.

C

chip (n.) A single piece of semiconductor material which contains an integrated circuit. Sometimes called a die if not in a package. See also: integrated circuit, die, package.

clock 1. (adj.) A signal used to synchronize the operation of a system. 2. (adj.) An input to a clocked flip-flop. The flip-flop will not change state until an appropriate pulse appears at the clock input. 3. (n.) A circuit which generates a clock signal. 4. (v.t.) To pulse the clock signal or the clock input of a clocked flip-flop. See also: flip-flop, clocked flip-flop.

clocked flip-flop (n.) A flip-flop that does not change state until a clock signal is received. See also: flip-flop, unclocked flip-flop, clock.

CMOS (n., adj.) Complementary MOS. A type of circuit which makes use of both N-channel and P-channel MOS transistors. Many CMOS logic circuits consume no power when not actually switching. See also: MOS, NMOS, PMOS, standby power.

combinational (adj.) See combinatorial.

combinatorial (adj.) Refers to a logic circuit which implements logic functions of present input signals only. Also called combinational. See also: sequential.

complement 1. (adj). Refers to a signal which is identical to some reference signal, except that it is of opposite polarity. Opposite of "true". 2. (v.t.) To invert. See also: true, polarity, invert.

complementary (adj.) Refers to logic device outputs which implement identical logic functions, but with opposite polarities. Used on some PLDs and ECL devices. See also: polarity, PLD, ECL.

D

decimal (adj.) Based on the number 10.

die (n.; plural: dice) Same as a chip, particularly before being placed in a package. See also: chip, package.

digit (n.) Any number from 0 to 9.

DIP (n.) Dual In-line Package. The most common integrated circuit package. It is rectangular in shape, with widths ranging from .300 inch to .900 inch, and has vertical leads along the length. Available for up to 64 pins. See also: integrated circuit, package.

disable 1. (v.t.) To turn off a three-state output. 2. (v.t.) To inhibit another function, such as "disabling the clock". See also: three-state, enable.

download 1. (v.t.) To pass data from one machine to a less complex machine. 2. (n.) The act of downloading data. See also: upload.

E

ECL (n., adj.) Emitter Coupled Logic family. An extremely high speed family of bipolar logic and memory devices. See also: bipolar.

EE cell (E^2 cell) (n.) A floating gate cell which can be both programmed and erased with electrical signals.

EEPROM (n.) Electrically Erasable Programmable Read-Only Memory. A nonvolatile read-only memory device which can be erased and reprogrammed, both with special electrical signals. See also: program, erase, EPROM, PROM, ROM, RAM, non-volatile.

enable 1. (v.t.) To turn on a three-state output. 2. (adj.) By itself, usually refers to a pin which is used to enable a three-state output. Also called "output enable". 3. (adj.) Used with other function names, indicates a qualifier or inhibitor of the function. For example, "clock enable" is a function which qualifies the clock function. 4. (v.t.) To allow a signal which has been disabled to function; for example, "enabling the clock" removes any restraint which may disable the clock signal. See also: three-state, disable.

EPROM (n.) Erasable Programmable Read-Only Memory. A non-volatile read-only memory device which can be erased and reprogrammed. Erasure is accomplished by exposing the die to ultraviolet light for a period of time. Die must be packaged in a windowed package to allow erasure. See also: program, erase, EEPROM, PROM, ROM, RAM, non-volatile, windowed package.

erase 1. (v.t.) To return a programmed device to its blank state. Opposite of "program". 2. (v.t.) To return an individual programmable cell to its blank state. See also: blank, programmable cell, program.

ESD (n.) Electrostatic Discharge. The natural physical event of the transferring of electrical charges. If uncontrolled, ESD can destroy or degrade both CMOS and bipolar semiconductor devices with inadequate on-chip protection circuitry and/or insufficient packaging and handling protection. See also: ESDS Device, CMOS, bipolar.

ESDS Device (n.) Electrostatic Discharge Sensitive Device. A device which is sensitive to damage at certain levels of ESD. Three classes exist at ESD levels of up to 1999V, to 3999V and above 4000V. See also: ESD.

F

finite state machine (FSM) (n.) A machine which can be in one of a finite number of states. Often used for logic circuits which sequence through various states. Such a circuit is referred to as sequential. See also: sequential.

flip-flop (n.) A bistable digital circuit. The simplest variety is called an S-R flip-flop. Other types are J-K, T, and D-type. May be unclocked or clocked. See also: bistable, unclocked flip-flop, clocked flip-flop.

floating gate (n.) A gate on an MOS transistor which is not connected to anything. Used to store charge; forms the basis of UV cells and EE cells. See also: MOS, gate, UV cell, EE cell.

FPGA 1. (n.) Field Programmable Gate Array. A high-density PLD with multiple levels of logic and programmable interconnect. 2. (n.) Field Programmable Gate Array. An array of logic gates whose configuration can be programmed by the customer. The gates are often NAND gates, but can also be NOR gates. See also: gate, program, NAND, NOR.

FPLA (n.) Field Programmable Logic Array. See PLA.

FPLS (n.) Field Programmable Logic Sequencer. A programmable logic device which is intended for sequencing or state machine applications. See also: finite state machine.

functionally complete (adj.) Refers to a logic operation or group of operations from which any complex logic function can be built. The NAND and NOR operators are functionally complete. See also: NAND, NOR.

fuse (n.) As used in programmable logic, usually refers to a lateral metal link fuse. See also: lateral fuse.

fuse map (n.) A graphic representation of the contents of a PLD. The state of each connection (fuse or other programmable cell) is represented, usually with "X" indicating an intact connection, and "-" indicating an open connection. See also: PLD, programmable cell.

G

gate 1. (n.) A fundamental logic element. The elementary gates provide NOT, AND, and OR logic functions. 2. (n.) The control terminal of a gated D-type latch. See also: latch, gated latch.

gate array (n.) A logic device which consists of an array of logic gates (usually NAND) which can be interconnected during fabrication. A custom metallization pattern is used to configure the desired functions. See also: gate, NAND, metallization.

gate equivalency (n.) A rough measure of the complexity of a digital logic integrated circuit. Indicates the approximate number of discrete logic gates that would be needed to implement the same function. See also: gate.

gated latch (n.) Generally refers to an unclocked D-type flip-flop which has a control signal called a gate. When the gate is "open", the flip-flop output follows the data input. When the gate is "closed", the output holds its current state. Also called a transparent latch. See also: flip-flop, unclocked flip-flop, gate, latch.

H

HAL® device (n.) Hard Array Logic device. A version of a PAL device which is configured during fabrication with a custom metallization pattern. HAL is a registered trademark of Advanced Micro Devices. See also: PAL device, metallization.

I

I^2L (IIL) (n., adj.) Integrated Injection Logic. A less common bipolar logic design technique which, when used, is found primarily in portions of LSI and VLSI circuits. See also: bipolar, LSI, VLSI.

integrated circuit (n.) An electronic device which has many transistors and other semiconductor components integrated onto one piece of silicon. Often abbreviated IC.

invert (v.t.) To perform the logical NOT function on a digital signal. To reverse the polarity of a digital signal. See also: polarity, NOT.

inverter (n.) A logic gate which performs logical inversion, or the NOT operation. See also: gate, NOT.

I/O (Input/Output) 1. (n.) The methods and equipment used to pass information into and/or out of a system or device. 2. (adj.) On a programmable logic device, a pin which can function as an input and/or an output.

J

JEDEC 1. (n.) Joint Electronic Device Engineering Council. A council which creates, approves, arbitrates, and/or oversees industry standards for electronic devices. 2. (adj.) In programmable logic, refers to a computer file containing information about the programming of a device. The file format is a JEDEC-approved standard. Used for downloading to programmers. See also: program, programmer, download.

junction isolation (n.) A bipolar integrated circuit fabrication technique which uses P-N functions to isolate transistors. This is the original integrated circuit technology, and is being supplanted by oxide isolation in places where speed is critical. See also: oxide isolation, bipolar.

K

Karnaugh map (K-map) (n.) A graphic tool for minimizing sum-of-products or product-of-sums logic functions. Useful for up to six logic variables. See also: sum-of-products, product-of-sums.

L

latch 1. (n.) A type of flip-flop. Means different things to different people. In general, an unclocked flip-flop. Sometimes used to refer specifically to a gated D-type flip-flop. 2. (v.t.) To capture a signal in a latch. See also: flip-flop, unclocked flip-flop, gate, gated latch.

latch up (v.t.) To enter the latch-up condition. See also: latch-up.

latch-up (n.) A condition in which a circuit draws uncontrolled amounts of current, and certain voltages are forced, or "latched-up" to some level. Used especially in reference to CMOS devices, which can latch up if the operating conditions are violated. See also: CMOS, latch up.

lateral fuse (n.) A thin metal link which is disconnected when programmed. Connected in the blank state, disconnected in the programmed state. Usually just called a "fuse". See also: program, programmed, blank.

LCC (n.) Leadless Chip Carrier. A ceramic integrated circuit package having no leads. Connection is made to metal contacts which are flush with the package. See also: integrated circuit, lead, package.

lead (n.) [l$\bar{e}$d] A metal conductor which provides a connection from the inside of an integrated circuit package to the outside world for soldering or other mounting techniques. See also: integrated circuit.

logic array (n.) Generally an array of programmable cells which attach inputs to logic gates of a specified type. See also: program, gate, programmable cell.

logic simulation (n.) A means whereby a logic design can be evaluated on a computer before actually being built. The computer simulates the behavior of the components to predict the behavior of the overall circuit.

LS (adj.) Low-power Schottky TTL family. Lower power version of the standard Schottky TTL family. See also: TTL, Schottky TTL.

LSI (adj.) Large-Scale Integration. A rough measure of the complexity of a digital circuit. Characterized as having 100–5000 gate equivalents for logic chips, or 1K–16K bits for memory chips. See also: gate equivalent, bit, VLSI, SSI, MSI.

M

macrocell (n.) Typically the output cell of a PLD, containing a flip-flop and path multiplexers.

maxterm (n.) A sum in the canonical product-of-sums form. Each maxterm contains every input variable, in either true or complemented form. See also: product-of-sums, true, complement.

metallization (n.) The process of connecting the various elements of an integrated circuit or printed circuit board by placing a layer of metal over the entire wafer or board, and then selectively etching away unwanted metal. A photolithographic mask defines the pattern of connections. See also: integrated circuit, wafer, printed circuit board.

minterm (n.) A product in the canonical sum-of-products form. Each minterm contains every input variable, either in true or complemented form. See also: sum-of-products, true, complement.

monolithic (adj.) In the electronics industry, refers to a circuit which has been integrated onto one semiconductor chip. Integrated circuits are monolithic by definition. See also: integrated circuit.

monostable (adj.) Describes a system which has 1 stable state. Any other state is unstable, and will eventually change to the stable state. The most common monostable circuit is a "one-shot". See also: bistable, astable.

MOS (n., adj.) Metal-Oxide-Semiconductor transistor. One of the two basic types of transistor. In logic design, used for NMOS, PMOS, and CMOS families. See also: NMOS, PMOS, CMOS, bipolar.

MSI (adj.) Medium-Scale Integration. A rough measure of the complexity of a digital logic circuit. Characterized as having 10–100 gate equivalents. See also: gate equivalent, SSI, LSI, VLSI.

N

NAND (adj.) Not AND. A commonly used logic gate which is equivalent to an AND gate followed by an inverter. The NAND logic operation is functionally complete. See also: gate, inverter, functionally complete, AND.

negative logic (n.) A physical implementation of logic wherein a low voltage level represents a logic 1, or "true", and a high voltage level represents a logic 0, or "false". See also: positive logic, polarity.

NMOS (n., adj.) N-channel MOS. A type of circuit which makes exclusive use of N-channel MOS transistors. See also: MOS, PMOS, CMOS.

non-volatile (adj.) Refers to memory devices which do not lose their contents when power is removed. See also: volatile.

NOR (adj.) Not OR. A logic gate which is equivalent to an OR gate followed by an inverter. The NOR logic operation is functionally complete. See also: gate, inverter, functionally complete, OR.

NOT (adj.) One of the three elementary logic functions. Unary operation whose result is true if and only if the operand is false.

O

OR 1. (adj.) One of the three elementary logic functions. Result of the OR operation is false if and only if all operands are false. 2. (v.t.) To perform the OR operation.

OTP (adj.) One-Time Programmable. Refers to programmable devices which are UV-erasable, but which are not packaged in windowed packages. As a result, there is no way to erase the device, making it programmable only once. See also: program, erase, UV-erasable, windowed package.

oxide isolation (n.) A bipolar integrated circuit fabrication technique which uses silicon dioxide to isolate transistors. This results in higher speed and density. See also: junction isolation, bipolar.

P

package (n.) The encasement which protects a die and provides convenient electrical contact to the die. Materials used are generally ceramic or plastic compounds. There is a variety of shapes and sizes. See also: die.

PAL® device (n.) Programmable Array Logic device. A PLD which implements logic via a programmable AND logic array driving a fixed OR logic array. PAL is a registered trademark of Advanced Micro Devices. See also: program, logic array, sum-of-products, PLD, AND, OR.

PLA (n.) Programmable Logic Array. A programmable logic device which implements sum-of-products logic via a programmable AND logic array driving a programmable OR logic array. See also: program, logic array, sum-of-products, AND, OR.

PLCC (n.) Plastic Leaded Chip Carrier. A molded plastic integrated circuit package with leads shaped like a "J" (J-leads). Intended for surface mounting. See also: integrated circuit, lead, surface mounting, package.

PLD (n.) Programmable Logic Device. Generic term for a logic device whose function can be configured by the customer after purchase. See also: program.

PMOS (n., adj.) P-channel MOS. A type of circuit which makes exclusive use of P-channel MOS transistors. See also: MOS, NMOS, CMOS.

polarity (n.) Specifies the sense of "active" and "inactive", or "true" and "false" in a digital signal. "Active high" represents "true" as a high signal; "active low" represents "true" as a low signal.

positive logic (n.) A physical implementation of logic wherein a high voltage level represents a logic 1, or "true", and a low voltage level represents a logic 0, or "false". See also: negative logic, polarity.

power dissipation (n.) The amount of electrical power used by a device. Calculated as the product of the operating voltage and current. Measured in watts (W) or milliwatts (mW), as appropriate. Sometimes incorrectly used to refer to the operating current only.

printed circuit board (PC board, PCB) (n.) A board for assembling electrical components. Component connections are made by metal traces which have been fabricated through a metallization process. See also: trace, metallization.

product-of-sums (POS) (adj.) A representation of a logic function where the input signals are individually inverted (if necessary), then ORed together to form sums which are ANDed together. Any combinatorial logic function can be represented in product-of-sums form. See also: sum-of-products, combinatorial, AND, OR.

product term (pterm, p-term) (n.) An AND gate in a PLD which implements sum-of-products logic. See also: sum-of-products, PLD, AND, gate.

product term sharing (n.) See product term steering.

product term steering (n.) A means whereby product terms in a PAL device can be routed to one of two device outputs, instead of being dedicated only to one output. Sometimes called "product term sharing". See also: product term, PAL device.

program 1. (v.t.) As used in programmable logic, to configure a blank device so that it can perform some desired function. Applies to memory and logic devices. Opposite of "erase". 2. (v.t.) To change an individual programmable cell from a blank state to a programmed state. See also: blank, programmable cell, programmed, erase.

programmable cell (n.) Any of a variety of cells which can be altered by applying certain electrical signals. Various types are lateral and vertical fuses, UV cells, E^2 cells, and even RAM cells. All but RAM cells are non-volatile. See also: lateral fuse, vertical fuse, UV cell, E^2 cell, RAM cell, non-volatile, volatile.

programmed (adj.) Describes the state of a programmable cell or device after programming. Opposite of "blank".

programmer (n.) A device or machine used for configuring, or "programming", PLDs or PROMs. See also: program, PLD, PROM.

PROM (n.) Programmable Read-Only Memory. A nonvolatile memory device whose contents are programmed by the customer. Once programmed, it cannot be erased. Also functions as a PLD with a fixed AND logic array which drives a programmable OR logic array. See also: program, erase, EEPROM, EPROM, ROM, RAM, non-volatile, AND, OR, logic array.

R

RAM (n.) Random-Access Memory. Sometimes called read/write memory. A type of memory device which can be written to and read at any time. Such memory is volatile. Actually a misnomer, since most types of memories can be accessed randomly. The distinguishing feature is the fact that RAM is designed specifically to be written to in normal usage. See also: ROM, volatile.

RAM cell (n.) A cell which is used make one bit of volatile memory in a RAM. Can also form the basis of a programmable logic connectivity array. See also: RAM, volatile.

ROM (n.) Read-Only Memory. A nonvolatile memory device which has its contents defined when manufactured. No changes can be made to the memory contents. See also: PROM, EPROM, EEPROM, RAM, non-volatile.

S

Schottky TTL (adj.) Family of TTL devices which make use of Schottky diodes for higher speed. See also: TTL.

security fuse (n.) A PLD feature which allows a user to "secure" the PLD after programming. This prevents subsequent copying of the contents of the PLD. See also: PLD, program.

semicustom (adj.) Refers to a circuit which has been partially designed by the device vendor, and partially designed, or configured, by the customer. Primary types are PLDs, gate arrays, and standard cell circuits. See also: PLD, gate array, standard cell.

sequential (adj.) Refers to a logic circuit whose operation depends both on present input signals and previous operations, or states. Requires some kind of memory (usually flip-flops) for remembering past states. See also: flip-flop, combinatorial.

SSI (adj.) Small Scale Integration. A rough measure of the complexity of a digital logic circuit. Characterized as having less than 10 gate equivalents. See also: gate equivalent, MSI, LSI, VLSI.

standard cell (n.) A method of designing semicustom or full custom circuits whereby predefined cells are brought together to provide the specified function. Unlike gate arrays, all fabrication steps are customized, instead of just the metallization step. See also: semicustom, gate array, metallization.

standby power (n.) The power consumed by a device when none of the device inputs are switching. Usually used in reference to CMOS devices, many of which consume practically no standby power. See also: CMOS.

sum-of-products (SOP) (adj.) A representation of a logic function where the input signals are individually inverted (if necessary), then ANDed together to form products which are ORed together. Any combinatorial logic function can be represented in sum-of-products form. See also: product-of-sums, combinatorial, AND, OR.

surface mounting (n.) A printed circuit board assembly technique whereby the integrated circuit packages are placed on the board with no leads protruding through to the other side. Packages can thus be mounted on both sides of the board. See also: printed circuit board, lead, through-hole mounting.

synchronous 1. (adj.) Describes a sequential logic system wherein all operations are synchronized to a common clock. 2. (adj.) Describes signals whose behavior and timing are synchronized to a clock. 3. (adj.) Describes a communication protocol whereby the timing of various operations is determined by a system clock. See also: sequential, clock, asynchronous.

T

temperature compensation (n.) A circuit feature which allows some electrical characteristics to remain relatively constant with some variation in operating temperature.

three-state (adj.) A type of logic device output which can be in one of three-states: HIGH, LOW, and OFF, or High-Z (high impedance). When enabled (on), performs as a normal binary output. When disabled (off), acts as an open pin. See also: enable, disable, binary.

through-hole mounting (n.) A printed circuit board assembly technique whereby the leads of the various components extend through holes in the board. These leads are then soldered from the opposite side of the board. See also: printed circuit board, lead, surface mounting.

trace 1. (n.) During logic simulation, the behavior of a signal or group of signals. The results can sometimes be stored in a "trace file" on disk for later analysis. 2. (n.) A thin layer of metal on a printed circuit board which provides connections between components. Performs the function of a wire. See also: logic simulation, printed circuit board.

transparent latch (n.) See gated latch.

TRI-STATE® (adj.) See three-state. TRI-STATE is a registered trademark of National Semiconductor Corp.

true (adj.) Refers to a signal which is identical to some reference signal, with the same polarity. Opposite of "complement". See also: complement, polarity.

TTL (adj.) Transistor-Transistor Logic family. The most widely used family of bipolar logic devices. The name refers to the particular circuit design technique used. See also: bipolar.

U

unclocked flip-flop (n.) A flip-flop that changes state as soon as the appropriate control signals are applied. See also: flip-flop, clocked flip-flop.

upload 1. (v.t.) To pass data from one machine to a more complex machine. 2. (n.) The act of uploading data. See also: download.

UV cell (n.) A floating gate cell which can be erased by exposure to ultraviolet (UV) light. See also: floating gate, erase.

UV-erasable (adj.) Refers to devices or programmable cells which can be erased when exposed to ultraviolet (UV) light for a period of time. See also: programmable cell, erase.

V

vertical fuse (n.) A transistor arranged such that the emitter and base are shorted together when programmed. Disconnected in the blank state, connected in the programmed state. See also: program, programmed, blank.

VLSI (adj.) Very Large Scale Integration. A rough measure of the complexity of a digital circuit. Characterized as having 5000 or more gate equivalents for logic chips, or 16K or more bits for memory chips. See also: gate equivalent, bit, SSI, MSI, LSI.

volatile (adj.) Refers to memory devices which lose their contents when power is removed. See also: non-volatile.

voltage compensation (n.) A circuit feature which allows some electrical characteristics to remain relatively constant with some variation in the supply voltage.

W

wafer (n.) A round slice of very pure silicon which is used in the fabrication of integrated circuits. Several circuits can be built on one wafer. See also: integrated circuit.

windowed package (n.) A package which has a quartz window in the lid directly over the die. This makes it possible to expose the die to ultraviolet light for erasing the device. See also: erase, die, package.

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TWX: 910-917-4040

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TWX: 910-444-2067
FAX: 206-746-7425

Anthem Electronics
5020 148th Avenue NE, Suite 103
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Tel: (206) 881-0850
FAX: 206-885-4041

Arrow/Kierulff Electronics
19450 68th Avenue South
Kent, Washington 98032
Tel: (206) 575-4420
FAX: 206-575-4427

Hamilton/Avnet Electronics
Redmond Science Park, Bldg. C
17761 N.E. 78th Place
Redmond, Washington 98052
Tel: (206) 881-6697
FAX: 206-867-0159

Wyle Labs/EMG
15385 N.E. 90th
Redmond, Washington 98052
Tel: (206) 881-1150
FAX: 206-881-1567

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200 N. Patrick Boulevard
Brookfield, Wisconsin 53005
Tel: (414) 792-0150
TWX: 910-262-1193

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20875 Crossroads Circle
Waukesha, Wisconsin 53186
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Schweber Electronics
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INTERNATIONAL SALES REPRESENTATIVES AND DISTRIBUTORS

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TELEX: AA 33288 (RADET)

R and D Electronics
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Tel: (61) 439-5488

AUSTRIA
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A-1150 Wien
Tel: 43 222 838519

Ing E. Steiner
Hummelgasse 14
A-1130 Wien
Tel: 43 222 827474-0
TELEX: 135026

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Terlindenhofstraat 36, Bus 7
P.O. Box 110
2060 Antwerpen-Merksem
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TELEX: 73026

D & D Electronics PVBA
Viide Olympiadelaan 93
2020 Antwerp

EBV Electronik
Brucargo Bldg. 724
B-1931 Zaventum

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Icotron
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6 to Andar 05110
San Paolo SP
FAX: 011-55-11-833-2781

DENMARK
C-88 A. S.
Kokkedal Industipark 42A
DK-2980 Kokkedal
Tel: 45 2 24 48 68

FINLAND
Field OY
Nittylanpolku 10
SF-00620 Helsinki
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TELEX: 122022
FAX: 358 0 798853

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TELEX: 404695

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F-78152 Le Chesnay
Tel: 39 54 91 13
TELEX: 698376F

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Lyon
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TELEX: 900738

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31700 - Blagnac
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TELEX: 532103

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TELEX: 375446

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92100-Boulogne

Datadis
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33700 - Mérignac

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TELEX: 560627

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35510 Cesson Sevigne
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TELE: 741127

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F-31320 Esqualquens
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TELEX: 520927

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F-94520 Gentilly BF 78
Tel: 33 46 64 11 01
TELEX: 201069

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RTF
23, Av. Du Granier
Zac Les Bealieres
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TELEX: 5213059

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46300 Bochum 6
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Astronic GmbH
Winzerer Str. 47 D
D-8000 München 40
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TELEX: 521687

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D-3006 Burgwedel 1/Hannover
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TELEX: 943694

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TELEX: 8517605

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Tel: 089 61105-1
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7000 Stuttgart 1
Tel: 49-711-61910-0
TELEX: 722271

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1000 Berlin 10
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TELEX: 185323

Electronic 2000
Heinrich-Hertz, Str. 34
D-4000 Dusseldorf-Erk.
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TELEX: 8586810

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Schmidt Str. 49
6000 Frankfurt/M1
Tel: 49 69 730481
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Tel: 49 7156 24091
TELEX: 7245265

Electronic 2000
Uberseering 25
2000 Hamburg 60
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TELEX: 2164921

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8000 München 82
Tel: 49 89 42001-0
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Mueller Wuppertal
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D-5600 Wuppertal
Tel: 49 202 426016
TELEX: 8591543

Spoerle Electronic
Gneisenau Strasse 2
1000 Berlin 61
Tel: 49-30 693 4090
TELEX: 18029

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Tel: 49-231-21801-0
TELEX: 822555

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TELEX: 417972

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D-2000 Hamburg 54
Tel: 49-40 54 0091-0
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D-8043 Unterfohring b. München
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TELEX: 5216379

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TELEX: 622996

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HONG KONG
Tektron Electronics
1702 Bank Centre
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Kowloon
Tel: 3 880 629
FAX: 852-3-7805871

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San Jose, California 95122
Tel: (408) 294-2833

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TELEX: 31407
FAX: 353 1 453625

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Malahide
County Dublin
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TELEX: 31407

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Amtronics Ltd
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P.O. Box 1276
IL-64075 Tel Aviv
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ITALY
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1-40122 Bologna
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7/B, 50133 Firenze
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Asahi Glass Company, Ltd.
2-1-2, Marunouchi
Chiyoda-ku, Tokyo 100
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TELEX: 81-3-212-0568

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Seiwakai Bldg.
7-12-, 3-chome, Misaki-cho
Chiyoda-ku, Tokyo 101
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TELEX: 2722204 Dainic J
FAX: 03-234-8660

Internix Inc.
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7-4-7 Nishi Shinjuku
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Tel: 03-447-4141

Matsushita Elect Trading Co
4-3-2 Minami Semba
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Osaka 542
Tel: 06-282-5590
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7-9-17, Nishi-Shinjuku
Shinjuku-ku, Tokyo 160
Tel: 03-371-1811
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Nihon Denshikizai Co., Ltd.
2-20-10 Minamikaneda
Suita-shi, Osaka 564
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1-26-2, Nishi-Shinjuku-ku
Tokyo 160
Tel: (03) 343-4411

KOREA
ENC
#1602-4, Shucho-Dong
Kang Nam -Ku
Seoul
Tel: 82-2-582-5996

Gold Star Semiconductor Ltd.
Kuk Dong Building
60-1 Choongmu-RO 3-KA, Jung-Gu
C.P.O. Box 9495
Seoul 100
Tel: 82 2 274 3219
TELEX: GOLD SEC K22767 27923

NETHERLANDS
Arcobel BV
Griekenweg 25
P.O. Box 344
NL-5340 AH Oss
Tel: 04120 30335
TELEX: 37489

NORWAY
OTE Komponent
Postboks 102 Tveita
N-0617 Oslo 6
Tel: 47 2 26 9955
TELEX: 78955

SINGAPORE
Dynamar Computer Products LTD.
109 Defu Lane 10
Hougang Avenue 3
Singapore 1953

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7500A Beach Road
#09-322 The Plaza
Singapore 0719
Tel: 65-295-4604
TELEX: RS 39142 Impact

SOUTH AFRICA
Promilect Pty. Ltd.
275 Kent Avenue
P.O. Box 1184
Randburg 2125

SPAIN
Kontron S.A.
Gran Via De Carlos III, 94-10-1
E-08028 Barcelona
Tel: 34-3-33 07713
TELEX: 52220

Kontron S.A.
Avenida Ejercito, 87
E-48015 Bilboa
Tel: 34-4-4478189

Kontron S.A.
C/, Salvatierra N5
E-28034 Madrid
Tel: 34-1-729 1155
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E-08006 Barcelona
Tel: 34 3 2126583
TELEX: 97317

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E-Madrid-1
Tel: 34 1 4026085
TELEX: 43819

SWEDEN
Gösta Bäckstrom (AB)
Box 11026
S-220 11 Lund
Tel: 46-15-03-45

Gösta Bäckstrom (AB)
Box 12009
Alstromergata 22
S10221 Stockholm
Tel: 46-8-541080
TELEX: 10135

Naxab
Box 4115
S-17104 Solna

SWITZERLAND
Kontron AG
Components Division
Berner Strasse Sud 169
CH-8010 Zurich
Tel: 41-1-4354111
TELEX: 45-822 196

TAIWAN
ASEC
7F No. 344/1 Min-Sheng
East Road
Taipei
Tel: (02) 505-7025
FAX: 02-501 1524

Wei Keng Ind. Co. Ltd.
Rm. B2. Fl. 7
No. 126, Sec 4
Nanking E Road
P.O. Box 17-304
Taipei
Tel: 2-7763512

UNITED KINGDOM
Alpha Electronic Components, Ltd.
Jubilee House
Jubilee Road
Letchworth,
Hertfordshire SG7 1QJ
Tel: 44-462-480888
TELEX: 826505

Axiom
Turnpike Road
Cressex Estate
High Wycombe Buckinghanshire
HP12 3NR
Tel: 44 494 461616

Kudos/Thame Ltd.
55 Suttons Park
London Road
Reading
Berkshire RG6 1AZ
Tel: 44-734-351010
TELEX: 847575

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Burnham Lane
Slough
Berkshire SL1 6LN
Tel: 44-6286-4383
TELEX: 847945

Rapid Silicon Ltd.
Rapid House
Denmark Street
High Wycombe
Buckinghamshire
HP1 2ER
Tel: 44-494-442266
TELEX: 837931